Chapter Four OPERATION OVERVIEW

Chapter Four O P E R A T I O N O V E R V I E W

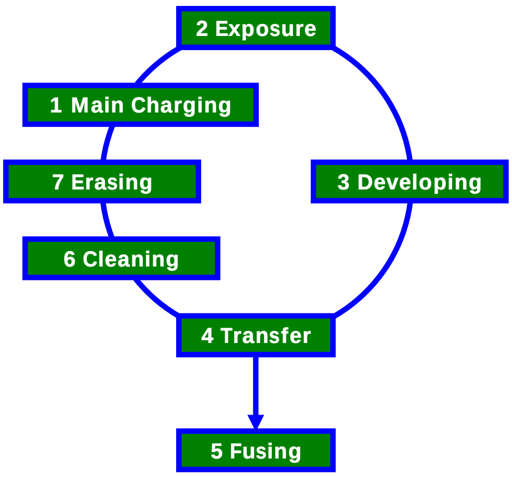
Electrophotographics system

Electrophotography is the technology used in laser printing which transfers data representing texts or graphics objects into a visible image which is developed on the photosensitive drum, finally fusing on paper, using light beam generated by a laser diode.

The key features for the electrophotography system used in the FS-1700 and FS-3700 printers are:

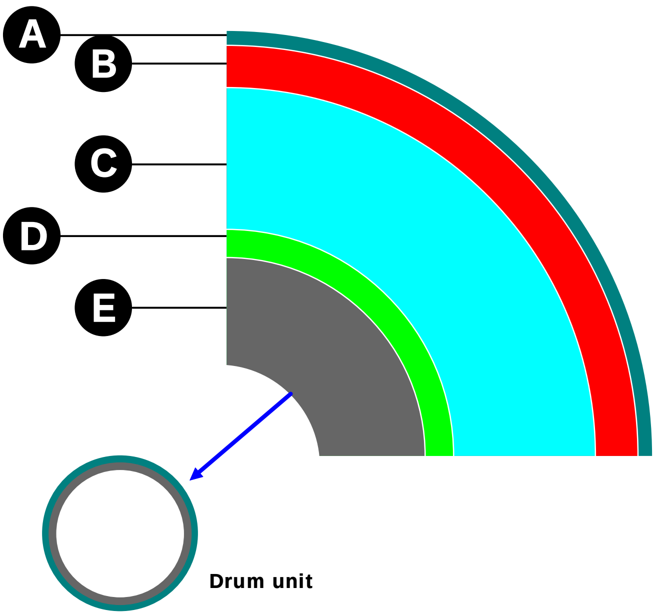
- 600 dpi resolution
- Newly developed amorphous silicon drum with no heating device
- Diode laser scanning
- Mono component toner

The electrophotography system of the printer performs a cyclic action made of seven steps as shown below.



Amorphous-silicon drum

The printer uses the long lasting amorphous silicon drum. The drum surface is a composite of five substances coated in five layers as shown below.



A Secondary protection layer

B Primary protection layer (1µm)

C Photoconductor α-Si (15µm)

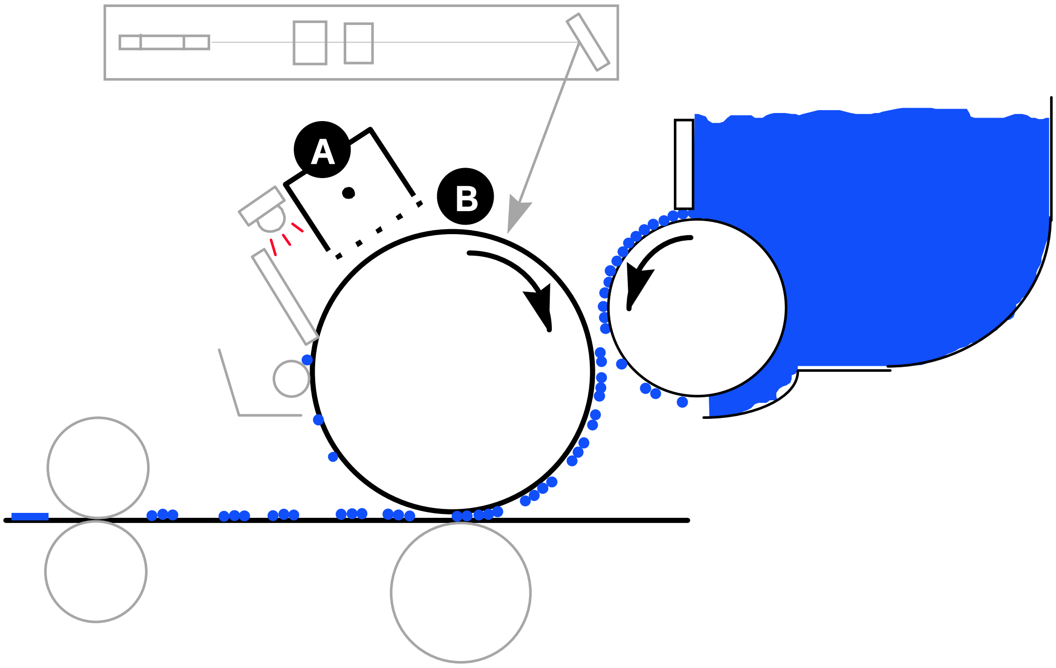
D Carrier block (1-3µm)

E Aluminum base

The primary and secondary layers are for protecting the amorphous silicon layer underneath. The amorphous silicon layer is of photoconductive, meaning it can be electronically conductive when exposed to a (laser) light source to effectively ground electrons charged on its outer surface to the ground. The carrier block layer lies between the amorphous silicon layer and the aluminum base cylinder and prevents the backward electron flow, from the base cylinder to the drum's outer surface, which might give adverse effect (usually "ghost") on the print quality.

Charging the drum

Figure below is a simplified diagram of the electrophotographics components. Charging the drum is done by the main charger wire (in the main charger unit) marked A in the diagram.

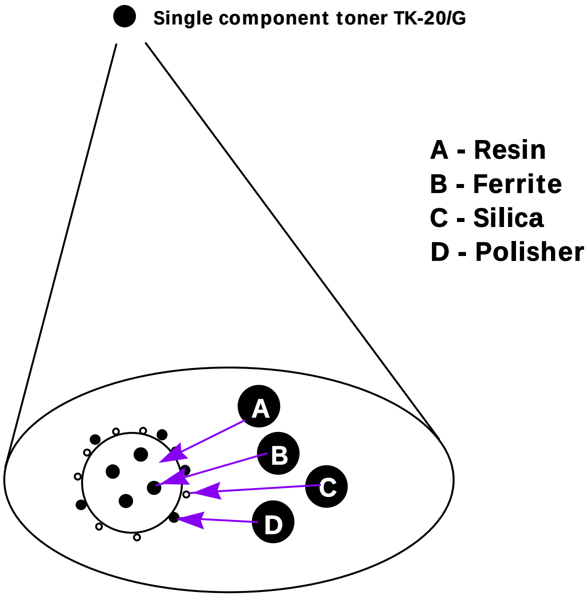


As the drum (B) rotates in a “clean (neutral)” state, its photoconductive layer is given a uniform, positive (+) electrical charge dispersed by the main charger wire (A).

Due to high-voltage scorotron charging, the charging wire can get contaminated by oxidization and therefore must be cleaned periodically from time to time using the method explained in section Main charger unit on page 3-7. Cleaning the charging wire prevents print quality problems such as black streaks caused by the oxide ac-cumulated around the charging wire.

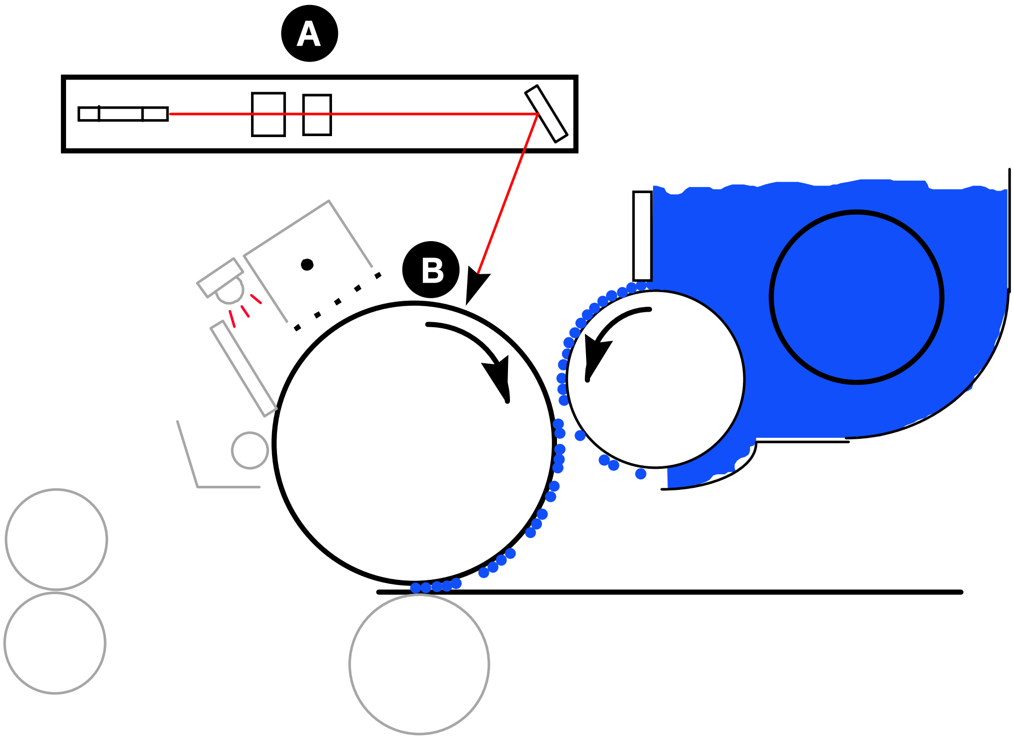
Toner

The toner is fed from the toner pack TK-20/G. The toner is comprised of the following substances as depicted below.

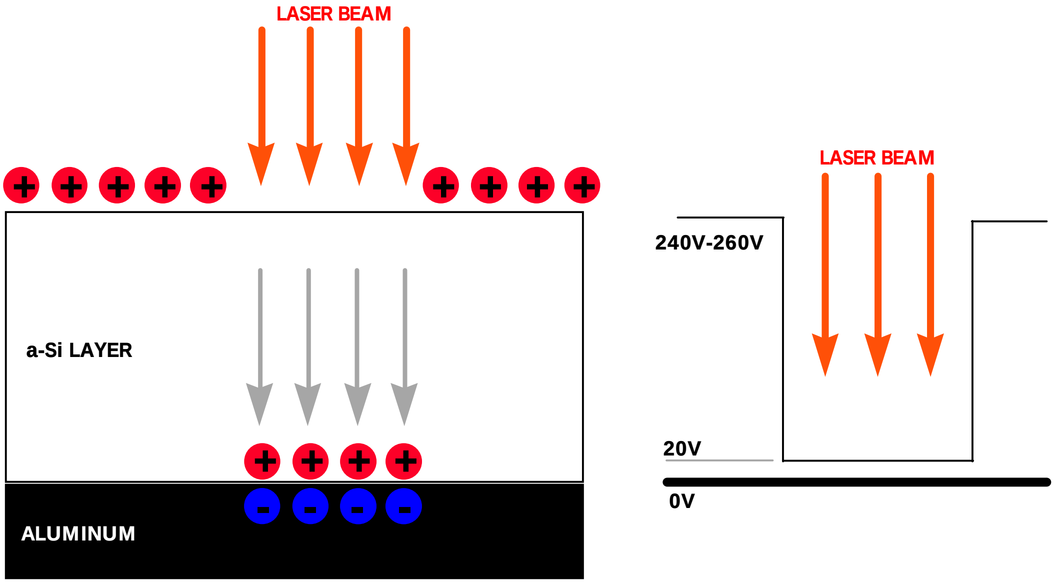

Single component toner TK-20/G
A - Resin
B - Ferrite
C - Silica
D - Polisher
A
B
C
D

Exposure

The charged surface of the drum (“B”) is then scanned by the laser beam from the scanner unit (“A”).

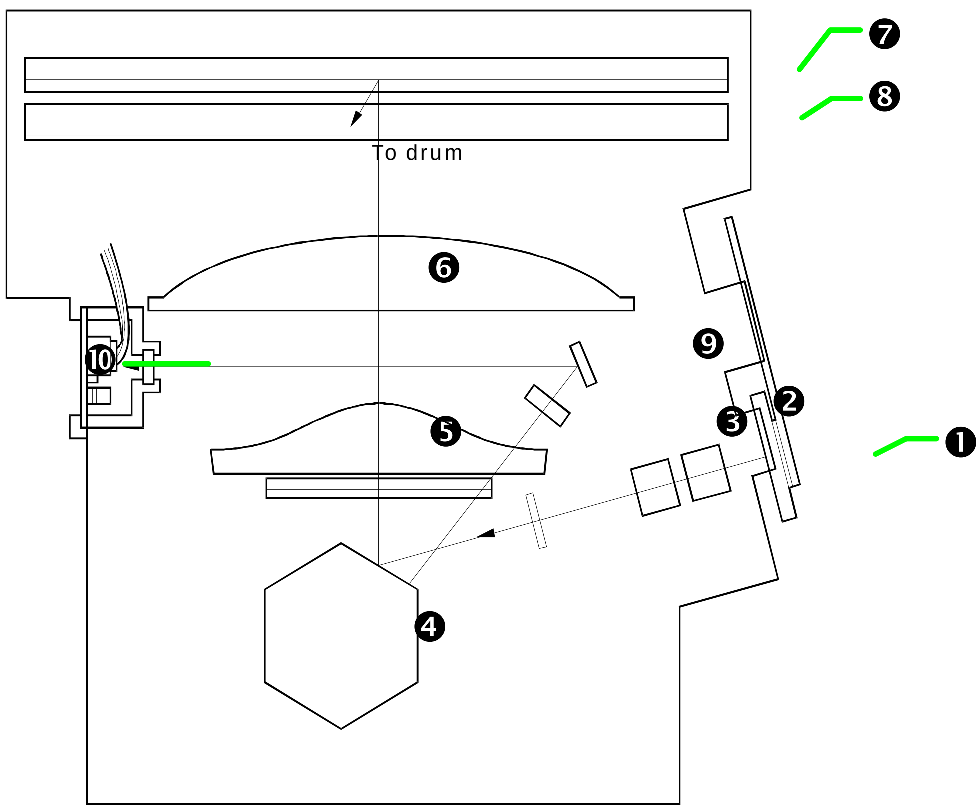


The laser beam is switched on for a black dot and off for a white (blank) dot according to the print data. Whenever it is illuminated by the laser beam, the electrical resistance of the photoconductor is reduced, the potential on the photoconductor is also lowered from approx. 260V (FS-1700) or 240V (FS-3700) to 20V, effectively driving the charge through the a-Si layer down to the aluminum base.



Scanner unit

The 600 dpi scanner unit includes the diode laser that produces the 670 nm wavelength laser beam. This wavelength is specifically designed to match the photoconductive response of amorphous silicon.



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The illustration shows the laser scanner for model FS-3700.

❶ Laser diode - emits diffused, visible laser.

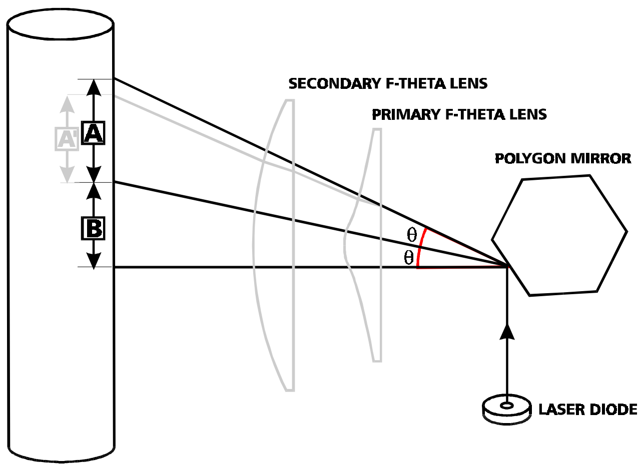
❷ Collimeter lens - aligns the laser beam to the cylindrical lens.

❸ Cylindrical lens - compensates the slant angle at which the laser beam hits a polygon mirror segment.

❹ Polygon mirror (motor) - has six mirror segments around its octagonal circumference; each mirror corresponding to one scanned line width on the drum when laser beam scans on it.

❺ Primary f-theta lens - See below.

❻ Secondary f-theta lens - The primary (above) and secondary f-theta lenses equalize focusing distortion on the drum edges. The effective length of line (“A,” “B” below) the laser beam draws on the drum becomes longer as the laser beam hits closer to the drum edges. In the figure below, distances represented by “A” and “B” are not the same (A>B) until the f-theta lenses are provided between the polygon mirror and the drum (A’=B).



❼ Diversion mirror - diverts the laser beam vertically onto the drum. Note the diffused laser beam finally pin-points on the drum.

❽ Protective glass - prevents dust, debris, etc., from entering the scanner assembly.

❾ Sensor mirror - bends the very first shot of a laser scan towards the beam detection sensor (See next.).

❿ Beam detector sensor - when shone by the sensor mirror above, this photosensor generates a trigger signal for the engine controller to start activating the paper feeding system.

Scanning laser

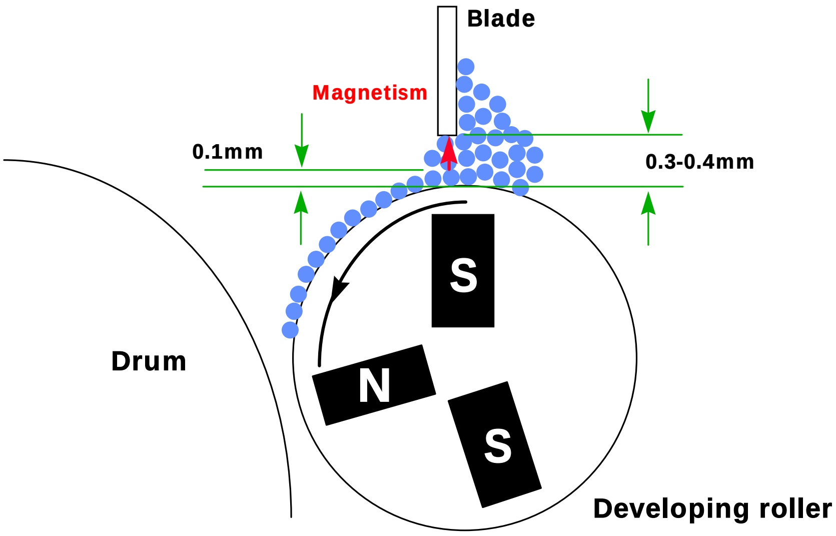
The laser beam hits one of six polygonal mirrors. As the mirror revolves (at the revolution of 17,000 rpm for model FS-1700; 27,000 rpm for model FS-3700), the laser beam reflects off of it and reaches the charged drum surface in a lengthwise manner.

A pair of (plastic) lenses provides focusing the horizontally sweeping laser beam onto the drum. As the drum rotates, the laser beam sweeps the entire length of the drum so that the drum's entire circumference is exposed to the laser beam. The revolution of the polygon mirror motor and the drum itself is timing-controlled so that each successive sweeping of the laser beam produces a $^{1}/_{600}$ inch offset. The printer's controller system continuously turns the laser beam on and off to put a dot at every $^{1}/_{600}$ inch distance horizontally. The diameter of a dot is typically 70 µm.

Synchronizing the output data with one scanning line is achieved by the photo sensor provided next to the first mirror. At the beginning of each laser sweeping, the beam hits the photo sensor which in turn sends a command to the logic controller for synchronization.

Development

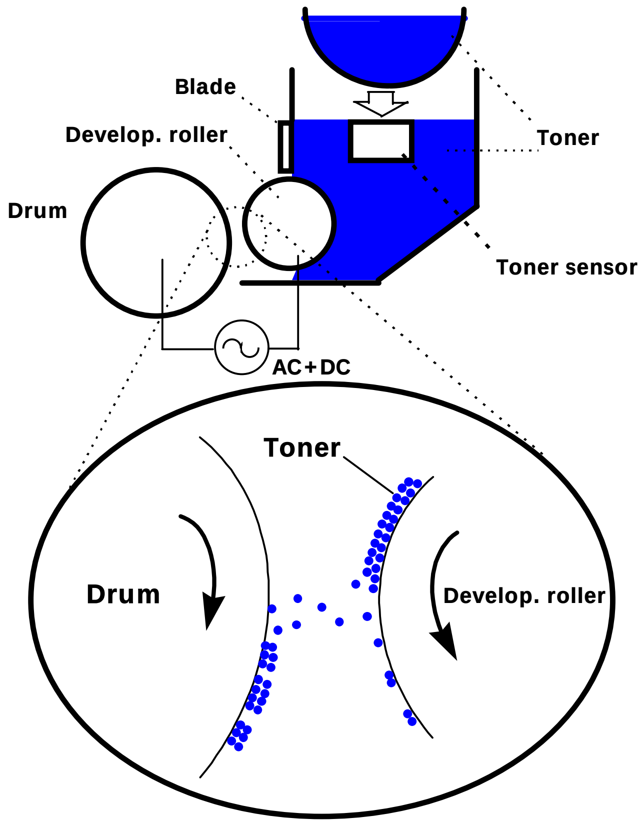
The latent image constituted on the drum is *developed* into a visible image. The developing roller contains a 3-pole (S-N-S) magnet core and an aluminum cylinder rotating around the magnet core. Toner attracts to the developing roller since it is powdery ink made of black resin bound to iron particles. A magnetized blade positioned approximately 0.3 mm above the developing roller constitutes a smooth layer of toner in accordance with the roller revolution.

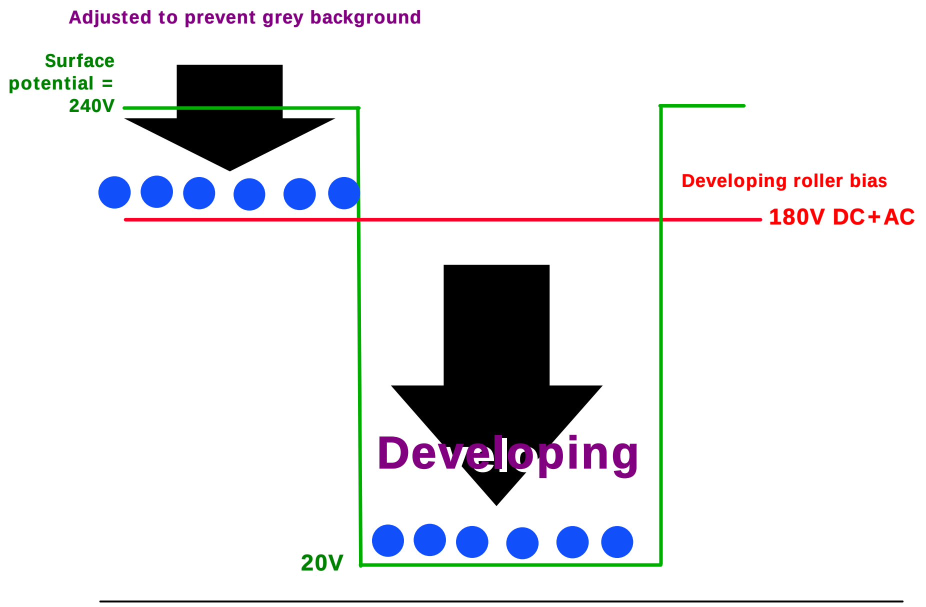


Developing roller bias

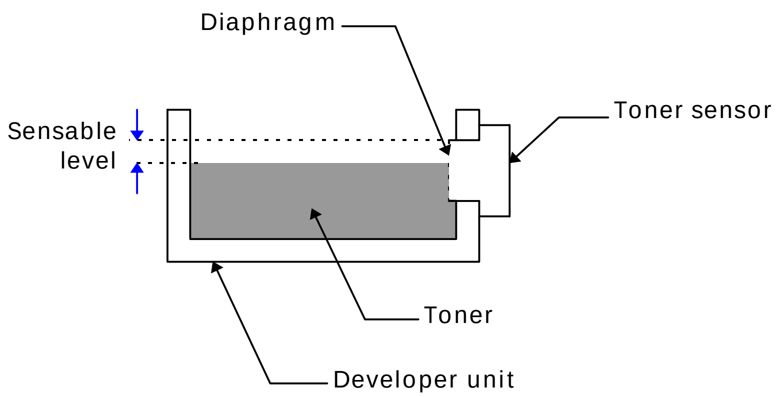
The developing roller is connected to a AC-weighted, positive DC power source. Toner on the developing roller is given a positive charge. The positively charged toner is then attracted to the areas of the drum which was exposed to the laser light. (The gap between the drum and the developing roller is approximately 0.3 mm.) The non-exposed areas of the drum repel the positively-charged toner as these areas maintain the positive charge.

The developing roller is also biased with an ac potential to apply compensation to the toner's attraction and repelling actions for more contrast in the development.





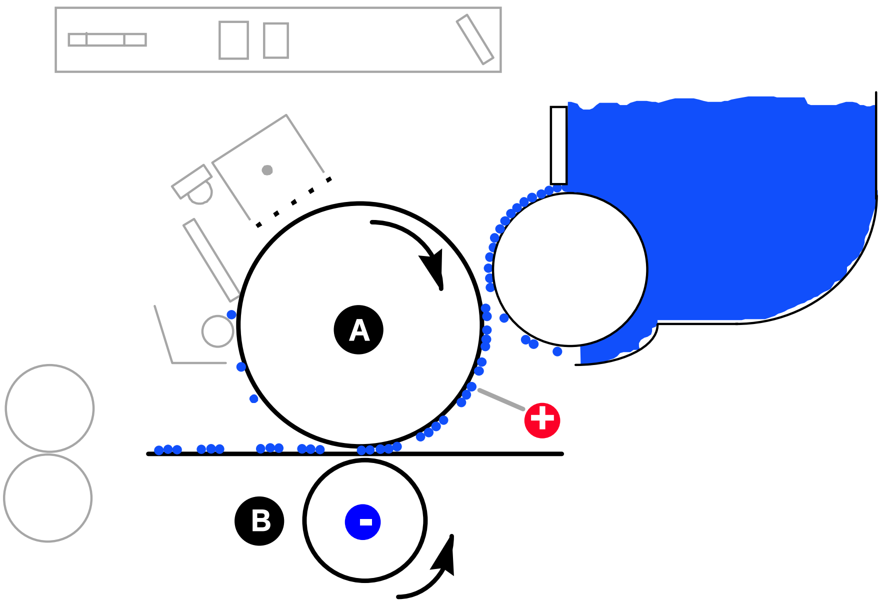
A toner replenishment sensor is provided within the developer. As the toner supply from the toner container dwindles and the toner level lowers in the reservoir, the sensor translates it through its diaphragm, urging the toner motor to feed more toner.



Transfer

The image developed by toner on the drum ("A" below) is transferred onto the paper using the electric charge attraction given by the toner itself and the transfer roller ("B" below). The transfer roller is negatively biased so that the positively charged toner is attracted onto the paper while it is pinched by the drum and the transfer roller.

The paper is automatically peeled off the drum because of the small diameter of the drum. To prevent thin paper wrapping around the drum, the static discharger brush is provided to reduce the attraction of the negatively charged paper to the positively charged drum.

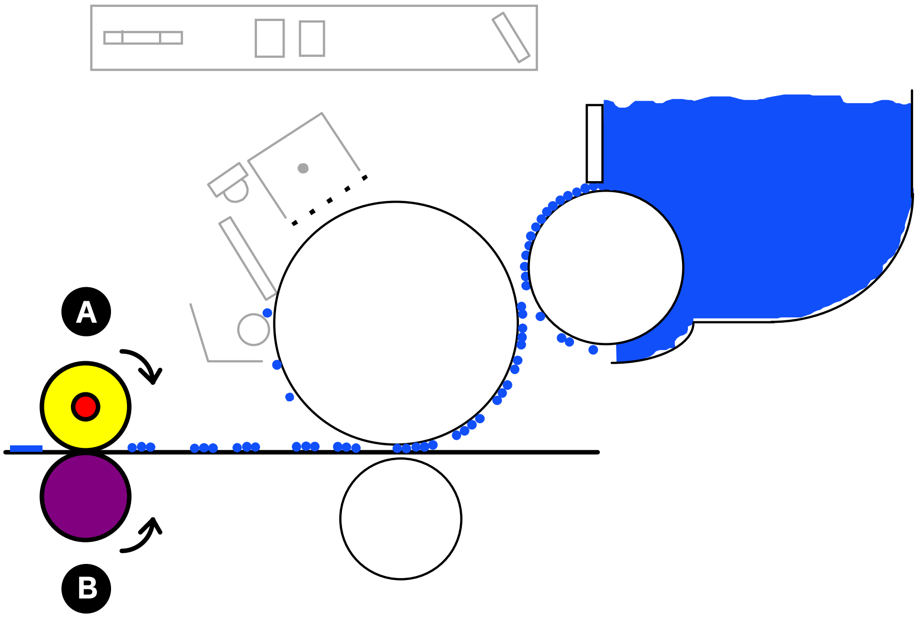


The nominal transfer bias is set to approximately -1.80 kV (limit) with the current of 65±2μA. Since thicker paper (91 to 200 g/m^2) such as postcards, OHP, envelopes, etc., tend to require more bias potential for the satisfactory transferring process, the transfer bias is user-switchable to -2.45 kV (limit) by using the printer's operator panel. Double-sided printing using a DU-20 duplexer automatically increases the transfer bias to the above value.

Fusing

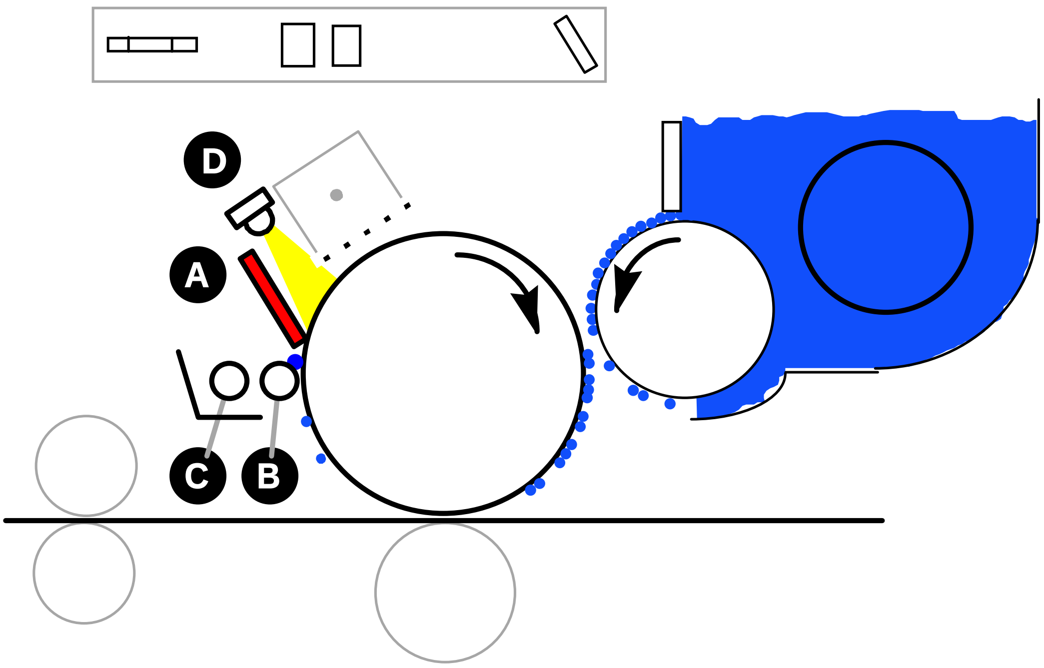
The toner on the paper is permanently fused onto the paper as it passes between the florin-finished heat roller (“A” below) and the pressure roller (“B” below) in the fuser unit. The toner is molten and pressed into the paper. The heat roller has a halogen lamp, turning frequently on and off to maintain a preheat temperature at approximately 175°C.

The heat roller temperature is constantly monitored by the engine control circuit using a thermistor. For safety against overheating, the fuser system is protected by a triac which automatically opens power to the halogen lamp. If the temperature exceeds 350°C, it activates the thermo-cut device to interrupt open power to the halogen lamp.



Drum cleaning and erasing static charge

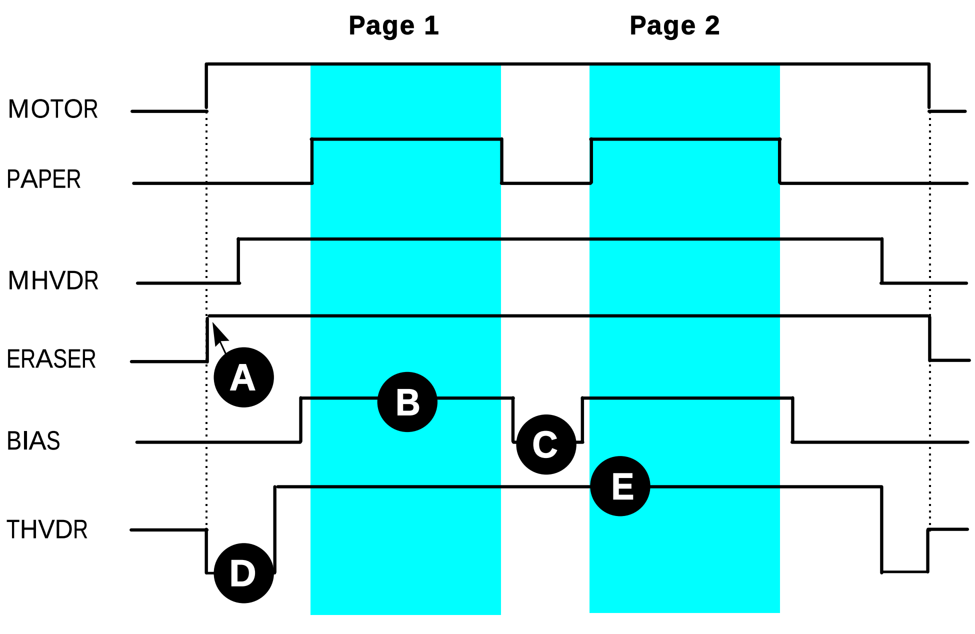
The drum needs to be physically cleaned of toner remaining on its surface in the previous rotation. The cleaning blade (A below) is constantly pressed against the drum and scrapes the residual toner on the drum off to the refresher roller (B below). The refresher roller drives the toner to the spiral (fins) roller (C below) at one end of which the waste toner bottle is connected to collect the waste toner.



After the drum is physically cleaned, it then must be cleaned to an electrically neutral state. This is necessary to erase any residual positive charges, ready to accept the next uniform charge. The residual charge is canceled by exposing the drum to the light emitted from the eraser LED (D above) in the similar manner as described in page 4-6. This lowers the electrical conductivity of the drum surface making the residual charge on the drum surface escape to the ground.

Typical photo process timing chart

The following chart shows the signals used for photo processing. These signals activate the corresponding device in the following timing sequences. A simple description for these signals follow.



MHVDR (Main High Voltage DRive) - drives main charger with high voltage bias. This signal is kept on during the job is processed.

ERASER - turns on the eraser (LED array) as soon as the motor begins revolving (A above).

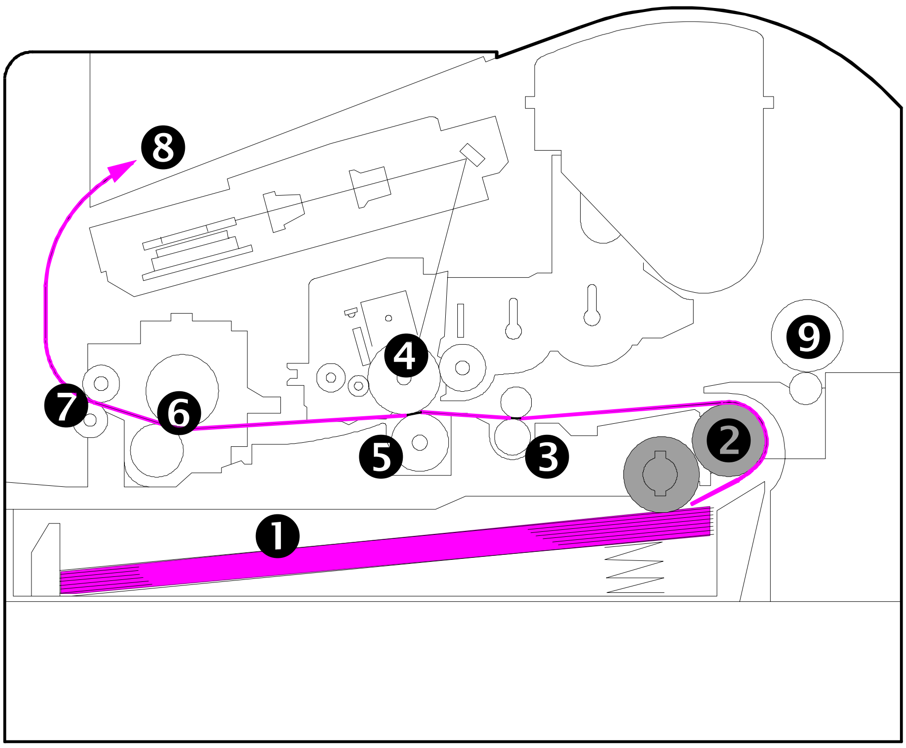
BIAS - turns on the developer bias (on the magnet roller). The duration of this signal is dependent on the current paper size (B) and turns off between pages (C).

THVDR (Transfer High Voltage Drive) - turns on the transfer bias. Note that the transfer bias is reverse (+300V) at the beginning of a print job (D)until the paper is actually fed onto the transfer roller. This prevents contamination on the back side of paper by effectively repelling the toner during the paper is not present between the drum and the transfer roller. The transfer bias is kept on during a print job (E).

Paper feeding system

The paper feeding system picks up paper from the paper cassette or the manual feeding tray and at a precise timing feeds it to the electrophotography system for developing image on the paper. It finally delivers the printed page to either the face-down or face-up tray.

The figure below shows the paper feeding path within the printer.



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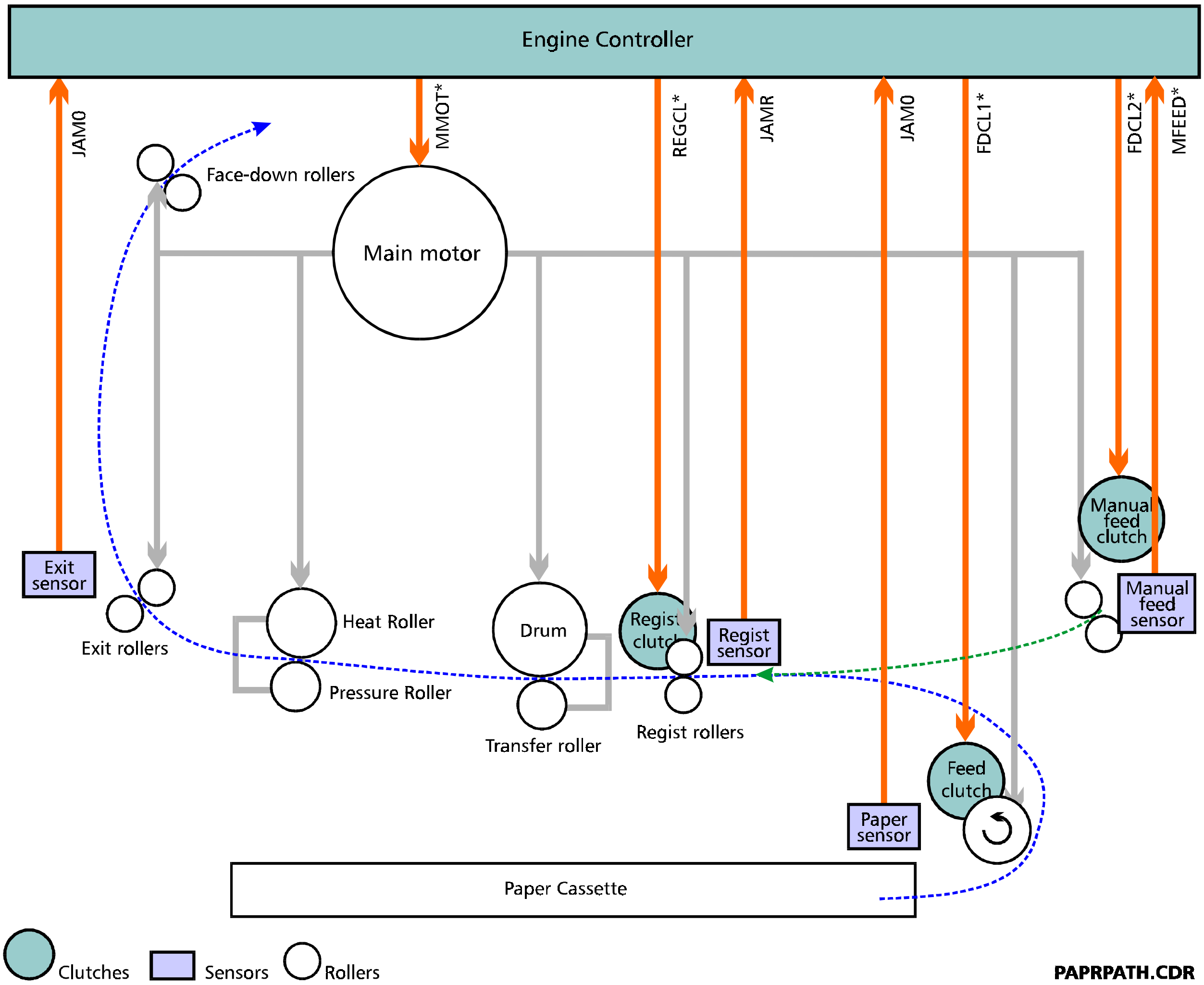
❶Paper (cassette). ❷Paper feed roller+clutch+sensor. ❸Registration rollers+clutch+sensor. ❹Drum. ❺Transfer roller. ❻Fuser rollers. ❼Exit rollers+sensor.❽Face-down output tray+sensor (FS-3700 only). ❾Manual feed roller+clutch+sensor.

Following on the next page is another diagram showing locations of sensors, roller, and solenoids arranged along with this paper path.



Paper feed components/signals

Cassette feeding

The main logic controller sends the PRINT* signal to the engine controller after finishing data processing. The engine controller CPU then starts the main motor (MMOT), polygon motor, registration rollers, and the fuser heater. The engine controller then issues the FDCL1 signal to connect the main motor power to the paper feed tires. The tires feed the top sheet in the paper stack in the cassette towards the registration rollers until the paper reaches the registration jam sensor (JAMR). As the engine controller sends VSREQ to the main logic controller, the main logic controller subsequently issues VSYNC to activate the registration rollers, thus starting to feed paper towards the drum.

The paper is advanced to the drum, to the fuser unit, triggering the exit sensor (JAM0), and finally delivered either to the face-down tray or the face-up tray as switched by the output stack selector tab.

Manual/multi purpose tray feeding

The printer recognizes the existence of paper on the manual feed or multi purpose tray when the manual feed sensor is pushed up (HANDS).

In manual paper feed mode, the paper placed on the manual feeding tray or multi purpose tray is drawn in when the manual feed clutch is energized by the FDCL2 signal to drive the manual feed roller.

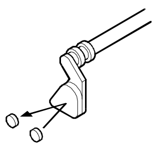
The subsequent print process is identical to the above section.

Paper jam sensing

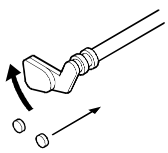
The registration sensor and the exit (fuser) sensor keep track of the paper sent through the printer's paper path by watching the time of period during which either sensor is kept activated.

Registration sensor - A photo reflector sensor is used. While the paper is not present (❶), the reflector (shiny mirror surface) at the end of the actuator is in the position that can reflect the light to shine the receptor. As the top edge of the paper reaches the registration sensor, the reflector is pushed up and the light is interrupted(❷), triggering the sensor.

❶

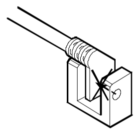


❷

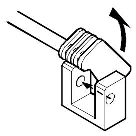


Exit sensor - This is a photo penetration sensor, combined with an actuator arm extending to the fuser board. The actuator is in the way back at the fuser outlet. The reflector at one end of the actuator is normally seated in-between the photo transmitter and sensor (❶). It is dressed away out of them when the paper in the fuser sensor pushed up the actuator (❷), allowing the light to hit the receptor and turning the sensor circuit on.

❶



❷



On detecting a paper jam, the engine controller stops printing action and shows the “Paper jam” message. After removing paper jam, the printer resumes printing when either the toner access door or the feed assembly is once opened and closed. If paper jammed past the exit sensor, the printer will not attempt to print the same page.

Paper coming from the paper cassette should pass the registration sensor in a predetermined period of time that begins with the feed clutch turned on (FDCL1).

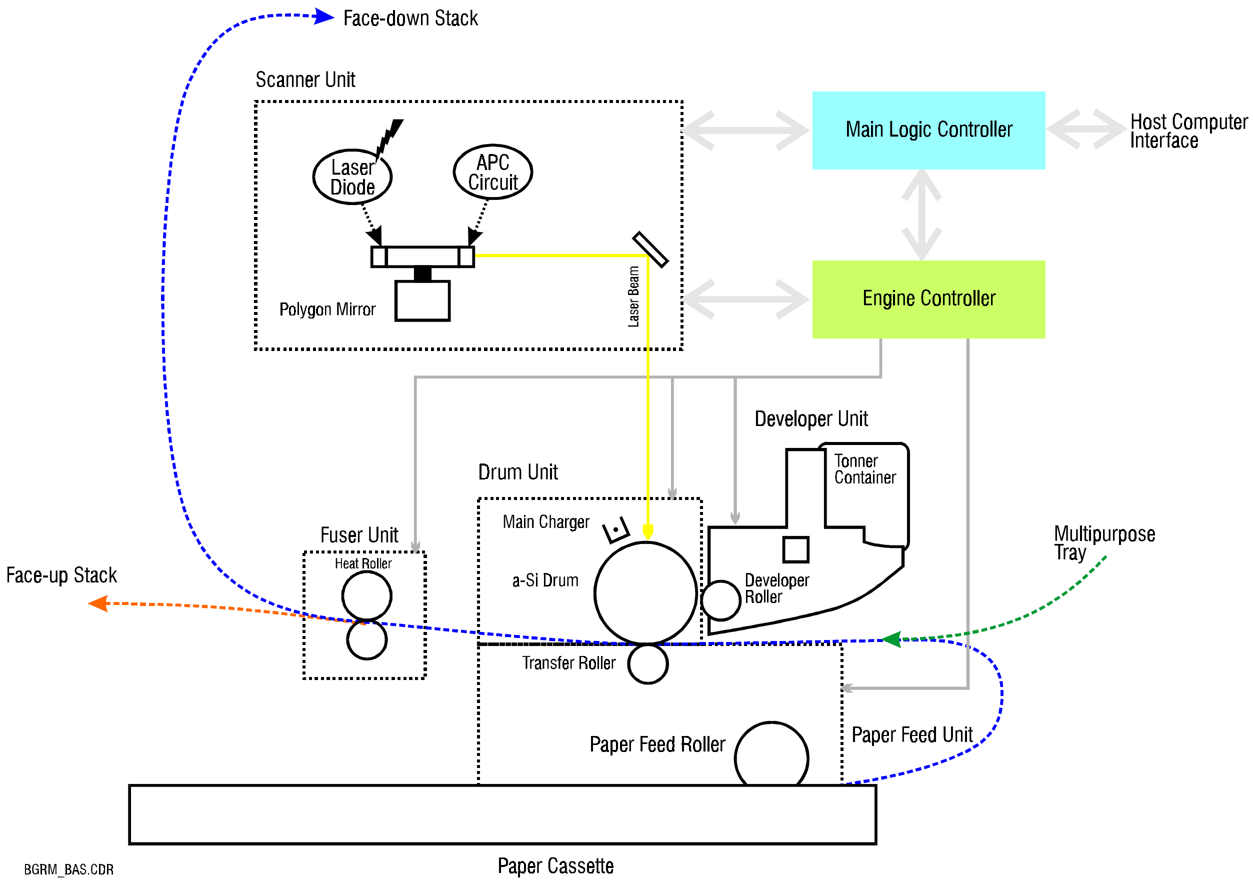
Basic engine functions

This section presents a general functional overview of the engine system of the printer. It was intended to provide a comprehensive knowledge on basic functions that the engine system performs during printing. The following printer functions are covered:

- ❒ Engine controller system
- ❒ Main logic controller system
- ❒ Paper feed system
- ❒ Power system

Basic sequence of operation

The following figure is a simplified block diagram of the printer engine system.



BASIC ENGINE SYSTEM DIAGRAM

Engine controller system

The engine controller provides control over all print engine activities. It drives laser, coordinates the electrophotography process with print data from the main logic controller. The engine system also manages information collected back from sensors, etc., so that a message is given in case of need for user attention.

The engine controller is responsible for the following systems, explained step by step in the following pages:

Flash memory

The engine controller uses a flash memory to store environmental parameters that does not require a battery backup. The flash memory is driven by +5 V power and designed to stand reading and writing for nominally 100,000 times.

High-voltage generator

The engine controller produces clocks (HVCLK1 and HVCLK2) and apply programmed divisor to generate high-voltage outputs for main charging. The clock oscillation can be toggled on and off by the engine controller CPU.

Laser scanner control

In order to activate the laser scanner, the engine controller does the following tasks:

- ❒ Forced laser activation timing
- ❒ Laser diode current limit
- ❒ Laser power control output
- ❒ Beam detection photo-sensor output
- ❒ Polygon motor activation
- ❒ Polygon motor readiness detection
- ❒ Polygon motor output frequency control (multi-step)

Polygon motor control

The output frequency signal to the polygon motor is generated by the engine gate array as it divides the engine system clock (16.9344 MHz).

The polygon motor has the following specifications (depending on model):

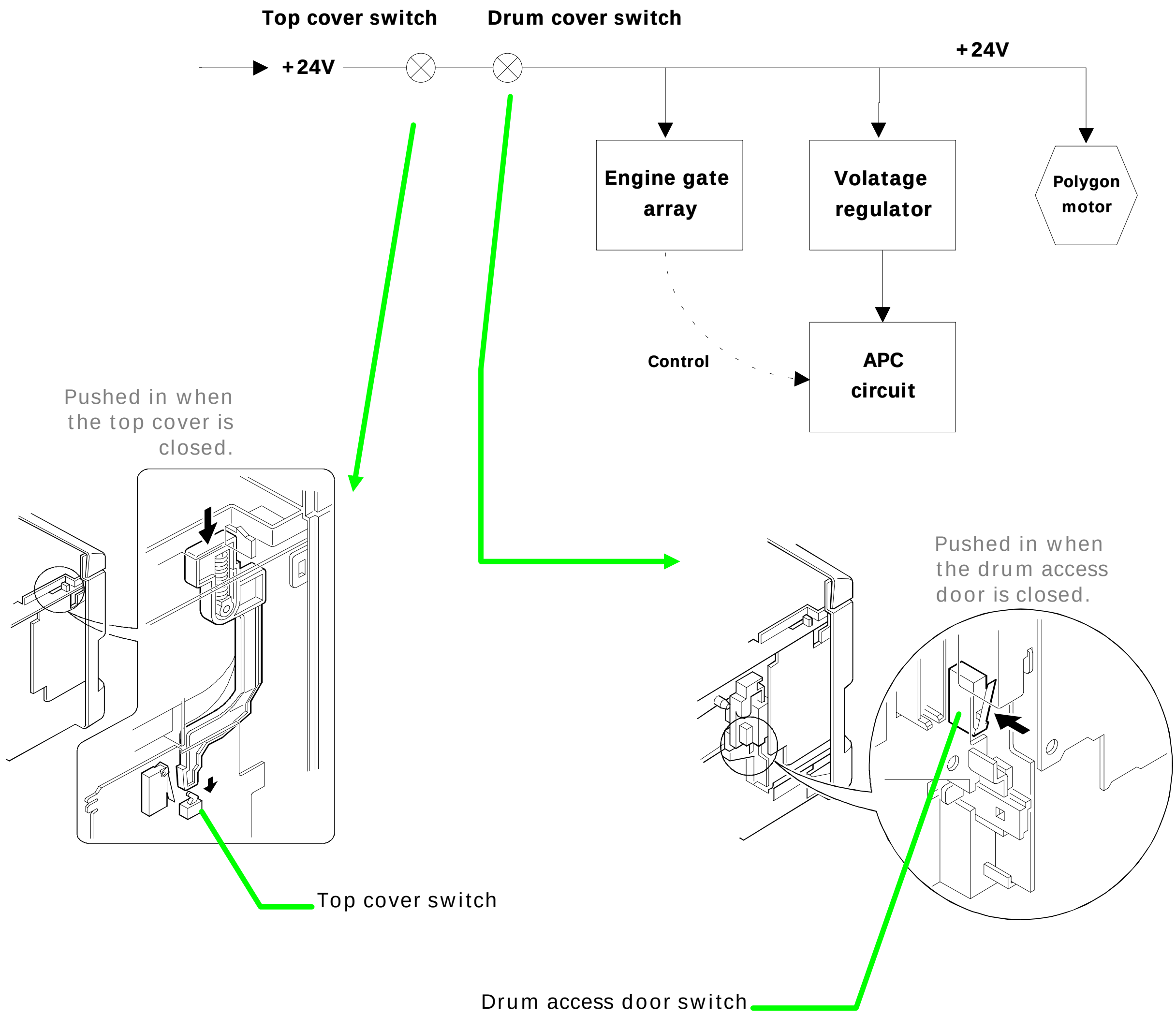
Model	Speed (rpm)	Input (Hz)	SCSEL signal
FS-1700	17008	1,696.15	0
FS-3700	27166	2,713.85	1

As the laser beam reaches the beam detector sensor, the sensor board generates the horizontal synchro signal (PD*). This signal makes the engine gate array consequently turn the video output signal (VDO*) and the APC signal (LONB*) high which respectively activate the laser light and the APC controller.

The engine CPV attempts to detect the horizontal synchronization signal so that the laser diode is normally triggered. If the horizontal synchronization output is not found after the laser driving current control (LENB*) is set low, the engine CPV recognizes it as the failure on the APC board and gives the E3 error.

Safety interlock

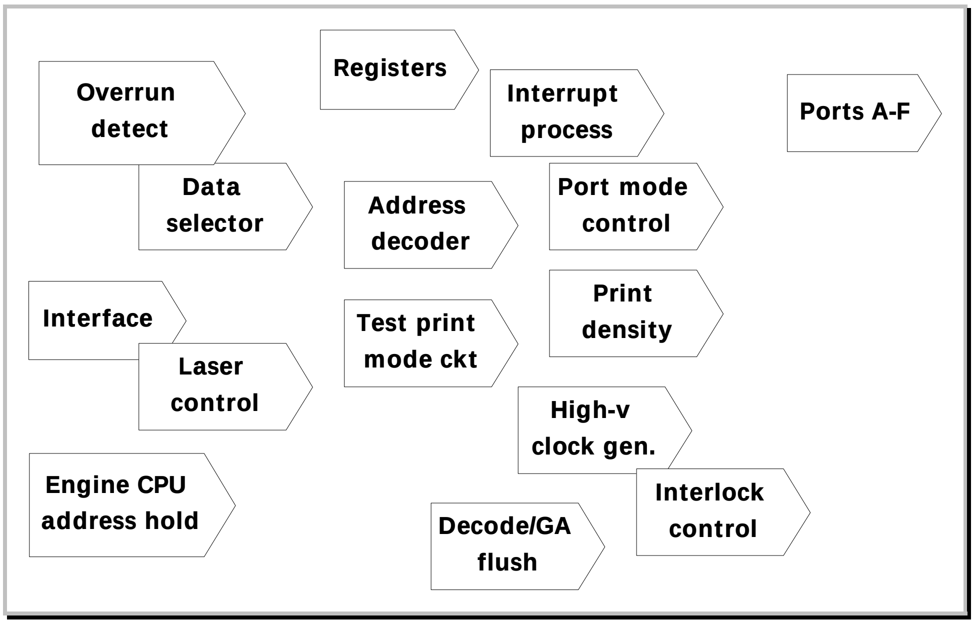
For safety purpose, micro switches are provided to sense that either the top (toner access) or side (drum access) cover is open. These switches, when the applicable cover is open, open and disconnect the DC power to the laser scanner as follows.



The engine gate array

The engine gate array is a supplementary device to the Engine CPU. The gate array is a 100-pin QFP type that has the internal blocks as figured below.

GATE ARRAY INTERNAL BLOCKS



Pin assignment

Pin assignment for the engine gate array is table on the following pages. The device in Remarks column means those which the signal is forwarded to.

ENGINE GATE ARRAY PINS

Pin No.	Ckt signal	GA signal	In/out	Description	Logic	Remarks
1	THVDR*	THVDR	OUT	Transfer charger control output, L: On	Neg.	HV board
2	REVB*	REVBN	OUT	Reverse bias control output, L: Rev. bias	Neg.	HV board
3	VDD	VDD		Power terminal (+5V)		
4	VSS	VSS		Power terminal (Ground)		
5	MHVDR*	MHVDR	OUT	Main charger control output, L: On	Neg.	HV board
6	BIAS*	BIAS	OUT	Bias control output, L: On	Neg.	HV board
7	ERASE*	ERASEN	OUT	Eraser control output, L: On	Neg.	Eraser
8	FDWSD*	PC3	OUT	Face-down solenoid	Neg.	FD solenoid
9	FOP	PC2	OUT	HS-20 gate diverter	Pos.	HS-20
10	JAMO*	PA1	IN	Fuser sensor input, H: No paper	Neg.	Fuser
11	EPAP*	PA0	IN	Envelope feeder paper sensing, H: Paper	Neg.	Env. feeder
12	EUNIT*	PB5	IN	Envelope feeder installation, L: Installed	Neg.	Env. feeder
13	EMOTR*	PD4	OUT	Envelope feeder motor control output, L: On	Neg.	Env. feeder
14	JAMR	PA2	IN	Registration sensor input, L: No paper	-	-
15	VSS	VSS		Power terminal (Ground)		
16	PAPER	PA4	IN	Cassette paper detection, L: Empty		
17	MFEED*	PA3	IN	Manual feed slot paper detection, L: Paper	Neg.	
18	BTBSEN*	PB1	IN	Waste toner reservoir detection, L: Installed	Neg.	
19	UNIT*	PB4	IN	HS-20 installation input, L: Installed	Neg.	HS-20
20	HSPAP*	PB3	IN	HS-20 paper sensing, L: Paper passing	Neg.	HS-20
21	COPN	PB2	IN	HS-20 status input, L: Open		HS-20
22	FUP	PC5	OUT	HS-20 gate diverter output, H: Face-up stack	Pos.	HS-20
23	FUPSD*	PC4	OUT	Face-up solenoid control	Neg.	Solenoid
24	MON*	PD1	OUT	HS-20 motor control output, L: On	Neg.	HS-20
25	VOLW*	PD0	OUT	HS-20 motor revolution output, L: On	Neg.	HS-20
26	TEST1	TEST1	IN	G/A test input 1, H: Test mode		Jumper
27	TEST0	TESTN	IN	G/A test mode, L: Test mode		Fixed high

Pin No.	Ckt signal	GA signal	In/out	Description	Logic	Remarks
28	VDD	VDD		Power terminal (+5 V)		
29	VSS	VSS		Power terminal (Ground)		
30	TESTCLK	TSTCLK	IN	G/A test clock		Fixed low
31	ILOCK	PB0	IN	Interlock input	Pos.	
32	ERRDY	PA5	IN	Eraser blow-out det., L: Blown		Eraser
33	THSBY	PD5	OUT	Fuser heater control, L: Print; H: Idle		Fuser
34	FCS*	GACE	OUT	Flash ROM chip select	Neg.	Flash ROM
35	FDCL2*	PC1	OUT	M-feed roller clutch control, L: On	Neg.	Clutch
36	FDCL1*	PC0	OUT	Paper pickup roller clutch control, L: On	Neg.	Clutch
37	REGCL	PD7	OUT	Regist. roller clutch, L: Off	Pos.	Clutch
38	SCCLK	SCCLK	OUT	Polygon motor clock	Pos.	Scanner
39	PDIN	PDIN	IN	Beam detect	Neg.	Scanner
40	VSS	VSS		Power terminal (Ground)		
41	LATCH	LATCH	OUT	Laser, LED density data latch	Pos.	Scanner
42	DSCLK	DSCLK	OUT	Laser, LED density data transfer clock	Pos.	Scanner
43	SDATA	SDATA	OUT	Laser, LED density data	Pos.	Scanner
44	VDO	VDOOUT	OUT	Video data	Neg.	Scanner
45	LENB	PC7	OUT	Laser diode drive control	Pos.	Scanner
46	LONB	LONB	OUT	APC control, L: Sampling	Neg.	Scanner
47	SCAN*	PC6	OUT	Polygon motor control, L: On	Neg.	Scanner
48	SCRDY*	PA7	IN	Polygon motor ready, L: Ready	Neg.	Scanner
49	MMOT*	PD3	OUT	Main motor control, L: On	Neg.	Main motor
50	FAN	PF0	OUT	Polygon motor ready, H: On	Pos.	Fan
51	X1	CKO0	OUT	Clock (Engine CPU)		
52	X2	CKO1	OUT	Clock (Engine CPU)		
53	VDD	VDD		Power terminal (+5 V)		
54	VSS	VSS		Power terminal (Ground terminal)		
55	CLCK*	CLCKN	IN	G/A test clock clear, L: Clearing		Fixed high
56	XTO	XTO	IN	Oscillator (16.9344 [MHz])		
57	XTI	XTI	IN	Oscillator (16.9344 [MHz])		
58	INTO	INTO	OUT	Interrupt	Pos.	
59	RES*	RSTN	IN	Power on reset	Neg.	
60	ASTB	ASTB	IN	Engine CPU ASTB		

Pin No.	Ckt signal	GA signal	In/out	Description	Logic	Remarks
61	WR*	WRN	IN	Engine CPU WR*	Neg.	
62	RD*	RDN	IN	Engine CPURD*	Neg.	
63	A16	A16	IN	Engine CPU address		
64	A15	EA15	IN	Engine CPU address		
65	VSS	VSS		Power terminal (Ground)		
66	A14	EA14	IN	Engine CPU address		
67	A13	EA13	IN	Engine CPU address		
68	A12	EA12	IN	Engine CPU address		
69	AD7	AD7	IN/OUT	Engine CPU address/data bus		
70	AD6	AD6	IN/OUT	Engine CPU address/data bus		
71	AD5	AD5	IN/OUT	Engine CPU address/data bus		
72	AD4	AD4	IN/OUT	Engine CPU address/data bus		
73	AD3	AD3	IN/OUT	Engine CPU address/data bus		
74	AD2	AD2	IN/OUT	Engine CPU address/data bus		
75	AD1	AD1	IN/OUT	Engine CPU address/data bus		
76	AD0	AD0	IN/OUT	Engine CPU address/data bus		
77	EA7	EA7	OUT	Engine CPU address		ROM address
78	VDD	VDD		Power terminal (+5 V)		
79	VSS	VSS		Power terminal (Ground)		
80	EA6	EA6	OUT	Engine CPU address		ROM address
81	EA5	EA5	OUT	Engine CPU address		ROM address
82	EA4	EA4	OUT	Engine CPU address		ROM address
83	EA3	EA3	OUT	Engine CPU address		ROM address
84	EA2	EA2	OUT	Engine CPU address		ROM address
85	EA1	EA1	OUT	Engine CPU address		ROM address
86	EA0	EA0	OUT	Engine CPU address		ROM address
87	RCSEN*	PD2	IN	Waste toner reservoir fullness	Neg.	
88	HEATT	PD6	OUT	Fuser heater control, H: On		Fuser
89	VDOIN	VDOIN	IN	Video data	Neg.	Scanner
90	VSS	VSS		Power terminal (Ground)		
91	PDOUT	PDOUT	OUT	Beam detect sensing	Neg.	Main log. board
92	S/C	SC	IN/OUT	Main I/F status command		Main I/F
93	SCLK	SCLK	IN	Main I/F status command clock		Main I/F

Pin No.	Ckt signal	GA signal	In/out	Description	Logic	Remarks
94	CBSY*	CBSYN	IN	Main commands in transmission	Neg.	Main I/F
95	SBSY*	SBSYN	OUT	Engine status in transmission	Neg.	Main I/F
96	CINH*	CINHN	OUT	Engine busy	Neg.	Main I/F
97	HVCLK1	HVCK1	OUT	HV unit clock 1		HV board
98	HVCLK2	HVCK2	OUT	HV unit clock 2		HV board
99	T/CSN	PA6	IN	Remaining toner sensing , H: Empty		HV board
100	HVOL	HVOL	OUT	Transfer bias (Thick/normal paper)		HV board

Power supply

The power supply contains the AC and DC power and distribution circuitry on the board. The high voltage generator is not included on this board but on the separate high-voltage board. The power supply circuit is diagrammed on the next page.

AC INPUT AND RECTIFIER: Either 120V or 230V AC power arriving at CN1 is fed to the AC line filter circuit (L1, L3, C1, C2, etc.) and rectified by diode array BD1 to DC power. Transistor Q1 performs switching of the DC power output for downverting it to the 24V and 5V AC voltage by means of transformer T1.

24V DC POWER LINE: The 24V AC at the secondary output of T1 is rectified by D1 and C12/C13 and delivered to connectors CN3 and CN4 for distribution. The 24V DC power is referred to as *VDD* or *VDDCOM* and is used by the following components in the engine system:

- Face-up/down stack solenoids
- Clutches (registration, feed, manual-feed)
- Fans
- High-voltage generator (board)
- Main motor and laser polygon motor
- Clutches, motors, solenoids within the option units

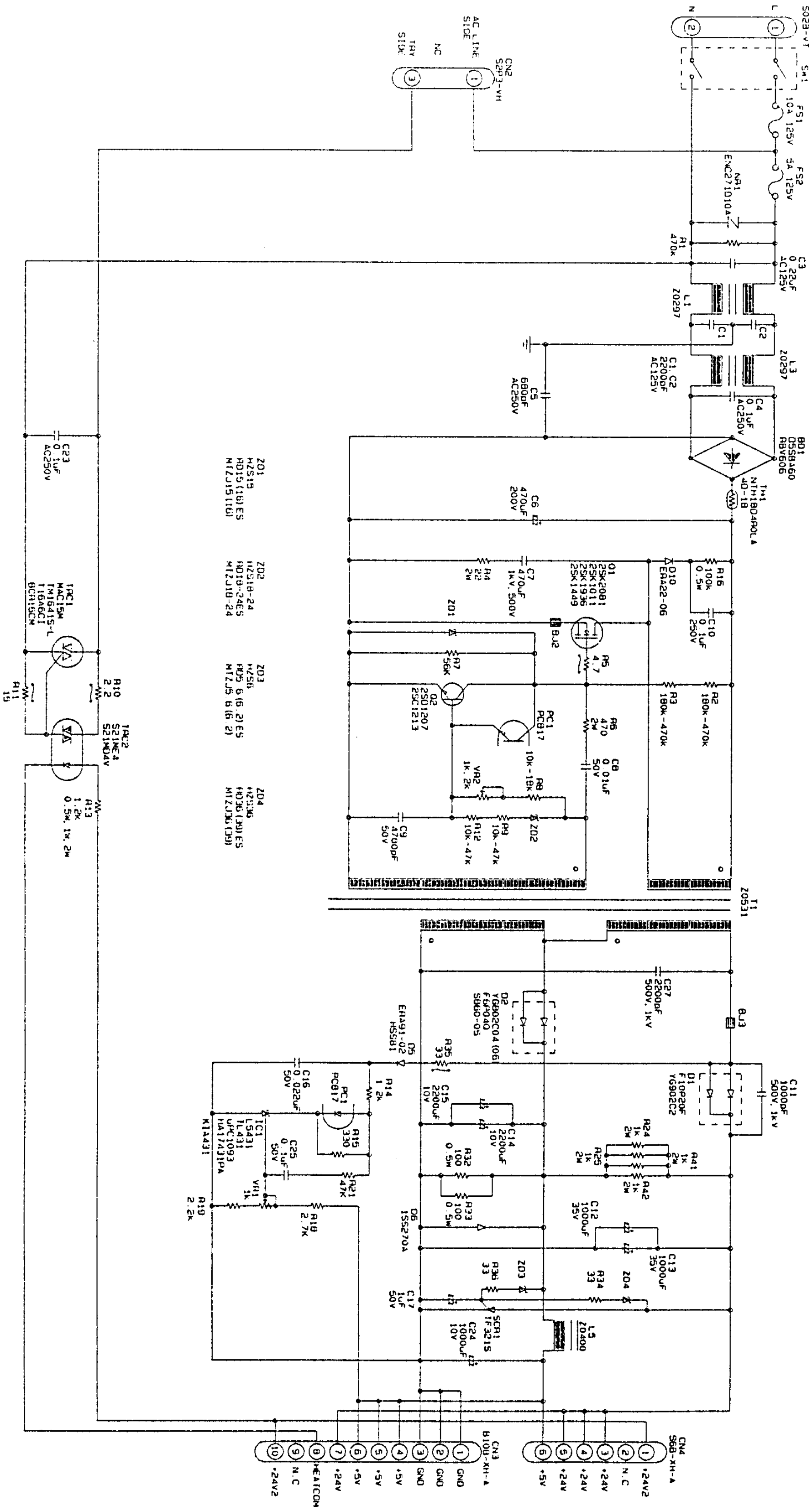
The 24V DC power is forcibly interrupted for safety whenever the printer top cover or the drum unit access door is opened. For details, see the Safety interlock section, page 4-4-30.

5V DC POWER LINE: The 5V AC at the secondary output of T1 is rectified by D2 and C14/15, etc., like as for the 24V DC power line. It also delivered to CN3 and CN4. The 5V DC power is referred to as *VCC* and is comprehensively used by the main controller, sensors, engine controller, etc.

POWER PROTECTION CIRCUIT: A fraction of the 5V DC output is wired to the diode segment of PC1, protection controller. In case of short-circuiting in the 5V DC load side , the diode triggers the transistor segment of PC1, activating Q2 and effectively shutting off the switching regulator (Q1) output.

FUSER HEATER POWER CONTROL: On the AC primary side, the fuser heater and thermo-cut device are wired in series across CN2. The heater is switched on and off as being controlled by TRIAC TRC1. TRC1 turns on the heater when HEATCOM (pin 8) at CN3 is energized by command from the engine controller.

POWER SUPPLY CIRCUIT (US/CANADA VERSION)



Logic controller system

The logic controller system does the following:

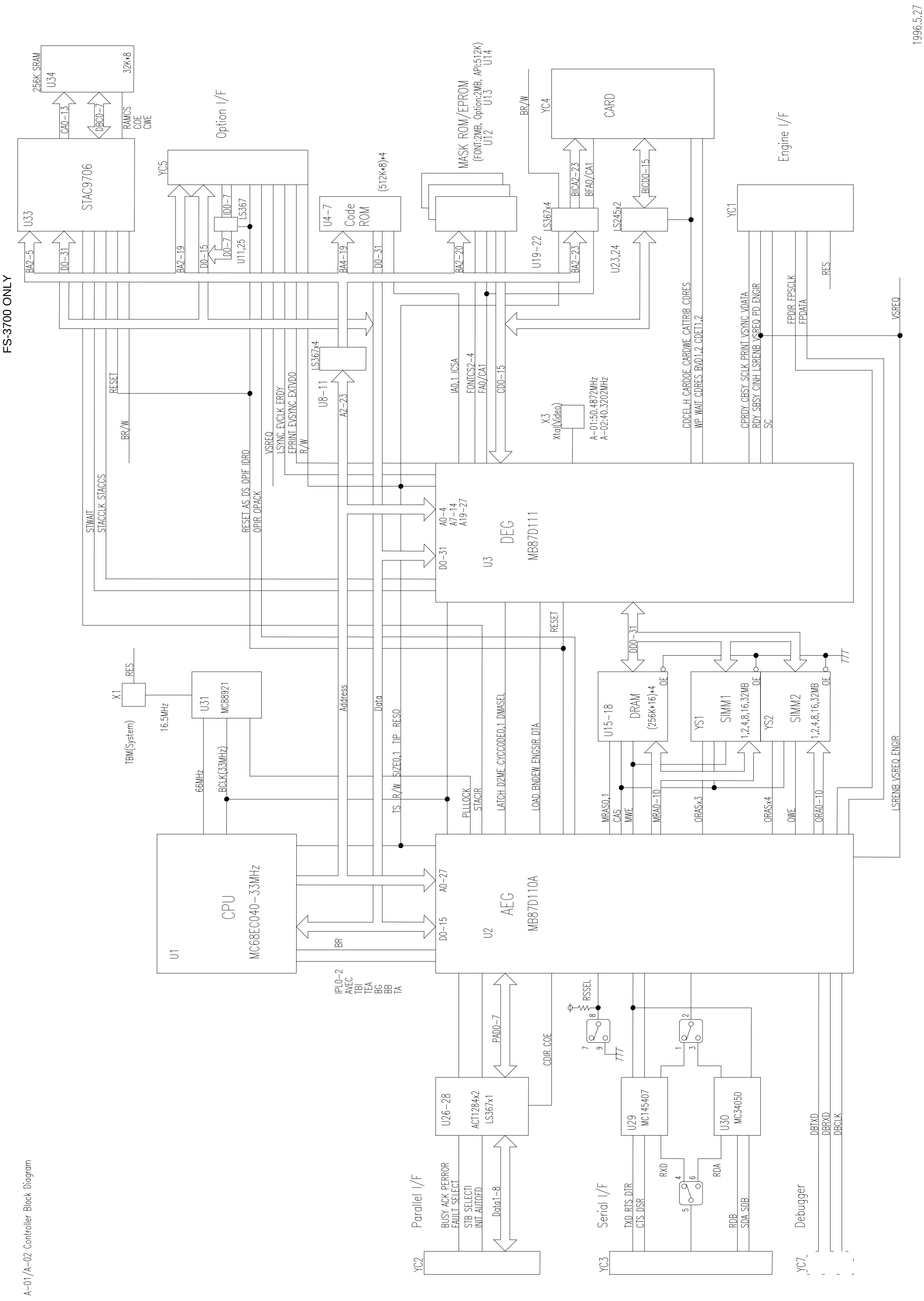
- ❒ Communicates with the host computer to receive data at one of the printer’s interface
- ❒ Analyzes and translates the print data to be the dot data in the raster memory
- ❒ Communicates with the engine system to discern radiness for printing
- ❒ Stores fonts and macro information

The main logic controller has specifications as shown in the following section. A simplified diagram is illustrated on page 4-40.

Logic controller specifications

Item		Specification
CPU		MC68EC040/33 MHz
System ROM size		2 MB (512 kB × 4)
RAM size	Standard	2 MB (512 kB × 4)
	Maximum	66 MB (Two PC SIMM slots)
Fonts	Resident	2 MB (2 MB × 1)
	Custom	2 MB [PK-1/2/4]
Application program interface		512 kB (512kB×1)
PC card		1 slot, JEIDA4.2/PCMCIA2.1
Interface	Parallel	High-speed bi-directional [IEEE 1284]
	Serial	RS-232C/422A (Jumper setting)
	Option	See Interface.
Engine communication		Serial interface
Front panel communication		Serial interface
Other features	Smoothing	KIR2 (Vector compensation method)
	Toner saver	EcoPrint [On/Off]
	Enlarge/reduction	Main scan/sub scan
	Video clock	50.4872 MHz (FS-1700)/40.3202 MHz (FS-3700)

CONTROLLER BLOCK DIAGRAM



Printing data processing

The printer communicates with the host computer for receiving the print data at one of the printer's interfaces and temporarily store them in the interface buffer. The main logic controller analyzes the data for translating them into the dot data according to the original print image. The resultant dot data are depicted in the raster memory (DRAM's).

While data processing is in course, on the other hand, the main logic controller CPU talks to the engine CPU via the engine interface, to discern the readiness of the printer's engine for printing.

If the engine is ready to start printing, the main conttroller issues print signal towards the engine controller which request the paper feed. In synchronization with the procerssion of the paper within the printer, U2 and U3 release video data in the raster memory. Thus the video data are transfered to the laser scanner together with the horizontal synchronization signal and the video clock.

On reception of the video data, the laser diode turns on and off to constitutes the print image over the drum. The image on the drum, referred to as the static latent image, is applied with toner, transferred onto the paper, and finally fused permanently on the paper by means of heat and pressure.

API ROM socket (U14)

Socket U14 which is empty at the shipment accepts an API (Application Program Interface) ROM. The API ROM should be a JEDEC-conforming EPROM, having the following features:

Socket No.	U14
Pins	40
Size	4 Mbits
Composition	256 k by 16 bits
Access speed	>120 ns

The number of clocks should be 19. Data are read in a 32-bit mode expanded using hardware.

The following table shows the pin-to-signal assignments for the ROM to be used.

API ROM socket pin assignment

Pin No.	Terminal description	Signal name	Pin No.	Terminal descritpion	Signal name
1	AVpp	VCC (fixed)	21	A0	FA0/CA1
2	CE*	GND (fixed)	22	A1	BA2
3	D15	CD15	23	A2	BA3
4	D14	CD14	24	A3	BA4
5	D13	CD13	25	A4	BA5
6	D12	CD12	26	A5	BA6
7	D11	CD11	27	A6	BA7
8	D10	CD10	28	A7	BA8
9	D9	CD9	29	A8	BA9
10	D8	CD8	30	GND	GND
11	GND	GND	31	A9	BA10
12	D7	CD7	32	A10	BA11
13	D6	CD6	33	A11	BA12
14	D5	CD5	34	A12	BA13
15	D4	CD4	35	A13	BA14
16	D3	CD3	36	A14	BA15
17	D2	CD2	37	A15	BA16
18	D1	CD1	38	A16	BA17
19	D0	CD0	39	A17	BA18
20	OE*	FONTCS4*	40	VCC	VCC

The asterisked (*) descriptions mean negative logic.

System ROMs (U4 to U7)

The system ROMs, also referred to as code ROM, contain informaton for controlling the controller CPU. These are served by the controller CPU MC68EC040 (33 MHz) which is a 18-pin CQFP. The system ROM chips incorporate the following features:

Number of ROMs	4
Socket Nos.	U4 to U7
Pins	32, DIP
Size	4 Mbits
Composition	512 k by 8 bits
Access speed	>120 ns

RAM (U15 to U18)

The RAM temporarily holds print data and font information transferred from the host buffers. The size of the RAM is expandable using comprehensive PC SIMMs. The standard RAM size is 2 MB for both FS-1700 and FS-3700. The maximum expanded RAM size is 66 MB.

Number of RAMs	4
Socket Nos.	U15 to U18
Pins	40, SOJ
Size	2 MB
Composition	512 kB (256 k by 16 bits) by 4
Access speed	80 ns

The expansion SIMM should incorporate the following features:

Number of SIMM sockets	2
Socket Nos.	YS1/YS2
Pins	72
Size	1/2/4/8/16/32 MB
Access speed	<80 ns

Memory card slot interface

The controller accepts a SRAM (or certain flash) type memory card that comforms to the PCMCIA (version 2.1) standards. The address and data busses for the card are bufferred using U19 to U22 and U23/24.

Option interface

The printer has an open socket for installing an optional interface card such as a serial interface card or an Ethernet network interface card. The interface has a video interface that can receive video data of either 300 dpi or 600 dpi. The transmission of video data must be in accordance with the video data transfer clock (EVCLK) that the DEG date array issues to accept the optional video interface. The video data transferred in synchoronization with the clock are temporarily stored in the line buffer (SRAM, contained in the DEG gate array), then passed to the engine controller.

The option interface has the following features:

Card connector	80 pins (See table below), AMP 176372-3 or equivalent
Applicable interface card	Kyocera IB-3

Option interface pin assignment

Pin assignment of the option interface connector is tabled on the following page.Option interface pin assignment

Pin No.	Terminal	Signal	Pin No.	Terminal	Signal
1	+5V	VCC	16	A16	BA17
2	+5V	VCC	17	A15	BA16
3	+5V	VCC	18	A14	BA15
4	+5V	VCC	19	A13	BA14
5	+5V	VCC	2O	A12	BA13
6	+5V	VCC	21	A11	BA12
7	+12V	NC (Not used)	22	A10	BA11
8	+12V	NC (Not used)	23	A9	BA10
9	-12V	NC (Not used)	24	A8	BA9
10	-12V	NC (Not used)	25	A7	BA8
11	NC	NC (Reserved)	26	A6	BA7
12	NC	NC (Reserved)	27	A5	BA6
13	NC	NC (Reserved)	28	A4	BA5
14	A18	BA19	29	A3	BA4
15	A17	BA18	30	A2	BA3

Option interface pin assignment - Continued

Pin No.	Terminal	Signal	Pin No.	Terminal	Signal
31	A1	BA2	56	D10	D10
32	NC	NC (Reserved)	57	D9	D9
33	NC	NC (Reserved)	58	D8	D8
34	OPIF*	OPIF*	59	D7	D7
35	OPRDY*	(D7)	60	D6	D6
36	ID6	(D6)	61	D5	D5
37	ID5	(D5)	62	D4	D4
38	ID4	(D4)	63	D3	D3
39	ID3	(D3)	64	D2	D2
40	ID2	(D2)	65	D1	D1
41	ID1	(D1)	66	D0	D0
42	ID0	(D0)	67	VDO%	EXTVDO
43	NC	NC (Reserved)	68	LSYNC*	LSYNC*
44	NC	NC (Reserved)	69	VCLK	EVCLK
45	AS*	AS*	70	PRINT*%	EPRINT*
46	DS*	DS*	71	VSREQ*	VSREQ*
47	OPDAC*	OPACK*	72	VSYNC*%	EVSYNC*
48	RW	R/W	73	RDY*%	ERDY*
49	OPIR*	OPIR*	74	NC	NC (Reserved)
50	RESET*	RESET*	75	GND	GND
51	D15	D15	76	GND	GND
52	D14	D14˘	77	GND	GND
53	D13	D13	78	GND	GND
54	D12	D12	79	GND	GND
55	D11	D11	80	GND	GND

Parallel interface

The printers have a port for the parappel interface that is compatible with the gate array µPD65650-268-3BA used with the current line-up of the Plus series printers. The parallel interface supports the protocols defined by the IEEE 1284 standards. To gain conformity to these standards, the printer supports the ECP and nibble modes.

Details on the signals on the parallel interface are described in the appropriate appendix in this manual.

Serial interface

The printer incorporates a port for the serial interface. The serial interface controller is included within the gate array and supports both the RS-232C and RS-422A protocols. Since the RS-232C support is designed to be compatible with SNMP (Simple Network Management Protocol), CTS and DSR signals are included. Switching to either mode is toggled by changing a jumper wire arrangement on the controller board. A 25-pin D-sub connector is used for the serial port. The RS-422A's extra signal lines are assigned to some of the vacant RS-232C terminals. (See *Appendix A* for the interface later in this manual for details.)

The serial interface has the following features:

Connector type	25-pin, D-sub
Baud rates/sec.	300/600/1200/2400/4800/9600/19200/38400/57600/115200
Protocol	RS-232C/RS-422A (switchable)

The serial interface connector also incorporates the debugging signal outputs as explained below.

Debugging outputs

Connector YC7 provides the following signals for debugging

Pin No.	Signal	Direction of flow	Definition
2	DBTXD	Printer to host	Transmission data
3	DBRXD	Host to printer	Reception data
4	DBCLK	Host to printer	Transfer clock

Engine interface

The interface to the engine system is based on the serial interface, not the parallel interface that was used with the previous line-up of the Ecosys printers. The serial-to-parallel conversion is executed on a hardware basis.

The engine board is detachable from the printer at its interface connector. The engine interface connector has the following pin assisngments:

Engine interface connector assignment

Pin No.	Terminal	Signal	Pin No.	Terminal	Signal
A1	GND	GND	B1	GND	GND
A2	VCC	VCC	B2	VCC	VCC
A3	VCC	VCC	B3	VCC	VCC
A4	RPORT	EGIR*	B4	D/CZ	NC (Reserved)
A5	VSREQZ	VSREQ*	B5	SBSYZ	SBSY*
A6	CBSYZ	CBSY*	B6	SCLK	SCLK
A7	S/CZ	SC	B7	CPRDY	CPRDY
A8	RDYZ	RDY*	B8	CINHZ	CINH*
A9	RXD	NC (Reserved)	B9	VCC	VCC
A10	TXD	NC (Reserved)	B10	FRM/BYZ	NC (Reserved)
A11	FPDATA	FPDAT	B11	VSYNCZ	VSYNC*
A12	PRINTZ	PRINT*	B12	PDZ	PDOUT*
A13	RESETZ	RST*	B13	FPSCLK	FPCK
A14	LEN	OUTPE*	B14	VDO	VIDEO
A15	GND	GND	B15	FPDRC	FPDR
A16	GND	GND	B16	GND	GND

* Means negative logic.

Signals used for the engine interface

The following signals are used for the engine interface communication. Figure on next page shows a simplified function diagram of the engine interface and the signals.

Signal	Meaning	Active	Definition
SBSYN	Status-BuSY-sigNal	Low	Determines which direction for the engine system to transfer the status data. If SBSYN is true, the controller is unable to transfer the command data towards the engine system. The controller can read in the status data transferred from the engine system by forwading SCLK to the engine.
CBSYN	Command-BuSY-sigNal	Low	Determines which direction for the controller system to transfer the command data. If CBSYN is true, the controller can transfer the command data towards the engine system by forwading SCLK to the engine system
S/C	Status-data/Command-data	-	This is a bi-directional serial datum containing the status data and command data as well as attributive information. The transfer data commences with LSB, then to MSB.
SCLK	Serial CLocK	-	The width of the clock pulse is approx. 1µsec (960 ns). SCLK is the clock delivered by the controller and used to synchronize the status data and command data with each other.
CINHN	Command INHibit sigNal	Low	This signal inhibits the signal transmission. If CINHN is low, the controller is not allowed to ready the transmission data. This inhibit is cancelled when the engine controller reads in the reception data.

Engine interface signals