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3.1. Printing Data Processing

This section describes the brief discussion on how the video data are generated and used to drive the LED head and how a printing job completes. It starts with the introduction of data on the printer's interface(s) and concludes the LED head driven to write image on the drum.

Discussion on the electrophotography process, such as development and transferring image, including paper transportation, are given in details in the Electrophotography section and this is not repeated here.

1. Printing data arrive at one of the printer's interface ports when the host computer starts sending through its output port (and through the network). These data are temporarily stored in the printer's interface buffers corresponding to each interface. The most printing data normally include software commands which instruct the printer to supplementary jobs needed to accomplish printing such as line-feeding, page-breaking, changing fonts, etc.
2. The main logic controller analyzes the data in sequence, translates them into dots according to the original image, and depicts the image resultant of the dot data in the raster memory (DRAM's). Operations additionally required during processing data is accomplished by U105 which supplements the main logic CPU.
3. While data processing is in course, on the other hand, the main logic CPU talks to the engine CPU, via the common RAM and the engine interface (U3), to discern the readiness of the printer's engine for printing.
4. If the main logic controller determines that the engine is ready to start, it triggers the engine CPU and, according to the vertical synchronization signal, requests to feed the paper.
5. In synchronization with the succession of the paper, U4 releases video data in sequence. The video data are then applied to the LED head driver together with the horizontal synchronization signal and the video clock.
6. On reception of video data, the LED head driver switches the LED segments of the head on and off and constitutes the image over the drum. The image on the drum, referred to as static latent image, is applied with toner, transferred onto the paper, and finally fused permanently on the paper by means of heat and pressure.

3.2. Data Processing System Overview

This section contains a detailed discussion on the operating features of the printer's main logic controller circuitry.

Figure 3.1. illustrates the component layout of the main logic controller board, KP-410.

Figure 3.2. shows the functional block diagram of the controller circuitry.

The printer uses a 32-bit microprocessor, 68LC040, as the main controller CPU. The function of each segment in the controller circuitry will be discussed in the following sections. In the following descriptions, the number with the letter *U* prefixed means the symbol number of the chip or device, which also appear on the printed circuit board.

3.2.1. Controller CPU: 68LC040 (U1)

The 68LC040, operating at 25MHz clock, takes care of the timings among the data and commands coming through the interfaces to the gate arrays [which are the main functionality of the controller system], dynamic RAMs, program RAMs, mask ROMs, etc.

3.2.2. System ROMs (U1/U2)

The system ROMs includes the control programs for driving CPU in the repeated routines during printing. Physical allocation is 512 kB for each of U6 through U9.

3.2.3. Font ROMs (U18—U21)

ROMs U18 and U19 have memory region of as large as 4MB in total in which resident fonts are contained. The fonts are 79 bitmap and 45 scalable, PCL5E compatible fonts. The open socket U20 is for an optional installation of the KPDL (PostScript) upgrade ROM. U21 is for accommodation of an additional installation of customized ROM. The EPROM should be of 4Mbit (by 16).

3.2.4. Dynamic RAMs (U10—U13)

The DRAM area is referred to as raster memory or video RAM for page printers. Four 512-kB (256 k by 16 bits) DRAMs are used to constitute the memory area of 2 Mbytes. This area is expandable using expansion SIMMs. Generation of the data to be printed is done in this area.

Figure 3.1. Main Controller Board Layout

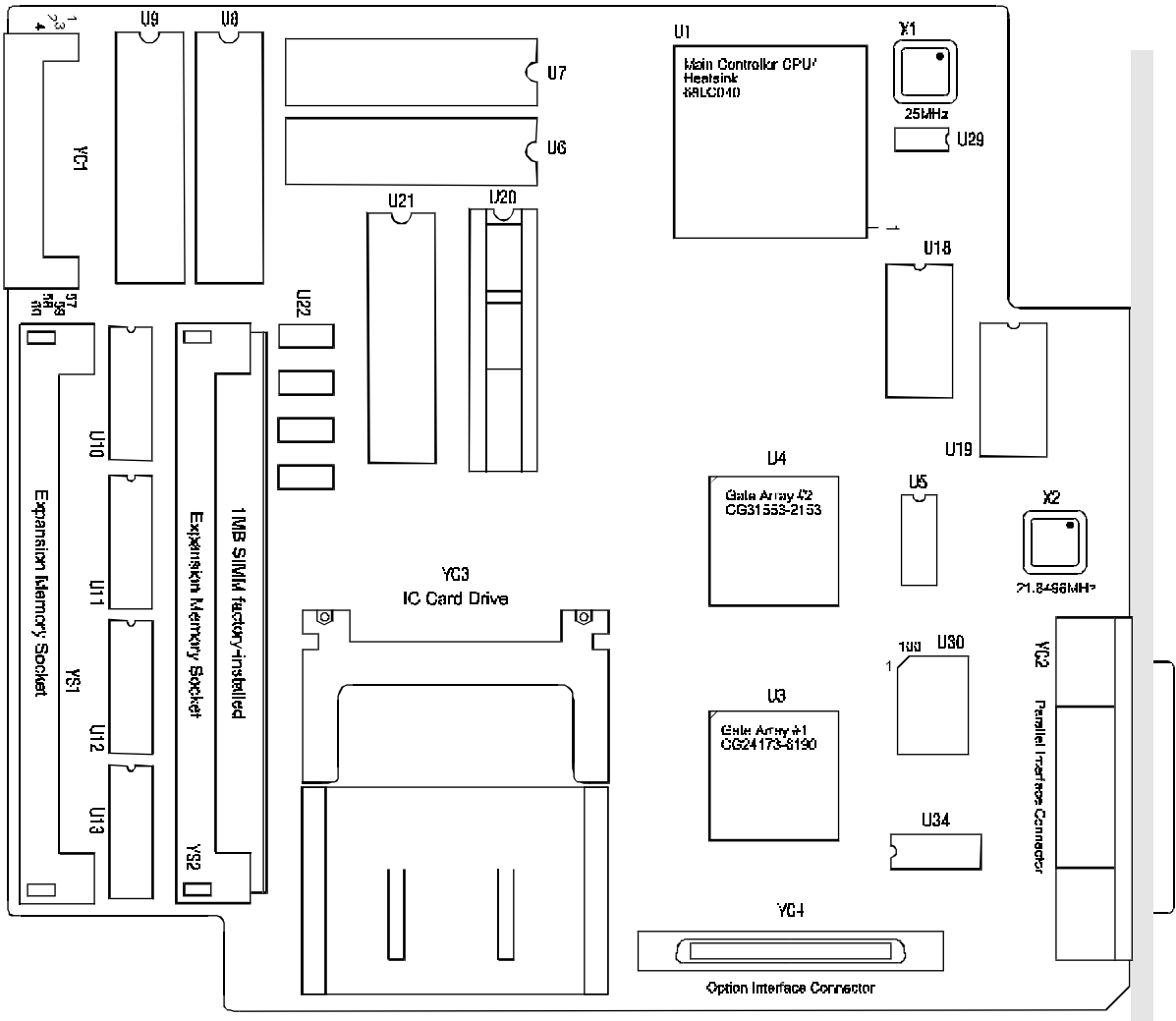
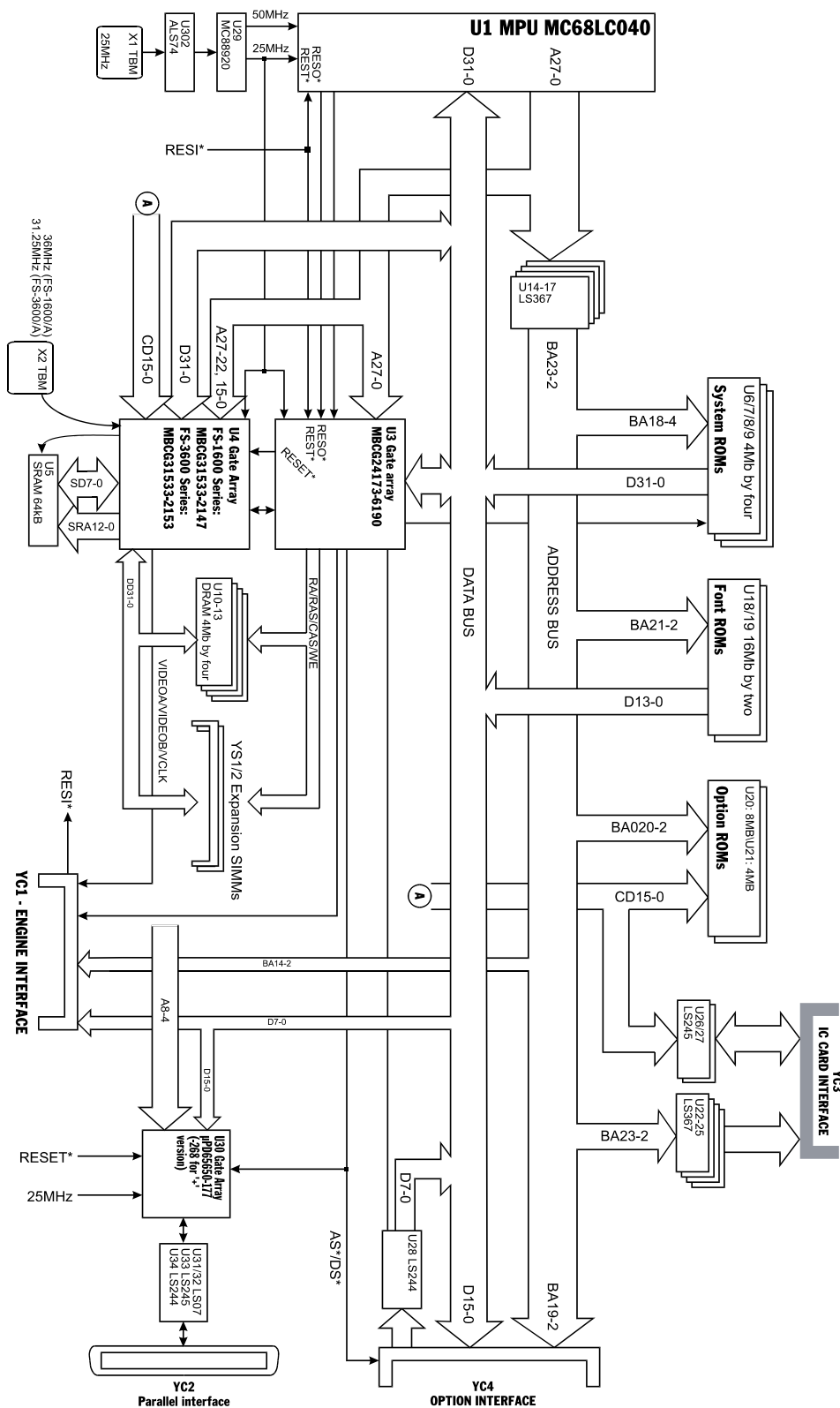


Figure 3.2. Main Logic Controller Block Diagram



3.2.5. Gate Array MBCG24173-6190 (U3)

This gate array implements the following functionality:

Address decoding: Generates the select signal for each I/O segment by decoding the addresses delivered from CPU, 68LC040.

Input control: Forwards a report to CPU 68LC040 with the level of interrupt.

Timer control: Generates the timer for use with CPU, 68LC040; and for refreshing DRAM's.

DRAM control: Provides an arbitration of whether DRAM's are used for the CPU 68LC040 system for transferring video data, or for refreshing themselves.

Front operator panel control: Takes responsibility for the LCD and LED indicators on the operator panel. Also reads the commands for the keyswitch manipulation.

Engine interface: Controls the dual port RAMs that are used for communication with the engine CPU.

3.2.6. Gate Array MBCG31553-2147(FS-1600)/2153(FS-3600) (U4)

This gate array implements the following functionality:

SRAM control: Takes responsibility for the battery-backed up SRAM for storing printer parameters while printer power is off.

Pattern data processing: Computes data used for implementation of the required print model.

Image refinement (KIR): Performs data process for image smoothing using KIR.

IC card control: Takes responsibility for IC cards in the battery condition, write protect status, and existence of an IC card in the slot.

Data bus control: Provides an arbitration of functionalities of CPU data buses, DRAM data bus, and IC card data bus.

Video data output control: Converts video data written in DRAM's into two parallel data, and then forwards them to the LED head.

3.2.7. Gate array μ PD65650-177/268 ('+' version) (U30)

This gate array performs management on the parallel interface. Both high-speed mode and bi-directional mode are implemented through the process of this gate array.

3.2.8. Clock driver (U29)

The clock driver generates both the 25MHz and 50MHz clock frequencies from a 25MHz time-base module. These clocks are fed to the controller CPU, 68LC040, after its phase has been optimized.

3.2.9. SRAM (U5)

This SRAM is used for buffering video data during the KIR process or 600-dpi printing.