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B

APPENDIX: PARALLEL INTERFACE

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B.1. Parallel Interface

This section describes the protocols and signals that the printer uses to communicate with the host computer through the parallel interface. The parallel interface supports several communication modes of data tranmission in conformity with IEEE (Institute of Electrical and Electronics Engineers) 1284 standards to *talk* and *listen* to the host computer.

This section also describes pin assignments, signal functions, timings, connector specifications, and voltage levels. Section B.2. provides similar information for the gate array used for the parallel interface.

B.1.1. Parallel interface communication modes

The printer features the fast and bi-directional data transmission on the parallel interface. The parallel interface mode can be manipulated using the printer's control panel or FRPO O0 parameter as follows (see the printer's *User's Manual* for details):

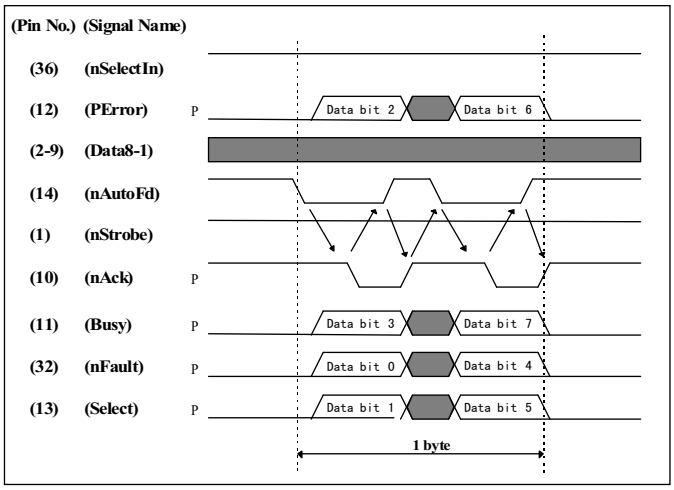
Note: Use the parallel printer cable that complies with the IEEE1284 standards.

Auto (O0=70 [Default])

The printer must be set to *Auto* mode in order to work in the bi-directional modes. It automatically changes its communication mode to the one of the following bi-directional modes depending on the one the host computer is currently using. The following IEEE modes are supported:

Nibble mode: This is the reverse direction only mode. Four status lines (see Figure B.1. below) on the parallel interface are used to forward the printer information (manufacturer, model, etc.) to the host computer. The Plug-and-Play printer installation feature under Windows 95 is achieved by this mode.

Figure B.1. Nibble Mode Signals/Timings



ECP mode: This is the fast, forward and reverse direction mode. The host computer must be installed with a hardware circuit specifically supporting the ECP mode. Eight data lines are used as shown in Figure B.2.

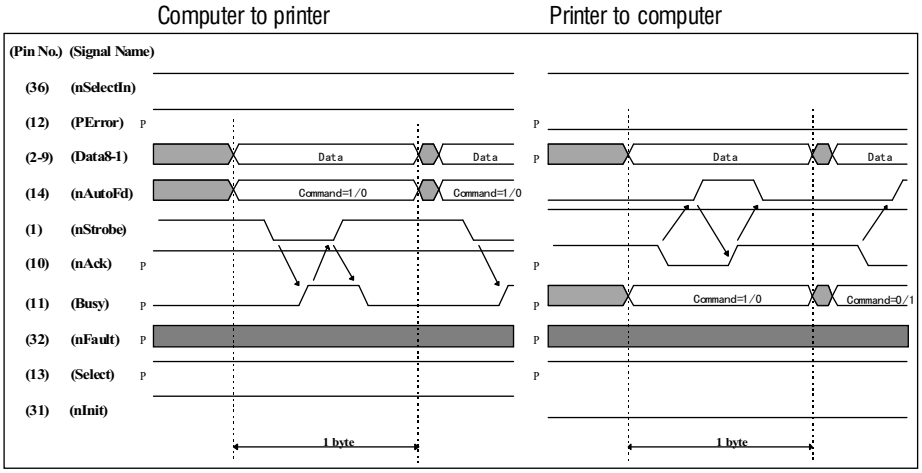


Figure B.2. ECP Mode Signals/Timings

Normal (00=0)

The printer uses the communication method according to the normal definitions of the Centronics interface.

High-speed (00=1)

This mode is also a non-IEEE mode but ensures faster data transmission between the printer and the host computer.

B.1.2. Interface Signals

The pins of the parallel interface connector carry the signals listed in Table B.1. Asterisks in the table indicate signals that are *active low*. The table also indicates whether each signal is incoming or outgoing with respect to the printer.

Table B.1 Parallel Connector Pin Assignments

Pin	In/out [ECP]	Description	
		Normal/Hi-speed	Auto
1	In [Out]	Strobe*	nStrobe
2	In [Out]	Data 0	Data 1
3	In [Out]	Data 1	Data 2
4	In [Out]	Data 2	Data 3
5	In [Out]	Data 3	Data 4
6	In [Out]	Data 4	Data 5
7	In [Out]	Data 5	Data 6
8	In [Out]	Data 6	Data 7
9	In [Out]	Data 7	Data 8
10	Out	Acknowledge*	nAck
11	Out	Busy	
12	Out	Paper Empty	PError
13	Out	On-Line (Select)	Select
14	In	Auto-feed	nAutoFd
15	—	Not connected	
16	—	0V DC	
17	—	Chassis GND	
18	—	+5V DC	
19	—	Ground return	
20	—	Ground return	
21	—	Ground return	
22	—	Ground return	
23	—	Ground return	
24	—	Ground return	
25	—	Ground return	
26	—	Ground return	
27	—	Ground return	
28	—	Ground return	
29	—	Ground return	
30	—	Ground return	
31	In	Ignored	
32	Out	Error*, returns error status if FRPO O2=2	nFault
33	—	—	
34	—	Not connected	
35	Out	Power Ready	
36	In	Select In	nSelectIn

Detailed descriptions of the signals follow. Those in [] are in IEEE modes.

Strobe* [nStrobe] (Pin 1)

A negative-going Strobe* pulse causes the printer to read and latch the data on the Data 0 [1] to Data 7 [8] signal lines.

Data 0 [1] to Data 7 [8] (Pins 2 to 9)

These eight signals form the data byte sent from the host computer to the printer. Data 7 [8] is the most significant bit.

Acknowledge* [nAck] (Pin 10)

This negative-going pulse acknowledges the previous character received by the printer. Acknowledge* pulses are sent only when Busy is low.

Busy (Pin 11)

This signal is high when the printer is busy and low when it is able to accept more data. Every high-to-low transition is followed by an Acknowledge* pulse.

Paper Empty [PError] (Pin 12)

This signal goes high when the printer runs out of paper.

On-Line [Select] (Pin 13)

This signal is high when the printer is on-line and low when the printer is off -line. It goes low when the upper unit is raised, or when the ONLINE key is pressed to set the printer off-line.

Note: The Paper Empty and On-Line signals are not used unless enabled by the FRPO command (O2 parameter).

Auto-Feed (Pin 14)

This signal is used in the Epson version of the Centronics interface to receive a carriage return. In high-speed mode, it is used as an interrupt.

+5V DC (pin 18)

This line is connected to the printer's +5V DC line (+5V ± 0.5V, 250 mA maximum, fused).

Prime (Pin 31)

This signal is used in the standard Centronics interface to enable the computer to reset the printer. It is ignored by the printer.

Error* [nFault] (Pin 32)

When the high-speed parallel line control is on (FRPO O2=2), this line returns error status.

Auxiliary output 1 (Pin 33)

This signal line is not used.

Power Ready (Pin 35)

This signal is high when the printer's power is on.

Select In [nSelectIn] (Pin 36)

This signal is used in some versions of the Centronics interface to enable the computer to force the printer on-line. In high-speed mode, it is used as an interrupt.

B.1.3. Parallel interface G/A pin assignment

μ PD65650-268 is the gate array for the parallel interface. Pin assignment is as listed below.

Table B.2. Gate array pin assignment

Pin #	Signal	In/Out	Level CMOS/TTL	IOL (mA)	Description
1	GND				Ground
2	VDD				VDD
3	RWN	In	TTL		Read/write input
4	INTOUT	Out	CMOS	4.5	Interrupt output (Edge/level sel.)
5	RESETN	In	TTL Sch.		Reset input
6	GND				Ground (Aux.)
7	XT2	Out			Oscillator terminal
8	XT1	In			Oscillator terminal
9	GND				Ground (Aux.)
10	XTCLKOUT	Out	CMOS	4.5	Oscillator clock output
11	CLKIN	In	TTL		External clock input
12	GND				Ground (Aux.)
13	FOUT	Out	CMOS	4.5	Clock divisor (half) output
14	2FIN	In	TTL		Clock divisor (half) input
15	FRESETN	In	TTL Sch.		Clock divisor reset input
16	TESTOUT	Out	CMOS	4.5	Test output
17	GND				Ground (Aux.)
18	VDD				VDD (Aux.)
19	D15	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
20	D14	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
21	GND				Ground (Aux.)
22	D13	In/Out	TTL-IN/CMOS-OUT	9	Data bus input
23	D12	In/Out	TTL-IN/CMOS-OUT	9	Data bus input
24	GND				Ground (Aux.)
25	D11	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
26	D10	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output

Pin #	Signal	In/Out	Level CMOS/TTL	IOL (mA)	Description
27	D9	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
28	GND				Ground
29	VDD				VDD
30	D8	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
31	D7	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
32	GND				Ground (Aux.)
33	D6	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
34	D5	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
35	GND				Ground (Aux.)
36	VDD				VDD (Aux.)
37	D4	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
38	D3	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
39	D2	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
40	GND				Ground
41	D1	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
42	D0	In/Out	TTL-IN/CMOS-OUT	9	Data bus in/output
43	GND				Ground (Aux.)
44	VDD				VDD
45	CNT1OUT	Out	CMOS	4.5	CNT1 output
46	CNT2OUT	Out	CMOS	4.5	CNT2 output
47	CNT3OUT	Out	CMOS	4.5	CNT3 output
48	TESTI	In	TTL Schm.		Gate array TEST-IN
49	SELIO	Out	CMOS	4.5	External SELLI output
50	PRDYO	Out	CMOS	4.5	External PRDY0 output
51	LDO	Out	CMOS	4.5	LD output (FMR)
52	VDD				VDD
53	GND				Ground
54	RMRO	Out	CMOS	4.5	External RMR output
55	ASJAMO	Out	CMOS	4.5	External ASJAM output
56	CANO	Out	CMOS	4.5	External CAN output
57	SELO	Out	CMOS	4.5	External SEL output
58	ASFONO	Out	CMOS	4.5	External ASFON output
59	ARARMO	Out	CMOS	4.5	External ARARM output
60	PEO	Out	CMOS	4.5	External PE output
61	BUSYOUT	Out	CMOS	4.5	BUSY output
62	ACKOUT1	Out	CMOS	4.5	ACK output (1)
63	ACKOUT2	Out	CMOS	4.5	ACK output (2)
64	STBOUT	Out	CMOS	4.5	STROBE rev. output
65	EXIN	In	TTL Schm.		Aux. input (interruptable)
66	INT21	In	TTL Schm.		Parallel port INT2 input
67	SELII	In	TTL Schm.		Parallel port SELI [nSelectIn]
68	EXPRMI	In	TTL Schm.		EXPRM input (FMR, pin 34)
69	HSTII	In	TTL Schm.		Parallel port HSTI input
70	CANI	In	TTL Schm.		Parallel port CAN [nAutoFd]
71	ASJAMI	In	TTL Schm.		Parallel port ASJAM input
72	ASFONI	In	TTL Schm.		Parallel port ASFON [nInit]
73	STBIN1	In	TTL Schm.		Parallel port STB (1) [nStrobe]

Pin #	Signal	In/Out	Level CMOS/TTL	IOL (mA)	Description
74	STBIN2	In	CMOS Schm.		Parallel port STB (2) [nStrobe]
75	GND				Ground (Aux.)
76	STBGET	Out	CMOS	4.5	STB-GET output (monitor)
77	CDIR	Out	CMOS	4.5	External bi-d buffer switch output
78	COEN	Out	CMOS	4.5	External bi-d buffer OE output
79	VDD				VDD
80	GND				Ground
81	CDATA7	In/Out	TTL Schm IN/CMOS 3-state OUT	18	Parallel port data in/output
82	CDATA6	In/Out	TTL Schm IN/CMOS 3-state OUT	18	Parallel port data in/output
83	CDATA5	In/Out	TTL Schm IN/CMOS 3-state OUT	18	Parallel port data in/output
84	CDATA4	In/Out	TTL Schm IN/CMOS 3-state OUT	18	Parallel port data in/output
85	GND				Ground (Aux.)
86	CDATA3	In/Out	TTL Schm IN/CMOS 3-state OUT	18	Parallel port data in/output
87	CDATA2	In/Out	TTL Schm IN/CMOS 3-state OUT	18	Parallel port data in/output
88	CDATA1	In/Out	TTL Schm IN/CMOS 3-state OUT	18	Parallel port data in/output
89	CDATA0	In/Out	TTL Schm IN/CMOS 3-state OUT	18	Parallel port data in/output
90	GND				Ground (Aux.)
91	VDD				VDD (Aux.)
92	A8	In	TTL		Address input
93	A7	In	TTL		Address input
94	A6	In	TTL		Address input
95	A5	In	TTL		Address input
96	A4	In	TTL		Address input
97	CSN	In	TTL		CS input
98	ASN	In	TTL		AS input
99	DSN	In	TTL		DS input
100	DACK	Out	CMOS	4.5	DACK output