3 CONTROLLER OVERVIEW

CONTENTS

This page is left blank intentionally.

3.1. Print Data Processing

This section describes a brief discussion on how video data are generated and used for driving the LED head, and how a printing job completes. It starts with the introduction of data on the printer's interface(s) and concludes the LED head driven to write an image on the drum.

Discussion on the electrophotography process, such as development and transferring image, including paper transportation, are given in details in chapter 2.

1. Print data arrive at one of the printer's interfaces when the host computer starts sending the data through its output port (or through a network). Data are temporarily stored in the printer's interface buffers corresponding to each interface. Most printing data normally include software commands which instruct the printer for supplementary jobs needed to accomplish printing, such as line-feeding, page -break, changing resident fonts, etc.

2. The main logic controller analyzes the data in sequence, interprets them into *dots* according to the original image, and depicts the image resultant of the dot data in the raster memory (DRAM's). Operations additionally required during processing data are accomplished by U4 (U105 for FS-1550/A) which supplements the main logic CPU.

3. While data processing is in course, on the other hand, the main logic CPU talks to the engine CPU, via the common RAM and the engine interface (U4 [U105]), to discern the readiness of the printer's engine for printing.

4. If the main logic controller determines that the engine is ready to start, it triggers the engine CPU and, according to the vertical synchronization signal, requests to feed the paper.

5. In synchronization with the succession of the paper transportation, U104 releases video data in sequence. The video data are then applied to the LED head driver together with the horizontal synchronization signal and the video clock.

6. On reception of video data, the LED head driver switches the LED segments of the head on and off and constitutes the image over the drum. The image on the drum, referred to as the *static latent image*, is applied with toner, transferred onto the paper, and finally fused permanently on the paper by means of heat and pressure.

3.2. Controller System Overview

This section contains a detailed discussion on the operating features of the printer's main logic controller circuitry. The following figures show component layout for the main logic boards depending on the printer models:

Figure 3.3. (page 7)	KP-445	FS-1550/FS-1550A
Figure 3.5. (page 12)	KP-470	FS-3400/FS-3400A
	KP-485	FS-1550+/FS-3400+

Note. KP-470 and KP-485 has the identical component layout as shown in Figure 3.2, however, they are not compatible with each other.

Depending on model and version, the printer uses different microprocessor, 68EC000 or 68EC020, for its logic controller and different circuit configuration. This section provides independent descriptions for two categories of models: Section 3.3. provides system descriptions for model FS-1550/A; section 3.4. provides those for models FS-1550+ and FS-3400/A/+.

Function of each segment in the controller system will be discussed in the following sections. In the following, the number having a letter-U prefixed means the symbol number for the chip or device which is also printed on the printed circuit board.

3.3. FS-1550/A Controller System

Figure 3.2. on the next page is a simplified functional diagram for the controller system for models FS-1550 and FS-1550A. Figure 3.3. shows the component layout for the main controller board and will help understanding the descriptions beginning on this page.

3.3.1. Controller CPU (U1)

68EC000, operating at 16 MHz clock, takes care of the timings among data and commands coming through the interfaces to the gate arrays [which are the main functionality of the controller system], dynamic RAMs, program RAMs, mask ROMs, etc. 68EC000 can allocate the address memory of up to 16 MB. The controller system employs a bank manager for allocating a large area used for the address memory (See Figure 3.1.).

3.3.2. System ROMs/RAMs

System ROMs (U1/U2)

The system ROMs includes control programs for driving CPU in the repeated routines during printing. Physical allocation is 512 kB for each of U1 through U2.

Font ROMs (U52—U57)

These ROMs include font data that retain bitmap information and algorithms for the printer's resident fonts. The total physical area is 4 MB and is expanded by the internal bank manager as shown below.

Figure 3.1. FS-1550/A Memory Map

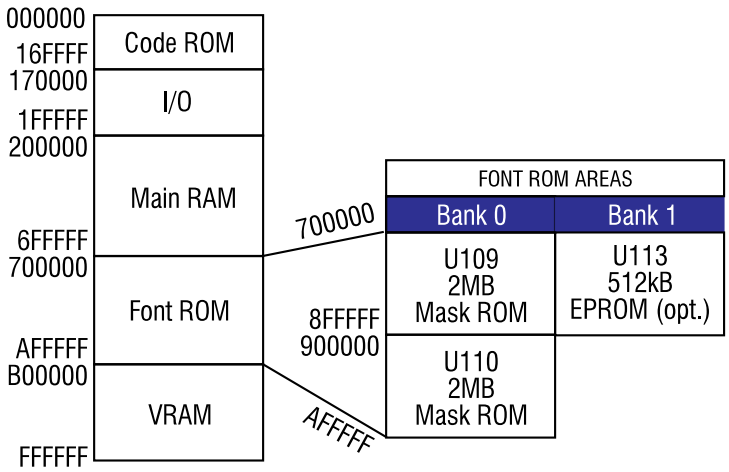
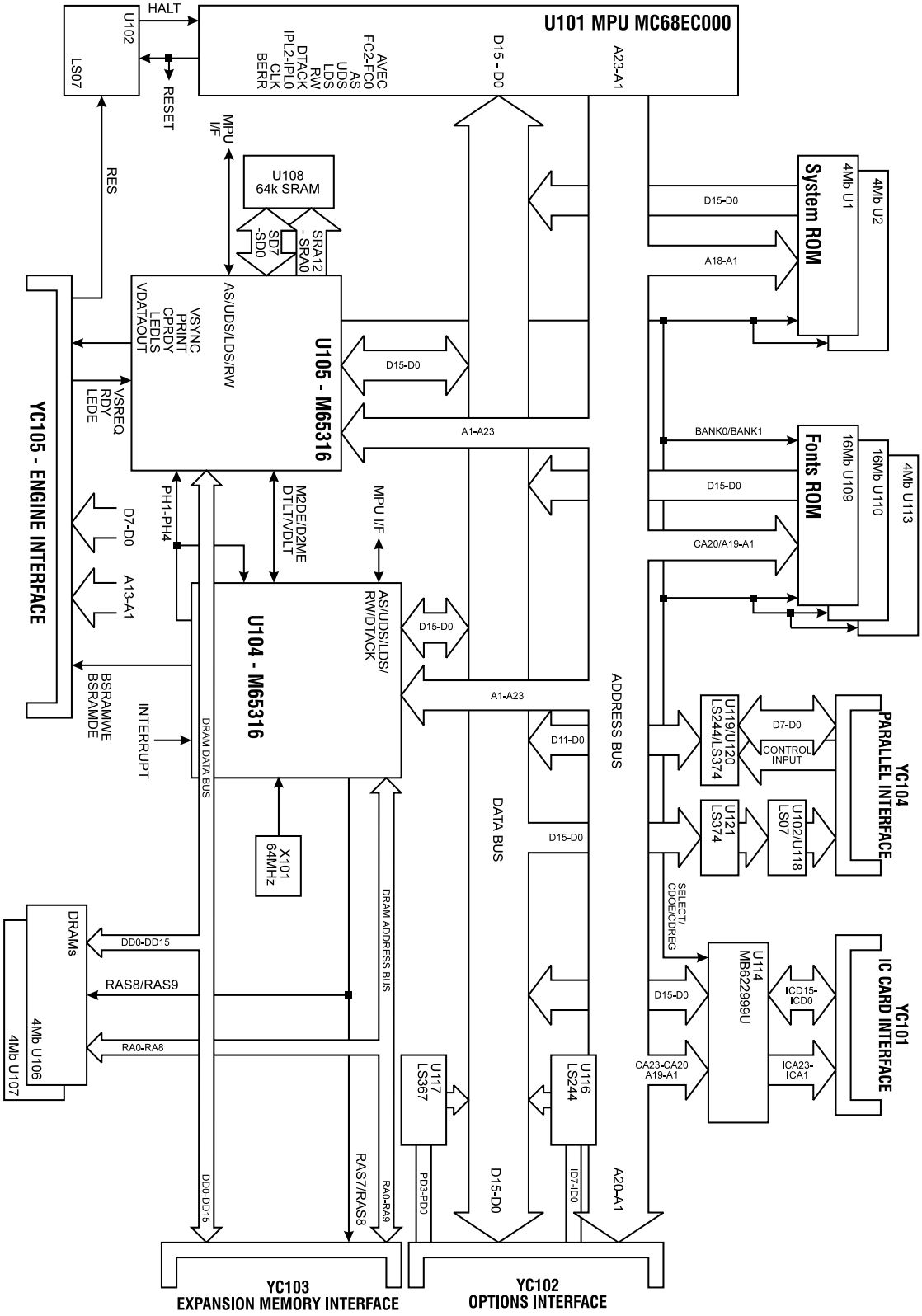
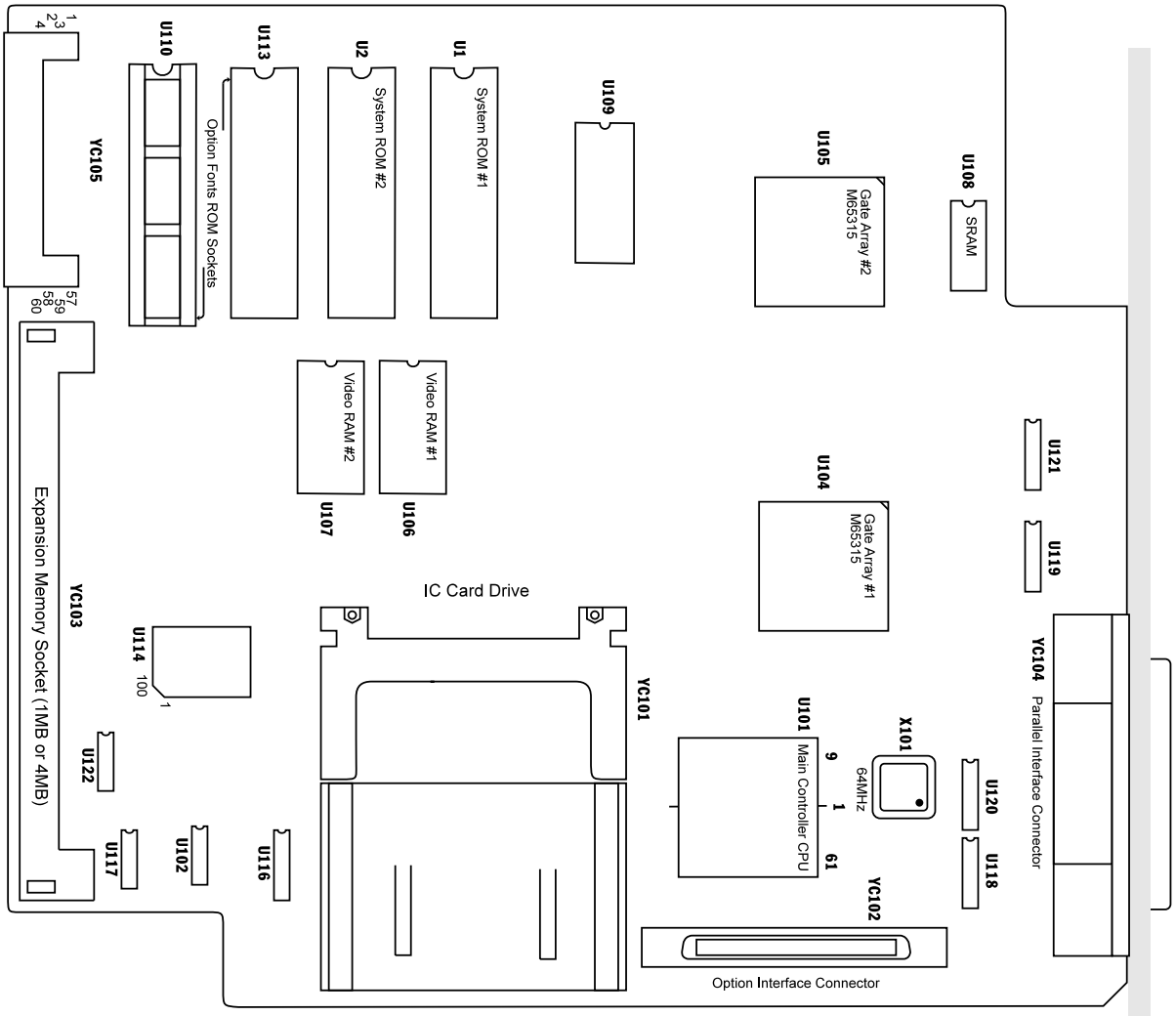


Figure 3.2. FS-1550/A Controller Diagram



VER. 1.22

Figure 3.3. FS-1550/A Main Controller Board Layout



VER. 1.22

Dynamic RAMs (U106 and U107)

The memory area these DRAMs provide is referred to as the *raster memory* or video RAM in page printer terminologies. Generation of print data is done using this area. These actually are comprised of two 512-kB (256 k by 16 bits) DRAMs and addressing the memory area of 2 MB. This area is user-expandable by means of PC-SIMMs which are available commercially.

3.3.3. Gate Arrays

Gate Array M65315 (U104)

This gate array implements the following major functions:

Address decoding: Decodes address information that 68EC000 needs in order to generate 'select' signals for use with the memories and I/O.

Clock divisor: Generates the quadruple-phase 16 MHz clock by division of the time -base module of 64 MHz.

Video data output control: Converts the video data 'drawn' in the raster memory (video RAM) into serial data. The resultant serial data is used to control the engine system.

System data bus control: Switches data buses to control the direction of data in the following:

- 68EC000 data bus
- Data bus connected to DRAMs
- Data bus connected to pattern operators

DRAM control: Takes care of timings among the signals present during reading/writing in DRAMs, and the signals during refreshing operation.

Timer control: Determines the interval of refreshing DRAMs and the programmable timer. The programmable timer operates to execute commands in the printer's firmware.

SRAM control: Implement management for the interrupting signals 68EC000 uses.

Front operator panel control: Takes control on keyboard signals and delivers the output signals for driving the panel LED indicators; and writes data for displaying messages on LCD.

Gate Array M65316 (U105)

Pattern data processing: Computes data for implementation of the required print model.

Image refinement (KIR): Provides processing data for image smoothing.

Parallel interface control: Takes care of signals coming in the parallel interface.

Engine interface: Manages communication between the controller system and the engine controller system.

SRAM (U108)

This is used for buffering video data during KIR processing.

3.4. FS-1550+/FS-3440 ser. Controller System

This section provides explanation on the controller system used for the printer models FS-1550+, FS-3400, FS-3400A, and FS-3400+.

Figure 3.5. on the next page is a simplified diagram for the controller system; Figure 3.6. shows component layout for the main controller boards and will help understanding the descriptions beginning below.

3.4.1. Controller CPU (U1)

68EC020, operating at 16.5 MHz clock, takes care of the timings among the data and commands coming through the interfaces to the gate arrays [which are the main functionality of the controller system], dynamic RAMs, program RAMs, mask ROMs, etc. 68EC020 can allocate the address memory of up to 16 MB. The controller system employs a bank manager for allocating a large area used for the address memory.

3.4.2. System ROMs/RAMs

System ROMs (U6/U7)

The system ROMs includes the control programs for driving CPU in the repeated routines during printing. Physical allocation is 1 MB using U6 and U7.

Font ROM (U10)

U10 contains bitmap data and algorithms for the printer's resident fonts. Refer to Figure 3.4. The physical area is 2 MB as allocated by *Bank 0*.

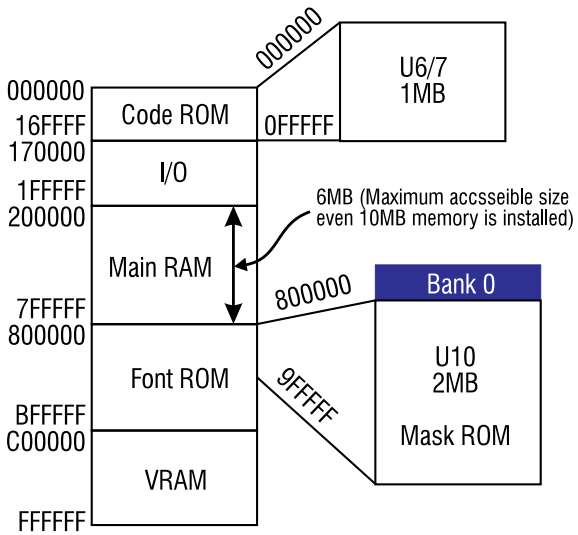


Figure 3.4. FS-1550+ & FS-3400 ser. Memory Map

VER. 1.22

Figure 3.5. FS-1550+ & FS-3400 ser. Controller Diagram

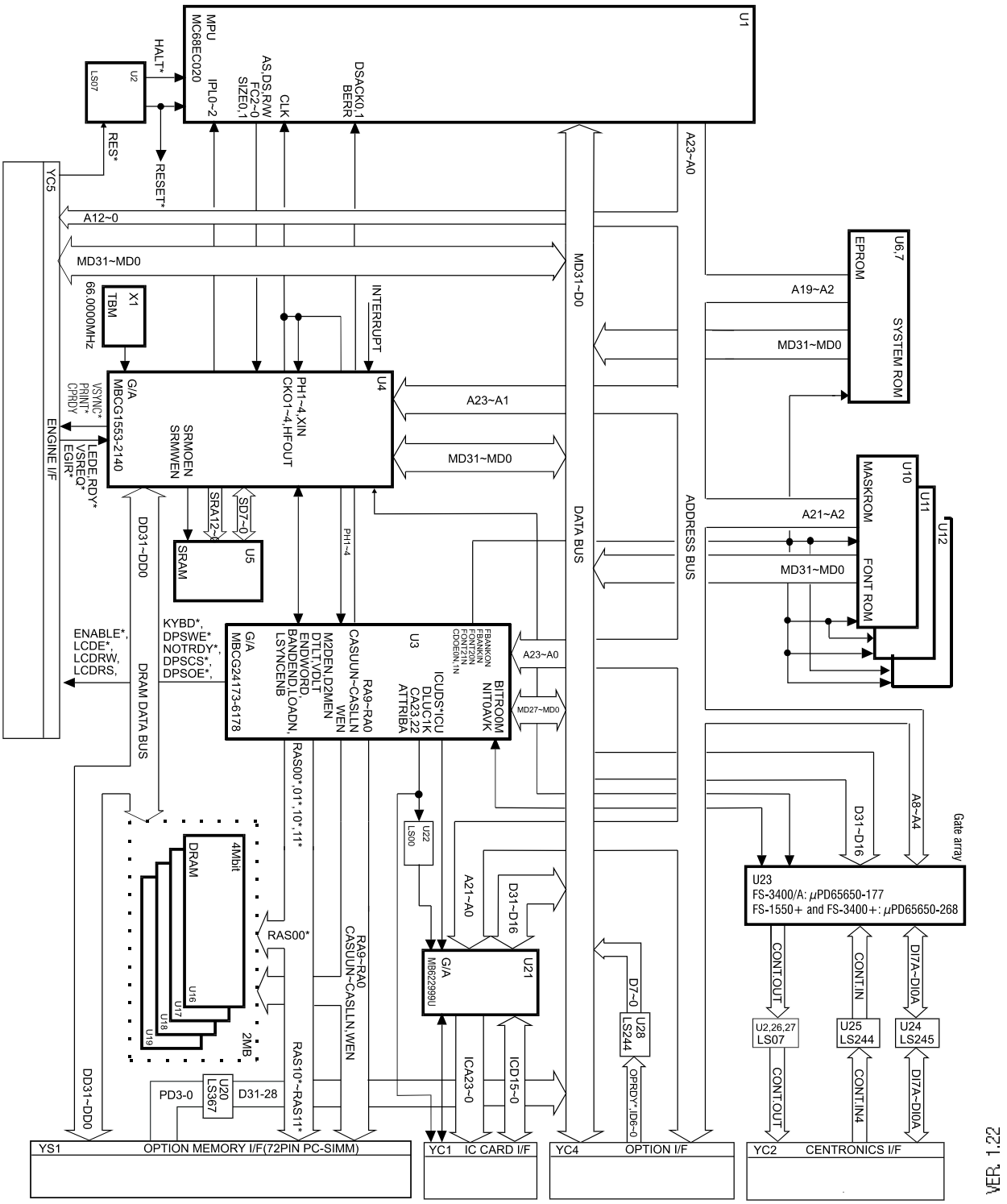
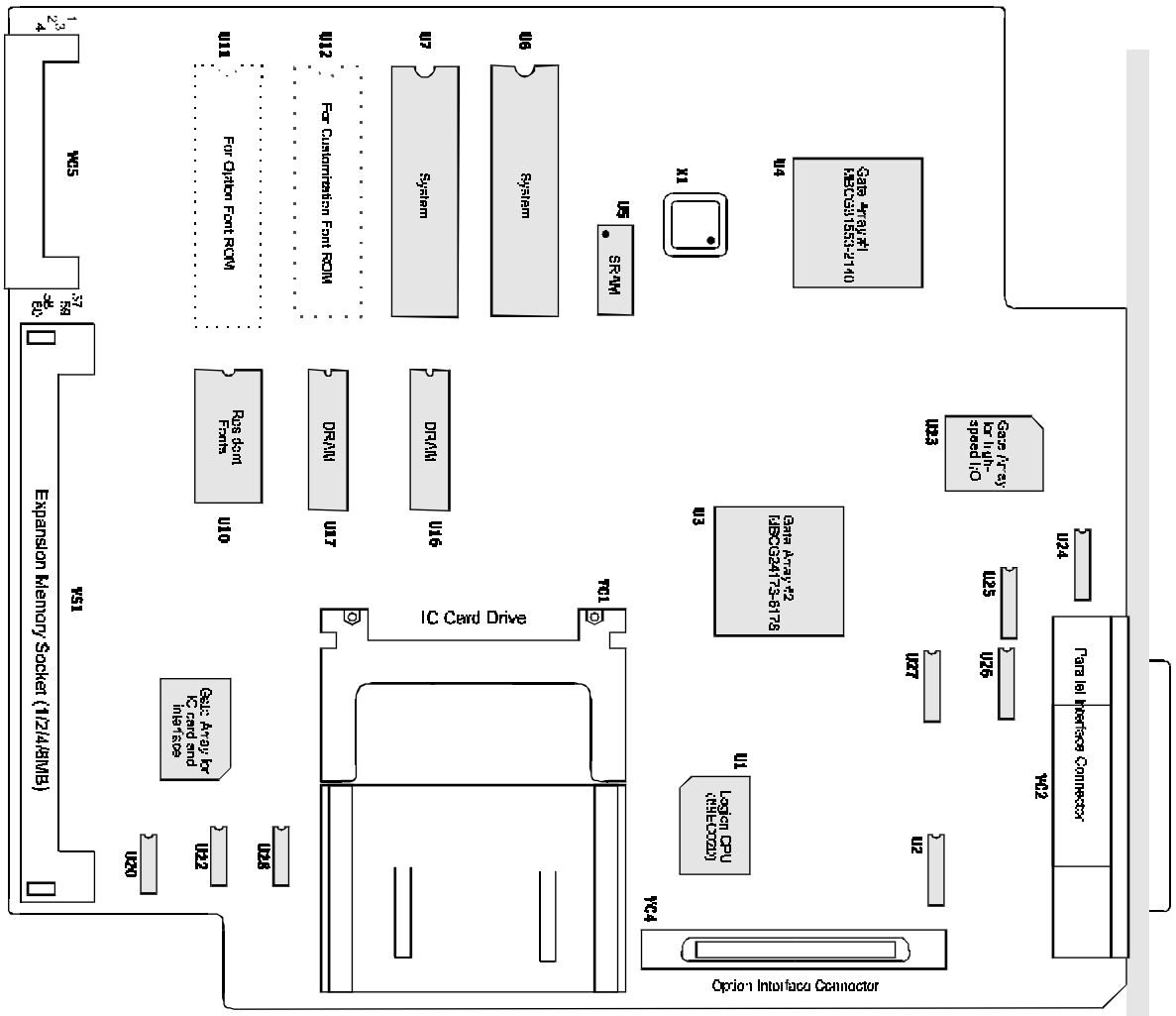


Figure 3.6. FS-1550+ & FS-3400 ser. Controller Diagram



VER. 1.22

Dynamic RAMs (U16/U17)

DRAMs provide as large as four 512 kB (512 k by 16 bits) consisting of 2 MB of memory. This is user-expandable using commercially-available PC-SIMMs.

3.4.3. Gate Arrays

Gate Array MBCG24173-6190 (U3)

This gate array provides the following functions:

DRAM management: Takes care of timings among the signals present during reading/writing DRAMs, and the signals during refreshing.

Address decoding/Transfer acknowledge control: Decodes address information that 68EC020 provides in order to generate 'select' signals for the memories and I/O.

Operator panel management: Brings keyboard signals on the operator panel into process to generate signals that activate the indicators. Also writes in data for the message display (LCD).

SRAM management: Executes management for SRAM which is used to retain the printer's permanent information.

Dual-port SRAM management: Executes management of the memory for communication between the controller system and the engine system.

Gate Array MBCG31553-2140 (U4)

This gate array implements the following functions:

DRAM data bus management: Takes control on the following three ways of data flow in the data bus:

- From DRAM data bus to CPU data bus
- From CPU to DRAM data bus
- From DRAM to the gate array's internal circuit

Triple operator operation/Pattern data processing: Provides a high-speed computation of print data and the pattern data.

Programmable timer: Provide management on the programmable timer interrupts during the internal firmware commands are executed.

Rotation: Rotates 16-bit data in either of 0°, 90°, 180°, and 270° in angle.

Interrupt management: Handles variety of interrupt signals.

Video data serialization: Converts the raster video data in DRAMs for driving the LED head.

KIR (Kyocera Image Refinement): Provides the KIR effect on the serialized video data.

Engine interface: Implements the handshake with the engine system.

Parallel interface: Handles data present on the parallel interface port.

Clock division: Generates a quadruple-phased 16 MHz clock by division of the time -base module of 64 MHz.

Magnification/reduction: Magnifies/reduces the serial data for printing by subtracting or adding data between dots.

SRAM (U5)

This is used to retain information regarding the printer's environmental parameters as set by gate arrays.

Gate array MB622999U (U21)

This gate array includes buffers for the IC card drive.

µPD65650-268 (U23) [µPD65650-177 for FS-3400/A]

This is for the parallel interface control. Timings are handled by the hardware for ensuring the higher processing speed.