Diskette Drive Controller

Figures

Description

The diskette drive controller and interface connector reside on the system board. The controller type is dependent on the system model.

The Type 1 controller supports:

- Two data transfer rates:
  - 250,000 bits per second (bps)
  - 500,000 bits per second.
- 125 nanoseconds of precompensation on all tracks
- The following IBM diskette drives:
  - 3.5-inch 1.44MB
  - 5.25-inch 360KB.

The Type 2 controller supports:

- Four data transfer rates:
  - 250,000 bits per second
  - 300,000 bits per second
  - 500,000 bits per second
  - 1,000,000 bits per second.
- Programmable precompensation
- 16 bytes of data buffering
- The following IBM diskette drives:
  - 3.5-inch 1.44MB
  - 5.25-inch 1.2MB.

The media formats supported by IBM drives are shown below.

Media Size	Unformatted Capacity	Formatted Capacity	Sectors Per Track	Number of Tracks	Data Rate (In 1,000 bps)
3.5 in.	1.0MB	720KB	9	80	250
3.5 in.	2.0MB	1.44MB	18	80	500
5.25 in.	0.5MB	360KB	9	40	300*/250
5.25 in.	1.6MB	1.20MB*	15	80	500

* Type 2 controller only

Figure 1. Media Format Table

Warning: The controller does not check to see that the media supports the selected capacity. Attempting to format media to an unsupported capacity may cause loss of data.

- 0.5MB (double sided, double density 5.25-inch) media can be reliably formatted only to the 360KB capacity.
- 1.0MB media can be reliably formatted only to the 720KB capacity.
- 1.6MB (high capacity 5.25-inch) media can be reliably formatted only to the 1.2MB capacity.
- 2.0MB media can be reliably formatted only to the 1.44MB capacity.

When the Type 1 diskette drive controller is switched from one data rate to another, the controller clock rate automatically changes to:

- 8 MHz for 2.0MB mode
- 4 MHz for 1.0MB mode.

The step rate time (SRT), head load time (HLT), and the head unload time (HUT) must then be changed to maintain the desired timings at the diskette interface.

For Type 2 controllers, the controller clock rate remains at 24MHz, but the SRT, HLT, and HUT parameters must still be updated using the same values as the Type 1 controller.

Note: With Type 1 controllers, 32-bit operations to the video subsystem may cause a Direct Memory Access (DMA) overrun. If the BIOS returns an error code indicating that an overrun has occurred, the operation should be repeated.

FIFO Mode

A 16-byte FIFO is provided on the Type 2 controller, which allows Direct Memory Access data transfers to be delayed for longer periods of time without causing DMA overrun errors. To maintain compatibility, the FIFO defaults to a Type 1 compatibility mode after system reset. All functions are then similar to the Type 1 controller.

The Configure command is used to enable FIFO operations. After the FIFO operations are enabled, the controller temporarily enters a byte mode during the command and result phases of the diskette controller operation. While in this mode, operations to, or from, the disk controller are FIFO compatible.

The FIFO is enabled only during the data transfer phase of operation. All command and status information is transferred in Type 1 compatibility mode. When the Type 2 controller first enters the data transfer phase, the FIFO is cleared of any residual data from previous operations.

Compatibility problems may occur when the FIFO mode is used with software that monitors the progress of a data transfer during the execution phase. It is recommended that the FIFO mode be disabled when software of this type is used.

Diskette Drive Controller Registers

The Type 2 controller supports a superset of the Type 1 controller registers. New functions that have been added to the Type 2 register set are noted in the individual register descriptions that follow.

Note: Some registers contain bits that are labeled as reserved. This ensures software compatibility with future system models. These bits must always be set to 0 (unless specified otherwise) when writing to the diskette controller registers.

Status Register A (Hex 03F0)

This read-only register shows the status of signals on the diskette drive interface.

Bit	Function
7	Interrupt Pending
6	-2nd Drive Installed
5	Step
4	-Track 0
3	Head 1 Select
2	-Index
1	-Write Protect
0	Direction In

Figure 2. Status Register A (Hex 03F0)

Status Register B (Hex 03F1)

This read-only register shows the status of signals on the diskette drive interface.

Bit	Function
7,6	Reserved
5	Drive Select 0
4	Write Data – Changes state when a Positive Transition on the -Write Data occurs.
3	Read Data – Changes state when a Positive Transition on the -Read Data occurs.
2	Write Enable
1	Motor Enable 1
0	Motor Enable 0

Figure 3. Status Register B (Hex 03F1)

Drive Control Register (Hex 03F2)

This read and write register controls drive motors, drive selection, and feature enable. All bits are set to 0 by a reset.

Bit	Function
7	Motor Enable 3*
6	Motor Enable 2*
5	Motor Enable 1
4	Motor Enable 0
3	Reserved = 1
2	−Diskette Controller Reset
1	Drive Select 1*
0	Drive Select 0

* Type 2 Controller Only.

Figure 4. Drive Control Register (Hex 03F2)

Note: The diskette controller reset, bit 2, must be set to 0 for a minimum of 3.5 microseconds to guarantee proper reset of the controller.

Drive Status Register (Hex 03F3 Read)

This register contains information about the diskette drive type, and start-up drive location. This register is for the Type 2 controller only.

Bit	Function
7,6	Media Type 1,0
5,4	Drive Type 1,0
3,2	Start-UP Map 1,0
1,0	Reserved

Figure 5. Drive Status Register (Hex 03F3 Read)

The following tables illustrate the media type, drive type and start-up drive location definitions:

Bit 7	Bit 6	Media Type
0	0	Reserved
0	1	Reserved
1	0	2MB
1	1	1MB

Note: These bits indicate the state of the Media type signal. These signals are inputs from the drive.

Figure 6. Media Type (Hex 03F3 Read)

Bit 5	Bit 4	Drive Type
0	0	3.5-inch, 1.44MB
0	1	Reserved
1	0	5.25 inch, 1.2MB
1	1	Reserved

Figure 7. Drive Type (Hex 03F3 Read)

Bit 3	Bit 2	Start-Up Drive
0	0	Bay A
0	1	Second Drive
1	0	Third Drive
1	1	Reserved

Figure 8. Start-Up Drive (Hex 03F3 Read)

Note: The media type and drive type bits are valid only when the drive is selected. The media type bits are valid only for 3.5-inch media types.

Diskette Drive Controller Status Register (Hex 03F4 Read)

This read-only register facilitates the transfer of data between the system microprocessor and the controller.

Bit	Function
7	Request for Master
6	Data Input/Output
5	Non DMA Mode
4	Diskette Controller Busy
3	Drive 3 Busy
2	Drive 2 Busy
1	Drive 1 Busy
0	Drive 0 Busy

Figure 9. Diskette Drive Controller Status Register (Hex 03F4)

Bit 7 When this bit is set to 1, the Data register is ready to transfer data with the system microprocessor.

Bit 6 This bit indicates the direction of data transfer between the diskette drive controller and the system microprocessor. If this bit is set to 1, the transfer is to the system microprocessor; if this bit is set to 0, the transfer is to the controller.

Bit 5 When this bit is set to 1, the controller is in the non-DMA mode.

Bit 4 When this bit is set to 1, command is being executed.

Bit 3 When this bit is set to 1, diskette drive 3 is in the seek mode.

Bit 2 When this bit is set to 1, diskette drive 2 is in the seek mode.

Bit 1 When this bit is set to 1, diskette drive 1 is in the seek mode.

Bit 0 When this bit is set to 1, diskette drive 0 is in the seek mode.

Precompensation Select Register (Hex 03F4 Write)

This write-only register is used to set the data rate and precompensation value for each data rate. This register exists only in Type 2 controllers.

Bit	Function
7-5	Reserved = 0
4	Precomp 2
3	Precomp 1
2	Precomp 0
1	Data Rate Select 1
0	Data Rate Select 0

Figure 10. Precompensation Select Register (Hex 03F4 Write)

The following table defines the precompensation values:

Bit 4	Bit 3	Bit 2	Precomp. Delay
0	0	0	Default
0	0	1	41.7 ns
0	1	0	83.3 ns
0	1	1	125 ns
1	0	0	167 ns
1	0	1	208 ns
1	1	0	250 ns
1	1	1	0.0ns

Figure 11. Precompensation Values

The following table shows the default precompensation values used when bits 4, 3, and 2 equal 000.

Bit 1	Bit 0	Data Rate	Precomp. Value
0	0	500 kbps	125 ns
0	1	300 kbps	125 ns
1	0	250 kbps	125 ns
1	1	1.0 Mbps	41.7 ns

Figure 12. Default Precompensation Values

Diskette Drive Controller Command/Data Register (Hex 03F5)

This read and write register passes data, commands and parameters to the diskette drive controller and provides diskette-drive status information.

Reserved Register (Hex 03F6)

This register is reserved.

Data Rate Status Register (Hex 03F7 - Read)

When read, this register identifies the data rate selected on the interface, and senses the state of the 'diskette change' and '-high density select' signals.

Bit	Function
7	Diskette Change
6 - 4	Reserved = 1
3	Reserved = 1
2	Data Rate Select 1
1	Data Rate Select 0
0	−High Density Select

Figure 13. Data Rate Status Register (Hex 03F7 - Read)

Data Rate Control Register (Hex 03F7 - Write)

When written, this register sets the transfer rate.

Bit	Function
7 - 3	Reserved
2	Reserved
1	Data Rate Select 1
0	Data Rate Select 0

Figure 14. Data Rate Control Register (Hex 03F7 - Write)

Bits 7 - 2 Reserved.

Bits 1, 0 These bits select the data rate, as shown in the following figure.

Bits 1 0	Data Rate
0 0	500,000 bits per second
0 1	300,000 bits per second*
1 0	250,000 bits per second
1 1	1,000,000 bits per second*

* Type 2 Controller only

Figure 15. Data Rate Selection

Diskette Drive Controller Programming Considerations

Each command is initiated by a multibyte transfer from the system microprocessor; the result can be a multibyte transfer back to the system microprocessor. Most transfers consist of three phases:

- *Command Phase:* The system microprocessor writes a series of command bytes to the controller directing it to perform a specific operation.
- *Execution Phase:* The controller performs the specified operation.
- *Result Phase:* After the operation is complete, status information is available to the system microprocessor through a sequence of read commands.

Note: The Seek, Relative Seek, and Recalibrate commands have no result phase. After issuing these commands, the Sense Interrupt Status command must be issued for proper termination and verification of the head position (Present Cylinder Number parameter or PCN).

Controller Commands

The following commands are supported by the diskette drive controller:

- Configure#
- Dumpreg#
- Format Track
- Read Data
- Read Deleted Data
- Read ID
- Read Track
- Recalibrate
- Relative Seek#
- Scan Equal
- Scan High or Equal
- Scan Low or Equal
- Seek
- Sense Drive Status
- Sense Interrupt Status
- Specify
- Verify#
- Version#
- Write Data
- Write Deleted Data.

Notes:

1. Commands marked with a pound sign are not supported by the Type 1 controller.
2. Diskette BIOS may not support all commands listed. To ensure software compatibility across system models, the diskette hardware should be accessed only through the diskette BIOS.

Symbol definitions are shown in Figures 16 and 17 on the following pages.

Symbol	Name	Description
DIR	Direction Control	This bit, when set to 0, causes the head to move away from the spindle during an Implied Seek. When set to 1, the head moves toward the spindle.
EC	Enable Count	This bit, when set to 1 enables the data length byte to become the number of sectors/track.
EFF	Enable FIFO (Type 2)	This bit, when set to 1, enables the Type 2 controller FIFO data buffer.
EIS	Enable Implied Seek (Type 2)	This bit, when set to 1, causes an implied Seek to be performed before executing a command that requires the Cylinder parameter in the command phase.
GPL	GAP 3 Length	This parameter determines the length of GAP 3, in bytes, during a Format operation and determines the VCO synchronization timing during Read operations.
HD	Head Select	This bit, when set to 0, selects Head 0, and selects Head 1 when set to 1.
HLT	Head Load Time	HLT is the head load time parameter. The programmable head load time ranges from 1 to 512 ms, as shown in the HLT parameter definition table on page 15.
HUT	Head Unload Time	HUT is the head unload time following a Read or Write operation. The programmable head unload time ranges from 8 to 512 ms, as shown in the HUT parameter definition on page 15.
MFM	FM or MFM	This bit, when set to 0, selects FM mode, and when set to 1, selects MFM mode.
MT	Multitrack	This bit, when set to 1, selects multitrack operation. (Side 0 and Side 1 are automatically read, written or verified).

Figure 16. (Page 1 of 2) Command Symbols, Diskette Drive Controller

Symbol	Name	Description
ND	Non DMA Mode	ND causes diskette operations to occur in the non DMA mode.
PD	Polling Disable	PD disables polling when set to 1 and enables polling when set to 0.
PTN	Precompensation Track Number	PTN is the track number where write precompensation begins. It is programmable from 0 to FFH.
RCN	Relative Cylinder Number	Indicates the relative cylinder from the present cylinder, as used by the Relative Seek command.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during execution of Read Data. If Read Deleted Data is executed, only sectors with a deleted address mark will be accessed. When set to 0, the sector is read or written the same as the read and write commands.
SRT	Step Rate Time	SRT is the stepping rate for the diskette drive. The programmable step rate time ranges from 0.5 to 32ms, as shown in the SRT parameter definition table on page 16.
THR	Threshold	THR is the FIFO threshold for Type 2 controllers where 0 = 1 byte, F = 16 bytes.
US	Unit Select	US indicates the drive number selected. 00 selects drive 0, 01 selects drive 1, 10 selects drive 2 and 11 selects Drive 3.

Figure 17. (Page 2 of 2) Command Symbols, Diskette Drive Controller

Head load time (HLT), head unload time (HUT), and set rate time (SRT) parameters are shown in the following three figures.

HLT Parameter	1 Mbps	500 kbps	300 kbps	250 kbps
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
7E	126	252	420	504
7F	127	254	423	508

Note: Delay time in ms at indicated data rate

Figure 18. HLT Parameter Definitions

HUT Parameter	1 Mbps	500 kbps	300 kbps	250 kbps
0	128	256	426	512
1	8	16	26.7	32
2	16	32	53.4	64
3	24	48	80.1	96
4	32	64	107	128
5	40	80	134	160
6	48	96	160	192
7	56	112	187	224
8	64	128	214	256
9	72	144	240	288
A	80	160	267	320
B	88	176	294	352
C	96	192	320	384
D	104	208	347	416
E	112	224	373	448
F	120	240	400	480

Note: Delay time in ms at indicated data rate

Figure 19. HUT Parameter Definitions

SRT Parameter	1 Mbps	500 kbps	300 kbps	250 kbps
0	8.0	16.0	26.7	32.0
1	7.5	15.0	25.0	30.0
2	7.0	14.0	23.3	28.0
3	6.5	13.0	21.7	26.0
4	6.0	12.0	20.0	24.0
5	5.5	11.0	18.3	22.0
6	5.0	10.0	16.7	20.0
7	4.5	9.0	15.0	18.0
8	4.0	8.0	13.3	16.0
9	3.5	7.0	11.7	14.0
A	3.0	6.0	10.0	12.0
B	2.5	5.0	8.33	10.0
C	2.0	4.0	6.67	8.0
D	1.5	3.0	5.00	6.0
E	1.0	2.0	3.33	4.0
F	0.5	1.0	1.67	2.0

Note: Delay time in ms at indicated data rate

Figure 20. SRT Parameter Definitions

The following commands are issued to the controller by the system.

Configure Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	1	0	0	1	1
Byte 1	0	0	0	0	0	0	0	0
Byte 2	0	EIS	EFF	PD	THR	THR	THR	THR
Byte 3	PTN	PTN	PTN	PTN	PTN	PTN	PTN	PTN

Figure 21. Configure Command

Result Phase: This command has no result phase.

Dumpreg Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	0

Figure 22. Dumpreg Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Present Track Number – Drive 0							
Byte 1	Present Track Number – Drive 1							
Byte 2	Present Track Number – Drive 2							
Byte 3	Present Track Number – Drive 3							
Byte 4	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT
Byte 5	HLT	HLT	HLT	HLT	HLT	HLT	HLT	ND
Byte 6	Number of Sectors per Track/End of Track							
Byte 7	0	0	0	0	0	0	0	0
Byte 8	0	EIS	EFF	PD	THR	THR	THR	THR
Byte 9	PTN	PTN	PTN	PTN	PTN	PTN	PTN	PTN

Figure 23. Dumpreg Result

Format Track Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MFM	0	0	1	1	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Number of Data Bytes in Sector							
Byte 3	Sectors per Track							
Byte 4	Gap Length							
Byte 5	Fill Byte							

Figure 24. Format Track Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Reserved
Byte 4	Reserved
Byte 5	Reserved
Byte 6	Reserved

Figure 25. Format Track Result

Read Data Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	0	0	1	1	0
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Figure 26. Read Data Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 27. Read Data Result

Read Deleted Data Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	0	1	1	0	0
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Figure 28. Read Deleted Data Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 29. Read Deleted Data Result

Read ID Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MFM	0	0	1	0	1	0
Byte 1	0	0	0	0	0	HD	US	US

Figure 30. Read ID Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 31. Read ID Result

Read Track Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MFM	0	0	0	0	1	0
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Figure 32. Read Track Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 33. Read Track Result

Recalibrate Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	0	0	0	0	0	0	US	US

Figure 34. Recalibrate Command

Result Phase: This command has no result phase.

Relative Seek Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	1	DIR	0	0	1	1	1	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	RCN	RCN	RCN	RCN	RCN	RCN	RCN	RCN

Figure 35. Relative Seek Command

Result Phase: This command has no result phase.

Scan Equal Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	1	0	0	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Figure 36. Scan Equal Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 37. Scan Equal Result

Scan High or Equal Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	1	1	1	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Figure 38. Scan High or Equal Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 39. Scan High or Equal Result

Scan Low or Equal Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	1	1	0	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Figure 40. Scan Low or Equal Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 41. Scan Low or Equal Result

Seek Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	New Track Number after Seek							

Figure 42. Seek Command

Result Phase: This command has no result phase.

Sense Drive Status Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	0
Byte 1	0	0	0	0	0	HD	US	US

Figure 43. Sense Drive Status Command

Result Phase

Byte 0	Status Register 3

Figure 44. Sense Drive Status Result

Sense Interrupt Status Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0

Figure 45. Sense Interrupt Status Command

Result Phase

Byte 0	Status Register 0
Byte 1	Present Track Number

Figure 46. Sense Interrupt Status Result

Specify Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT
Byte 2	HLT	HLT	HLT	HLT	HLT	HLT	HLT	ND

Figure 47. Specify Command

Result Phase: This command has no result phase.

Verify Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	SK	1	0	1	1	0
Byte 1	EC	0	0	0	0	HD	US	US
Byte 2	Cylinder Address							
Byte 3	Head Address							
Byte 4	Sector Address							
Byte 5	Sector size							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Byte Transfer Control							

Figure 48. Verify Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Cylinder Address
Byte 4	Head Address
Byte 5	Sector Address
Byte 6	Sector size

Figure 49. Verify Result

Version Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	1	0	0	0	0

Figure 50. Version Command

Result Phase

Byte 0	1	0	0	X	0	0	0	0

Note – x can be a 1 or a 0.

Figure 51. Version Result

Write Data Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	0	0	0	1	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Figure 52. Write Data Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 53. Write Data Result

Write Deleted Data Command

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MFM	0	0	1	0	0	1
Byte 1	0	0	0	0	0	HD	US	US
Byte 2	Track Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End-of-Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Figure 54. Write Deleted Data Command

Result Phase

Byte 0	Status Register 0
Byte 1	Status Register 1
Byte 2	Status Register 2
Byte 3	Track Number
Byte 4	Head Address
Byte 5	Sector Number
Byte 6	Number of Data Bytes in Sector

Figure 55. Write Deleted Data Result

Invalid Command Status

Result Phase: The following status byte is returned to the system microprocessor when an invalid command has been received.

Byte 0	Status Register 0 = hex 80

Figure 56. Invalid Command Result

Note: Bits 6 and 7 in Status Register 0 are used to indicate command status. When an invalid command is processed, this information is returned to the system microprocessor in the Invalid Command Status byte.

Command Status Registers

This section provides definitions for status registers 0 through 3.

Status Register 0

Bit	Function
7, 6	Interrupt Code
5	Seek End
4	Equipment Check
3	Reserved = 0
2	Head Address
1, 0	Drive Select

Figure 57. Status Register 0

Bits 7, 6 These bits indicate the command interrupt status.

Bits 7 6	Function
0 0	Normal Termination of Command
0 1	Abnormal Termination of Command
1 0	Invalid Command Issued
1 1	Reserved

Figure 58. Status Register 0 (Bits 7, 6)

Bit 5 This bit is set to 1 when the diskette drive completes the Seek or Recalibrate command, or a read or write operation with an implied Seek command.

Bit 4 This bit is set to 1 if the '-track 0' signal fails to occur after the Recalibrate command is issued or Relative Seek command to step outward beyond track 0.

Bit 3 Reserved. This bit is always set to 0.

Bit 2 This bit indicates the state of the '-head select' signal after the command was performed. When set to 1, head 1 was selected; when set to 0, head 0 was selected.

Bit 1, 0 These bits indicate the drive that was selected upon command completion.

Bits 1 0	Function
1 1	Drive 3
1 0	Drive 2
0 1	Drive 1
0 0	Drive 0

Figure 59. Status Register 0 (Bits 1, 0)

Status Register 1

Bit	Function
7	End-of-Track
6	Reserved
5	Cyclic Redundancy Check (CRC) Error
4	Overrun/Underrun Error
3	Reserved = 0
2	No Data
1	Not Writable
0	Missing Address Mark

Figure 60. Status Register 1

Bit 7 This bit is set to 1 when the controller tries to gain access to a sector beyond the final sector of a track.

Bit 6 Reserved. This bit is always set to 0.

Bit 5 This bit is set to 1 when a CRC error is detected in the ID or data field.

Bit 4 This bit is set to 1 if the system does not service the diskette drive controller within an adequate period of time during data transfers.

Bit 3 Reserved. This bit is always set to 0.

Bit 2 This bit is set to 1 when:

- The controller cannot find the sector specified in the ID register during the execution of a Read Data, Read Deleted Data, or Read ID or Read Track command.
- The controller cannot read the ID field without an error during the execution of a Read ID command
- The starting sector cannot be found during the execution of a Read Track command.

Bit 1 This bit is set to 1 when the '-write-protect' signal is active during a Write Data, Write Deleted Data, or Format Track command.

Bit 0 This bit is set to 1 if the controller cannot detect an address mark. When this occurs, bit 0 of Status Register 2 indicates whether the missing address mark is an ID-address mark or a data-address mark.

Status Register 2

Bit	Function
7	Reserved = 0
6	Control Mark
5	CRC Error in Data Field
4	Wrong Track
3	Scan Equal
2	Scan Not Satisfied
1	Bad Track
0	Missing Address Mark in Data Field

Figure 61. Status Register 2

Bit 7 Reserved. This bit is always set to 0.

Bit 6 This bit is set to 1 when the controller encounters a sector that has a deleted data-address mark during a Read Data or a Read Deleted Data encounters a data address mark.

Bit 5 This bit is set to 1 if the controller detects an error in the data.

Bit 4 This bit is set to 1 when the track number on the media is different from the track number issued by the command. When this occurs, bit 2 of Status Register 1 is also set to 1.

Bit 3 This bit is set to 1 during the Scan command when the conditions for "Equal" are satisfied.

Bit 2 This bit is set to 1 during the Scan Command when the scan conditions are not satisfied.

Bit 1 This bit is set to 1 when the track number on the media is hex FF and the track number value stored in the ID register is not hex FF. When this occurs, bit 2 of Status Register 1 is also set to 1.

Bit 0 This bit is set to 1 when the controller cannot find a data-address mark. This bit is set to 0 when an ID-address mark cannot be found. Bit 0 in Status Register 0 is also set if either address mark cannot be found.

Status Register 3

Bit	Function
7	Reserved = 0
6	Write Protect
5	Reserved = 1
4	Track 0
3	Reserved = 1
2	Head Address
1, 0	Drive Select

Figure 62. Status Register 3

Bit 7 Reserved. This bit is always set to 0.

Bit 6 This bit indicates the status of the '-write-protect' signal from the diskette drive. When this bit is set to 1, the '-write-protect' signal is active.

Bit 5 Reserved. This bit is always set to 1.

Bit 4 This bit indicates the status of the '-track 0' signal from the diskette drive. When this bit is set to 1, the '-track 0' signal is active.

Bit 3 Reserved. This bit is always set to 1.

Bit 2 This bit indicates the status of the '-head 1 select' signal from the diskette drive. When this bit is set to 1, the '-head 1 select' signal is active.

Bits 1, 0 These bits indicate the current selected drive.

Interface Signal Descriptions

The following section describes the interface signals to the diskette drive.

Output Signals

All output signals to the diskette drive operate between 5 Vdc and ground, with the following definitions:

- The inactive level is 2.0 Vdc minimum.
- The active level is 0.8 Vdc maximum.

-HIGH DENSITY SELECT: When this signal is active, the 2MB mode is selected. Diskettes are formatted with 18 sectors per track and a capacity of 1.44MB. When this signal is inactive, the 1MB mode is selected. Diskettes are formatted with 9 sectors per track and a capacity of 720KB.

DATA RATE SELECT 0 - 1: These signals are driven by the system to select the data rate of devices on the diskette drive interface.

-DRIVE SELECT: The drive-select signal enables or disables all drive interface signals except -MOTOR ENABLE. When the drive select signal is active, the drive is enabled. When it is inactive, all controlled inputs are ignored and all drive outputs are disabled.

-MOTOR ENABLE: When this signal is made active, the spindle starts to turn. There must be a 500-millisecond minimum delay after -MOTOR ENABLE becomes active before a read, write, or seek operation is initiated (750 ms for 5.25-inch drive types). When inactive, this signal causes the spindle motor to decelerate and stop.

-DIRECTION IN: When this signal is active, -STEP moves the heads toward the drive spindle. When this signal is inactive, -STEP moves the heads away from the drive spindle. This signal is stable for at least 1 microsecond before and after the trailing edge of the -STEP pulse.

Note: After a direction change, a 15-millisecond minimum delay is required before the next '-step' pulse is issued.

-STEP: A 1-microsecond active pulse of this signal causes the read/write heads to move one track. The state of -DIRECTION at the trailing edge of -STEP determines the direction of motion.

Note: A 15-millisecond seek settle time must be provided after the last step pulse occurs before a read, write, or seek operation initiated.

-WRITE DATA: A 125-nanosecond minimum pulse of this signal causes a flux reversal to occur on the media if -WRITE ENABLE is active.

-WRITE ENABLE: When active, this signal enables the write current circuits and -WRITE DATA controls the writing of information. Motor-start and head-settle times must be observed before this signal becomes active.

-HEAD 1 SELECT: When active, this signal selects the upper head; when inactive, the lower head is selected.

Input Signals

All input signals from the drive can sink 4.0 milliamperes at the active level.

- The inactive level is 3.7 Vdc minimum.
- The active level is 0.4 Vdc maximum.

DRIVE TYPE ID 0 - 1: These signals provide encoded drive-type information to the system when the drive is selected.

MEDIA TYPE ID 0 - 1: These signals provide encoded media-type information to the system when the drive is selected.

-INDEX: When the drive senses the index, it generates an active pulse of at least 1 millisecond on this line.

-TRACK 0: This signal is active when the read/write head is on track 0. Track 0 is determined by a sensor, not a track counter.

The drive can seek to track 0, under control of the system even if no diskette is installed. This allows system software to determine how many drives there are attached to the system. Software selects each drive and attempts to recalibrate that drive to track 0. The track 0 indication determines whether or not each drive is installed in the system.

-WRITE PROTECT: When this signal is active the drive cannot write data to the diskette.

-READ DATA: Each flux reversal detected on the media provides a 125-nanosecond minimum active pulse on this line.

-DISKETTE CHANGE: This signal is active at power-on and latched inactive when a diskette is present, the drive is selected and a step pulse occurs. This signal goes active when the diskette is removed from the drive. The presence of a diskette is determined by a sensor.

Connector

Signals and voltages are transferred between the system board and the diskette drives by a cable or printed-circuit board. The printed-circuit board provides a 2- by 20-pin card edge connector for each diskette drive, with a locator key between pins 34 and 36. The cable interface provides a 2 x 17 pin header connector to each diskette drive, with a locator key below pin 17.

The following figures show the signals and DC voltages for each diskette drive connector type:

Pin	Signal	Pin	Signal
1	Ground	2	-High Density Select
3	Reserved	4	Reserved
5	Ground	6	Reserved
7	Ground	8	-Index
9	Ground	10	Reserved
11	Ground	12	-Drive Select
13	Ground	14	Reserved
15	Ground	16	-Motor Enable
17	Ground	18	-Direction In
19	Ground	20	-Step
21	Ground	22	-Write Data
23	Ground	24	-Write Enable
25	Ground	26	-Track 0
27	Ground	28	-Write Protect
29	Ground	30	-Read Data
31	Ground	32	-Head 1 Select
33	Ground	34	-Diskette Change
35	Ground	36	Ground
37	Ground	38	+5 VDC
39	Ground	40	+12 VDC

Figure 63. Diskette Drive Connector Signal Assignments For the 40-pin Card Edge Interface

Pin	Signal	Pin	Signal
1	Ground	2	-High Density Select
3	+5VDC	4	Drive Type ID 1
5	Ground	6	+12DC
7	Ground	8	-Index
9	Ground	10	Reserved
11	Ground	12	-Drive Select
13	Ground	14	Reserved
15	Ground	16	-Motor Enable
17	Ground	18	-Direction In
19	Ground	20	-Step
21	Ground	22	-Write Data
23	Ground	24	-Write Enable
25	Ground	26	-Track 0
27	Ground	28	-Write Protect
29	Ground	30	-Read Data
31	Ground	32	-Head 1 Select
33	Ground	34	-Diskette Change

Figure 64. Diskette Drive Connector Signal Assignments For the 34-pin Header Interface

Pin	Signal	Pin	Signal
1	Ground	2	Data Rate Select 1
3	+5VDC	4	Drive Type ID 1
5	Ground	6	+12DC
7	Ground	8	-Index
9	Drive Type ID 0	10	Reserved
11	Ground	12	-Drive Select
13	Ground	14	Reserved
15	Ground	16	-Motor Enable
17	Media Type ID 1	18	-Direction In
19	Ground	20	-Step
21	Ground	22	-Write Data
23	Ground	24	-Write Enable
25	Ground	26	-Track 0
27	Media Type ID 0	28	-Write Protect
29	Ground	30	-Read Data
31	Ground	32	-Head 1 Select
33	Data Rate Select 0	34	-Diskette Change

Figure 65. Diskette Drive Connector Signal Assignments For the Enhanced 34-Pin Header Interface

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