IMS INTERNATIONAL

DISK STORAGE SUBSYSTEM - 5 1/4" WINCHESTER DISKS

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Revision 1.1

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5 1/4" WINCHESTER DISK STORAGE SUBSYSTEM

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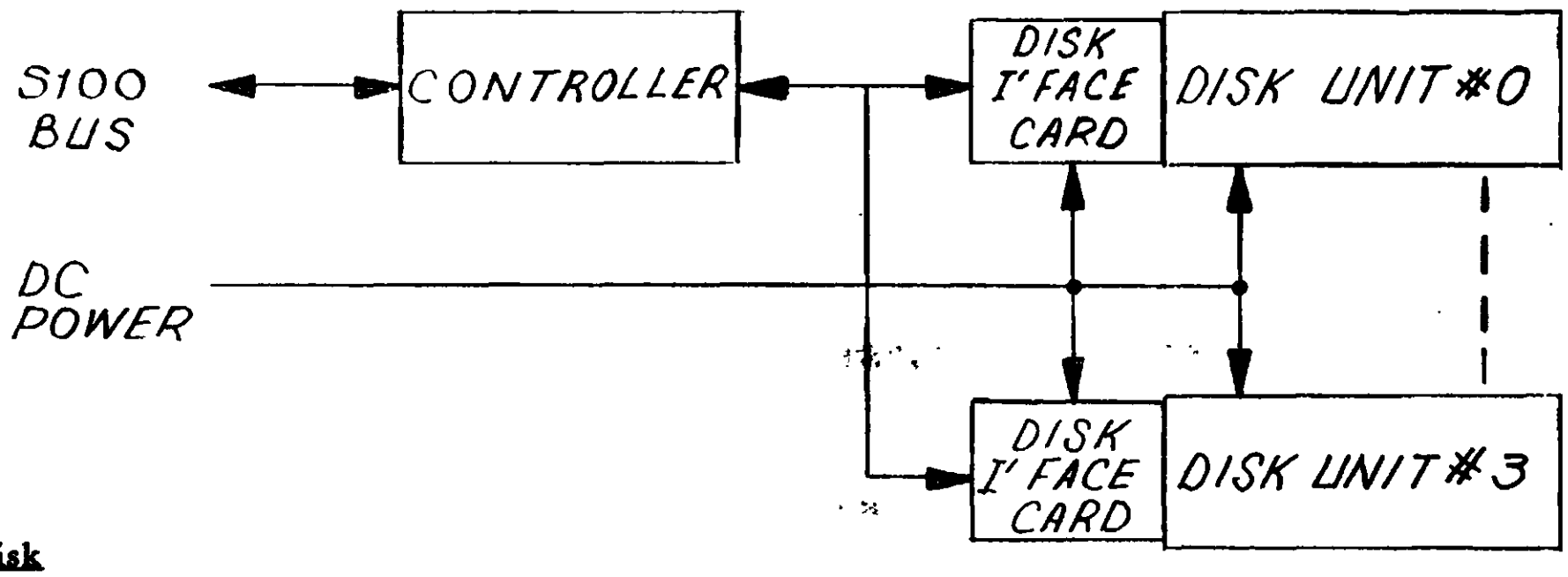
DESCRIPTION

The disk subsystem consists of the controller, up to 4 disk units, a disk interface card for each disk unit, together with power and control cables, shown below:



Disk

The disk unit is a 5 1/4 inch Winchester Technology sealed fixed disk drive with typical specifications as follows:

Environment:	Ambient Temperature	40° to 122° F.
	Relative Humidity	8 to 80%
	Wet Bulb	78° non-condensing maximum
Power:	+ 12VDC ± 5%, 1.8 A typical, 4.5 A maximum during power on	
	+ 5VDC ± 5%, 1.0 A maximum	
Unformatted Capacity:	10416 bytes per track	
Transfer Rate:	5.0 megabits per second	
Access Time:	3 milliseconds track to track 20 milliseconds settling time	

Interface Card

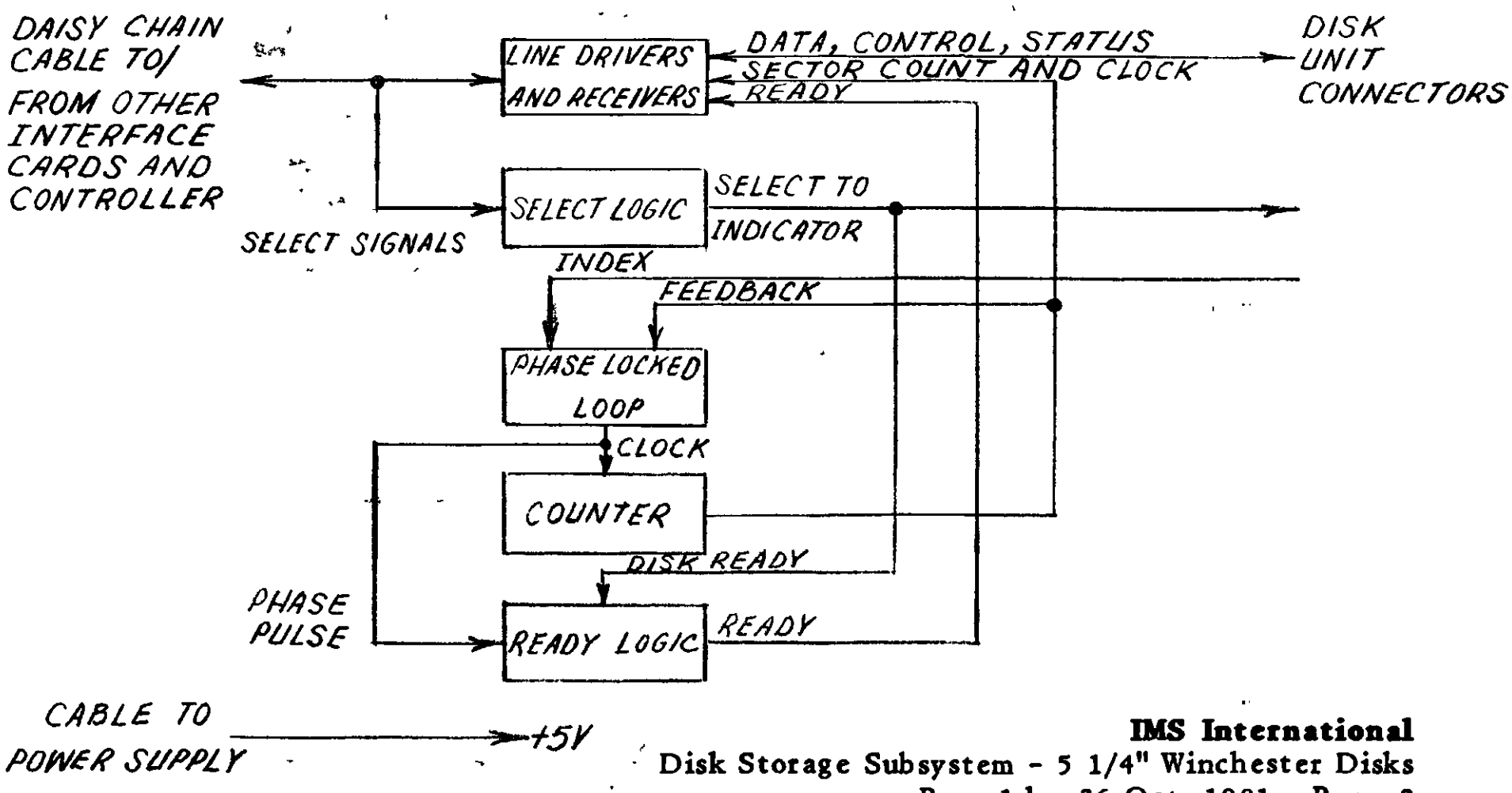
The interface card provides sector signals to the controller to use in disk read, write, or format operations by using a phase locked loop referenced to the disk unit's index signal.

The controller also uses the interface logic to generate the step pulses sent to the disk unit during seek operations.

The disk unit is configured so that it is always selected, regardless of the state of the controller's unit select signals. This gates the index signal from the disk unit and permits the loop to lock continuously.

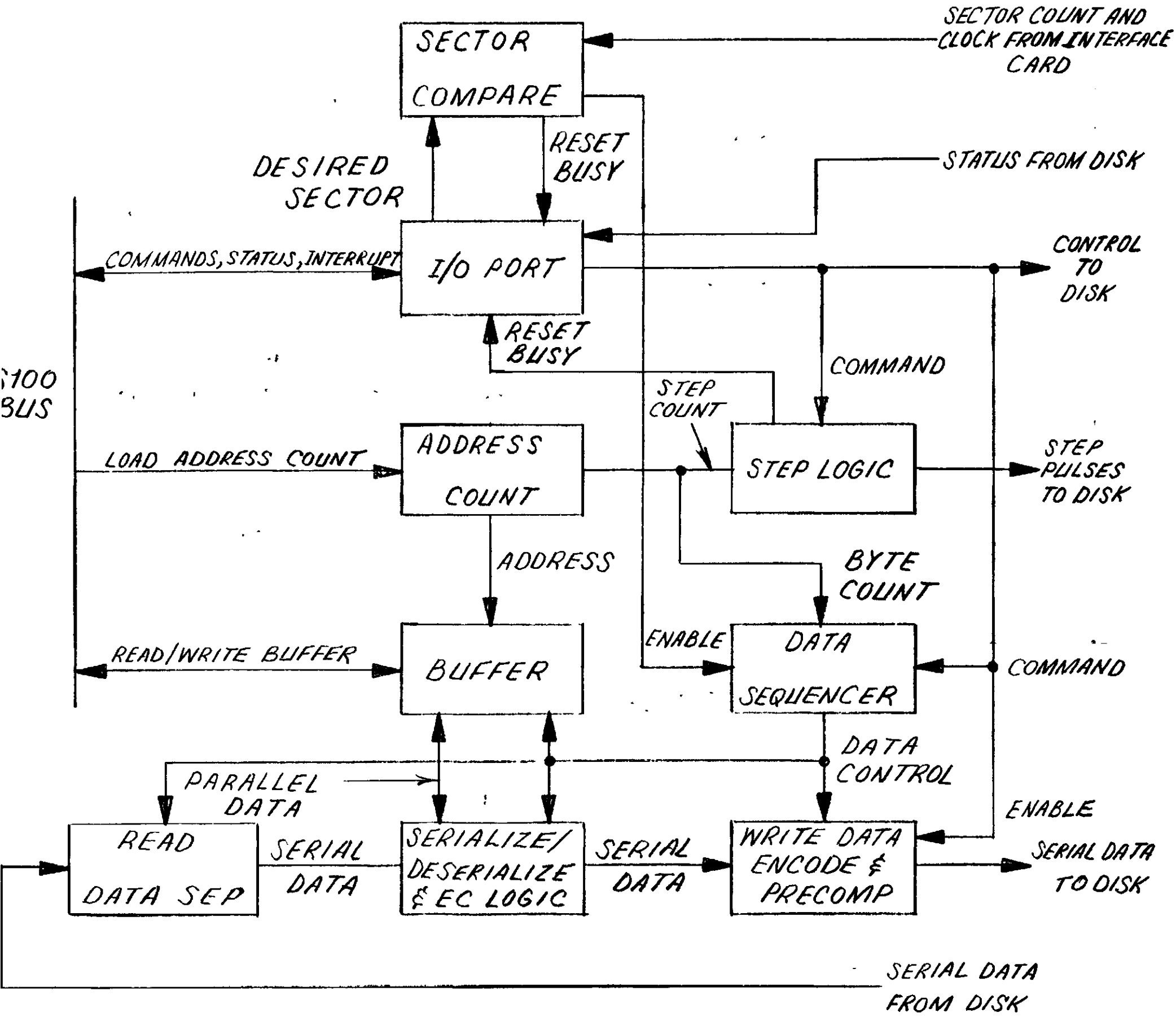
The interface card can accept any one of the four unit select signals from the controller. It uses this select to enable line drivers and receivers to gate signals to and from the "always selected" disk unit. The select signal is sent to the disk unit to operate the indicator on the disk's front panel.

The Ready Logic includes circuitry to monitor that the phase locked loop is locked. The "Ready" signal sent to the controller is the logical "and" of disk unit ready and loop locked.



Controller

The controller provides the means to transfer data between the S-100 bus and the disk units. A diagram and discussion follow.



Command information from the S-100 bus is registered in the controller's 8255 I/O Port. The 8255's "A" port, output mode 1, holds the read, write, or seek command, the step direction, and the desired sector address. The Port A "OBF" output functions as a "Busy" signal and enables the read/write or seek logic; the "ACK" input is used to reset "Busy" and to set interrupt.

The 8255's "B" port (output mode 0) holds 2 unit select bits, 3 head select bits, the write low current bit, and the write precompensation enable bit.
The 8255's "C" port, mode set as input, is used to send status information to the S-100 bus.

The controller includes a 1K byte data buffer through which data is transferred to and from either the disk or the system.

Media error control is accomplished by appending a 4 byte error checking and correction (ECC) polynomial to each disk sector written; on read the ECC is recalculated and compared to the written ECC. The program examines these bytes to determine if a read error occurred, whether the error is soft or hard (by multiple reads on ECC error), and whether the error is correctable or not.

ADDRESSING AND BIT ASSIGNMENTS

The standard controller responds to commands to I/O addresses A0-A7 (hex). Provision is made to reassign the controller's addresses to A8-AF.

I/O Address	Function
A0	Read or Write Data Buffer & Increment Address Counter I/O commands to A0 read or write the controller's 1K byte data buffer. The data byte is transferred from or to the location addressed by the buffer address counter. The buffer address is incremented after the I/O transfer
A1	Write Buffer Address Counter LS Byte. This address is used to write the least significant 8 bits of the buffer address counter, which must be initialized prior to data block transfers or seek commands.

A2	Write Buffer Address Counter MS Nibble. This address is used to write the most significant 4 bits of the buffer address counter.
A3	Not Used
A4	Read or Write 8255 Port A = Command and Sector
A5	Read or Write 8255 Port B = Head and Unit
A6	Read 8255 Port C = Status
A7	Write 8255 Mode or Write 8255 Port C Bits

The 8255 modes and bit assignments follow.

A4 Port A, Mode 1 Output

Bit	Mnemonic	Meaning/Use
7	RWCMD	1 = perform disk read or write; 0 = perform seek
6	READ	With RWCMD, 1 = read disk; 0 = write disk
5	STEPOUT	With not RWCMD, 1 = seek out (toward track 0); 0 = seek in
4	DSEC4	With RWCMD, Bits 0-4 address the desired sector
3	DSEC3	to be read or written. DSEC4 is desired sector
2	DSEC2	Address bit 4, DSEC3 is bit 3, etc.
1	DSEC1	
0	DSEC0	

A5 Port B, Mode 0 Output

Bit	Mnemonic	Meaning/Use
7	-	Always 0;
6	PRECMP	1 = enable write precompensation; used when writing cylinder 64 and higher
5	LOCUR	1 = reduce write current; used when writing cylinder 128 and higher.

4	HDSEL2	Head address for disk read or write operation; HDSEL2 is head address bit 2, HDSEL1 is bit 1, etc.
3	HDSEL1	
2	HDSEL0	
1	USEL1	Disk unit address; USEL1, USEL0 = 00 selects unit 0; =1 selects unit 1; etc.
0	USEL0	

A6 Port C, Input

Bit	Mnemonic	Meaning/Use
7	BUSY	0 during seek operation and during read/write until start of transfer from/to disk.
6	INTE	1 = interrupt enabled
5	TRACK0	0 = the selected disk's heads are positioned over cylinder 0.
4	FAULT	0 = the selected disk senses a fault and will not write or step.
3	INTR	1 = interrupt at completion of disk read, write, or seek.
2	SEEKCMP	0 = the selected disk's heads are positioned and ready to read or write (seek complete)
1	SELECTED	0 = a disk unit is responding to the unit select address (Port B).
0	READY	With SEEKCMP, 0 = the selected disk is ready to seek, read, or write.

A7 Output Mode and Interrupt Control

Four functions are performed with outputs to address A7. The functions are defined by the data byte written, described below.

Byte (hex)	Function
A9	Mode set, after power on or reset
0F	Reset BUSY, immediately after mode set
0D	Enable Interrupt

0C Disable Interrupt

OPERATIONS

Mode Set

Mode set and initialization of the controller is accomplished as follows:

```
INIT:   LD    A,0A9H
        OUT   (0A7H),A      ; set mode of 8255 (Port A output mode 1,
        LD    A,0FH             Port B output mode 0, Port C input)
        OUT   (0A7H),A      ; reset busy
```

Seek

The algorithm for a seek operation is as follows:

```
SEEKOUT: LD   A,NUMCYL      ; get number of cylinders to move
         ADD  A             ; double it for 2 steps per cylinder
         DEC  A             ; subtract 1
         OUT  (0A1H),A      ; set LS byte of counter
         XOR  A
         OUT  (0A2H),A      ; zero MS nibble of counter
         LD   A,20H         ; get step out command
         OUT  (0A4H),A      ; step out
         LD   A,0DH         ; get enable interrupt command
         OUT  (0A7H),A      ; enable controller's interrupt
```

Write

The write operation sends one sector of data from the controller's data buffer to the currently addressed cylinder on the selected disk unit.

The first four data bytes contain cylinder, head, and sector identification ("header") for use by the program in verifying correct positioning of head and sector selection. The program must place these "header" bytes in the buffer, along with the 512 data bytes. When writing to the disk, the controller will append the four ECC bytes to the

end of the data for a total information record of 520 bytes.

During the write, the controller is accessing the data buffer and using the buffer address counter. The program should not attempt to access these functions while the write is in progress.

Read

The read operation transfers one sector of data from the selected disk unit to the controller's data buffer. The head and unit to perform the read are selected by bits 0-4 of I/O Port B, I/O address A5.

With read initiation, the controller finds the desired sector, then reads 516 bytes from the sector to the data buffer, then places the result of the ECC value comparison into 5 bytes of the data buffer, then waits for end of sector. At end of sector, the controller sets Interrupt and goes not busy.

During the read, the controller accesses the data buffer using the buffer address counter. Neither the data buffer nor the address counter should be accessed by the program while the read is in progress.

If the ECC value result indicates no error detected, then the header should be verified prior to accepting the 512 data bytes.

Error Correction

Best error performance occurs when correction is applied only to hard errors; therefore 5 read retries are performed when a non- zero ECC is detected in order to recover soft errors. If the record cannot be recovered by retries, then the program attempts to correct the error using the ECC data.

Error patterns that span more than 8 bits exceed the capability of the code and are not correctable. Errors of less than 8- bit spans are corrected by the program.

Interrupts

The controller's interrupt is assigned to Interrupt Level 4. Provision is made to reassign the controller to Interrupt Level 1, 2, 3, 5, or 6.

Three events cause interrupt: termination of a disk read or write operation and termination of a seek operation when the disk sets its "Seek Complete" signal.