21MX Computer Series

Operator's Manual

HEWLETT hp PACKARD

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, 95014

PART NO. 02108-90004

Printed in U.S.A. 7/75

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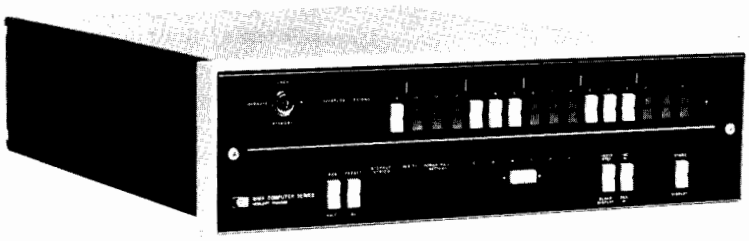
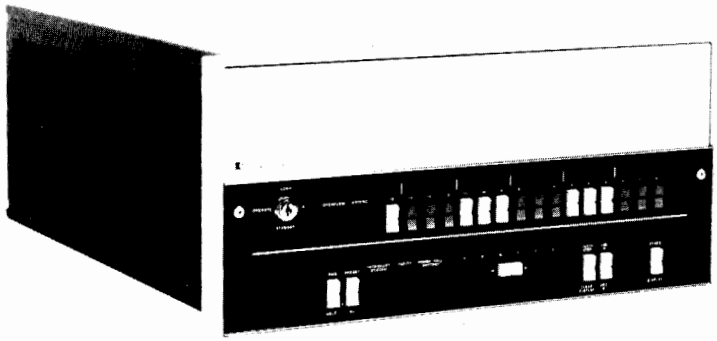


HP 2105A



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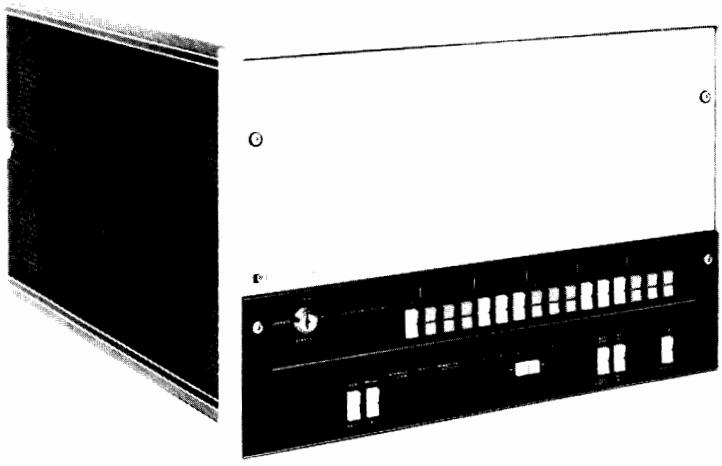

HP 2112A

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Figure 1. HP 21MX Computer Series

INTRODUCTION

This manual provides operator information for the HP 21MX Computer Series which are configured around the HP 2105A, HP 2108A, and HP 2112A Microprogrammable Processors illustrated in figure 1. Included in this manual are a list of the supporting documentation available; descriptive information for each control, connector, indicator, and fuse located on the operator or rear panel of the processor; basic operating procedures for the computer; and a list of halt codes and abnormal indications to aid the operator when one of these conditions exists.

SUPPORTING DOCUMENTATION

The following manuals may be ordered from a Hewlett-Packard Sales and Service Office. Sales and Service Offices are listed at the back of this manual.

a. HP 21MX Computer Series Reference Manual, part no. 02108-90002.

b. HP 21MX Computer Series Installation and Service Manual, part no. 02108-90006.

c. Microprogramming HP 21MX Computers Operating and Reference Manual, part no. 02108-90008.

OPERATOR PANEL

Figure 2 illustrates the location of each operator panel control and indicator and the following paragraphs describe their functions when used in the normal register display mode. For information on their use in the special register display mode, refer to the Operating Procedures section of this manual. Since the function of each is exactly the same as the function of those located on the operator panel of the HP 2105A and HP 2112A Microprogrammable Processors, only the HP 2108A Microprogrammable Processor is illustrated.

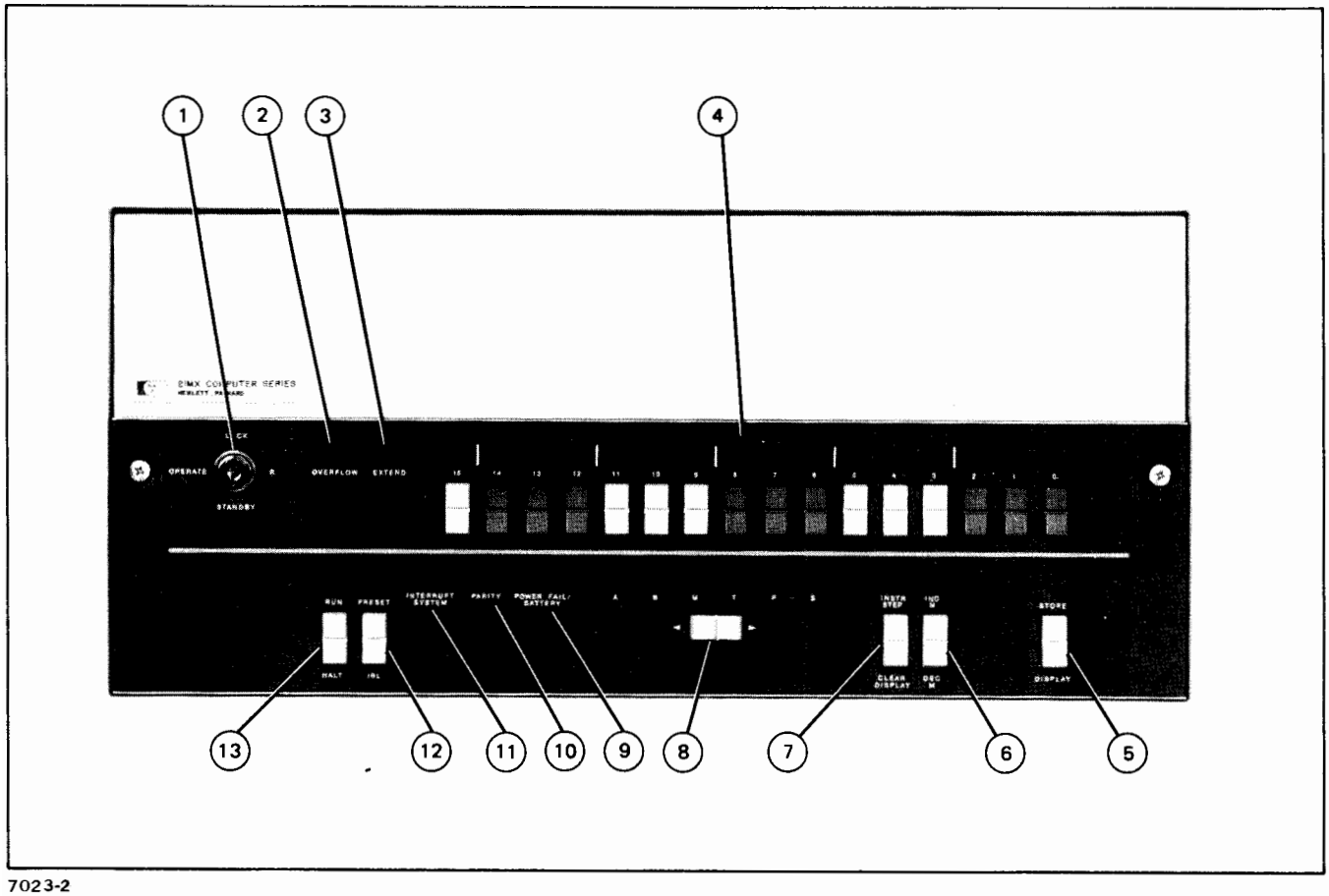

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Figure 2. Operator Panel Controls and Indicators

(1) **STANDBY/OPERATE/LOCK/R** — this four-position, key-operated switch selects one of four computer operating conditions as follows:

a. When set to the STANDBY position, the memory contents are sustained, the battery is charged, and CPU and I/O power is off. I/O interface printed circuit assemblies (PCA's) may be removed or installed without causing any damage to them, the processor, or the operator. If the optional power fail recovery system is installed and operative, the memory contents will be sustained for a minimum of 2 hours in the event of a power failure. The key is removable in this position.

b. When set to the OPERATE position, power is applied to the entire processor mainframe. The key is not removable in this position.

c. When set to the LOCK position, the RUN/HALT switch is disabled and all other processor functions are enabled (within the constraints of the run or halt mode of operation). The key is removable in this position.

d. When momentarily set to the R(reset) position after a prolonged power failure, memory power is restored and the POWER FAIL/BATTERY light is on. The switch, when released, will automatically return to the STANDBY position. The key is not removable in the R (reset) position.

(2) **OVERFLOW** — this light continuously displays the contents of the overflow register when the processor is in the run or halt mode.

A '1' is indicated when the light is on and a '0' is indicated when the light is off.

(3) **EXTEND** — this light continuously displays the contents of the extend register when the processor is in the run or halt mode.

A '1' is indicated when the light is on and a '0' is indicated when the light is off.

(4) **Display Register** — this combination of 16 two-position, momentary-contact, rocker switches and associated lights control and display the contents of the selected working register (A, B, M, T, P, or S) when the processor is in the halt mode. Only the contents of the S-register are displayed when the processor is in the run mode.

A '1' is indicated when the associated light is on and a '0' is indicated when the associated light is off. Pressing the upper half of the switch sets the corresponding bit to a '1', while pressing the lower half of the switch sets the corresponding bit to a '0'.

The Display Register is cleared to all zeros during the run or halt mode when CLEAR DISPLAY is pressed.

(5) **STORE/DISPLAY**— this two-position, momentary-contact, rocker switch causes the contents of the Display Register to be stored or displayed as follows:

a. When STORE is pressed during the halt mode, the contents of the Display Register are stored in the selected working register.

   If the T-register is selected when STORE is pressed, the contents of the Display Register are loaded into memory cell 'm', the contents of the M-register are automatically incremented to 'm+1', and the contents of the Display Register remain the same. This latter feature permits the same data to be loaded in consecutive locations in memory.

   If any other register is selected, only that register will be updated when STORE is pressed.

b. When DISPLAY is pressed during the halt mode, the current contents of the selected working register are placed into the Display Register. This feature is used to recall a register after the contents of the Display Register have been changed or to display the new contents of the T-register after STORE is pressed.

(6) **INC M/DEC M** — this two-position, momentary-contact, rocker switch increments and decrements the contents of the M-register as follows:

a. When INC M is pressed during the halt mode, the contents of the M-register are incremented by one.

b. When DEC M is pressed during the halt mode, the contents of the M-register are decremented by one.

Incrementing or decrementing the contents of the M-register occurs even when the M-register is not displayed.

(7) **INSTR STEP/CLEAR DISPLAY** — this two-position, momentary-contact, rocker switch advances the program to the next instruction and clears the Display Register as follows:

a. When INSTR STEP is pressed during the halt mode, the current instruction is executed and the program counter is advanced to the next instruction. With the T-register selected, the contents of the current instruction will be displayed in the Display Register. If any other register is selected, only the contents of the selected register will be displayed. Thus, if the current instruction is a halt instruction, the halt code will not be displayed. Also, if the T-register light comes on when the INSTR STEP switch is released, infinite indirect addressing is indicated. In this case, the program counter will not be advanced.

b. When CLEAR DISPLAY is pressed during the run or halt mode, the contents of the Display Register are cleared, i.e., the contents becomes 000000 (octal).

(8) **◂Register Select▸** — this combination of a two-position, momentary-contact, rocker switch and six lights selects and indicates one of the six working registers when the processor is in the halt mode. The register currently selected for display in the Display Register is indicated when the light associated with the selected register is on.

Pressing the left-hand half of this switch (◄) causes the next light to the left of the currently selected register to be on, which indicates that the associated register is now selected for display and modification. Similarly, pressing the right-hand half of this switch (►) causes the next light to the right of the currently selected register to be on, which indicates that the associated register is now selected for display and modification.

A wraparound feature is included so that when the A-register is selected and the left-hand half of this switch (◄) is pressed, the S-register will be selected for display. Similarly, when the S-register is selected and the right-hand half of this switch (►) is pressed, the A-register will be selected for display.

After a programmed or manual halt, the T-register is automatically selected for display. In the case of a programmed halt, the halt instruction will be displayed. In the case of a manual halt, the contents of the last accessed memory cell will be displayed. The light that corresponds to the T-register will be on to indicate that the contents of the T-register are being displayed.

(9) **POWER FAIL/BATTERY** — this light is turned on when power is restored after a power failure provided that the power fail/automatic restart feature is enabled.

Pressing HALT, then PRESET or executing an STC 04 or CLC 04 instruction will turn this light off.

This light will also flash on and off if the processor is equipped with the optional power-fail recovery system and battery is not charged to a sufficient level to sustain the memory contents for at least 2 hours, the BATTERY ON/OFF switch is set to OFF, or the battery is not connected.

Note: The battery is completely discharged before shipment. Upon initial application of power, or upon restoration of power after a prolonged power failure, the POWER FAIL/BATTERY light will flash on and off for approximately 16 hours until the battery is sufficiently charged to sustain memory. The battery level is sampled every seven minutes, so sufficient time must be allowed for the light to be turned off once corrective action is taken.

(10) **PARITY** — this light, when on, indicates that a parity error occurred while reading from memory.

In the halt mode, this light can be turned off by pressing PRESET.

With the memory protect option installed (HP 2108A only) and the parity error interrupt system enabled, this light is automatically turned off by a parity error interrupt and is therefore not ordinarily on long enough to be visible.

(11) **INTERRUPT SYSTEM** — this light indicates the status of the interrupt system. When on, it indicates that the interrupt system is enabled and when off, it indicates that the interrupt system is disabled.

(12) **PRESET/IBL** — this two-position, momentary-contact, rocker switch disables, the interrupt system, resets the power-fail logic, clears the parity and/or overflow bits, and loads the contents of the paper tape or optional loader read-only-memory (ROM) as follows:

a. When PRESET is pressed during the halt mode, the interrupt system is disabled, power-fail logic is reset, and the parity and/or overflow bits are cleared (if set).

   The function of the power fail/automatic restart feature will be overridden when PRESET is pressed during recovery from a power failure.

b. When IBL is pressed, the contents of the paper tape or optional loader ROM are written into the uppermost 64 locations in the first 32K of directly addressable memory. Bits 15 and 14 of the S-register select the desired loader as listed in table 1.

Table 1. Loader Selection

BIT		LOADER SELECTED
15	14	
0	0	Paper Tape Loader
0	1	Optional Loader #1
1	0	Optional Loader #2
1	1	Optional Loader #3

Bits 6 through 11 of the S-register must be set to the octal select code of the loading device. The function of the remaining bits is discussed in the procedure associated with the individual loader.

(13) **RUN/HALT** — this combination of a two-position, momentary-contact, rocker switch and associated light controls and indicates the run and halt modes of operation as follows:

a. When RUN is pressed, the run mode is selected, the associated light is on, the processor begins the programmed operation, and all other operator panel controls are disabled with the exception of the Display Register, CLEAR DISPLAY, and HALT switches.

   During the run mode, the contents of the S-register are automatically selected for display in the Display Register and none of the other registers can be selected. Therefore, the Display Register effectively becomes the S-register and it can be directly addressed as I/O select code 01 (octal) by the program.

b. When HALT is pressed, the associated light is turned off at the end of the current machine cycle. All operator panel controls are enabled and the T-register is automatically selected for display. If the halt was caused by a parity error or by pressing HALT, the contents of the last accessed memory cell will be displayed. If the halt was caused by the program, the halt instruction will be displayed.

The functions of the RUN/HALT switch are disabled when the STANDBY/OPERATE/LOCK/R switch is set to the LOCK position.

REAR PANEL (HP 2105A AND HP 2108A)

Figure 3 illustrates the location of each rear panel control, connector, and fuse and the following paragraphs describe their functions. Since the function of each is exactly the same as the function of those located on the rear panel of an HP 2105A Microprogrammable Processor, only the HP 2108A Microprogrammable Processor is illustrated.

(1) **Battery (optional)** — this 12-volt battery, which is part of the optional power fail recovery system, will sustain a 32K memory for a minimum of 2 hours in the event of a power failure. The battery must be fully charged and connected to the BAT. INPUT connector, the BATTERY ON/OFF switch must be set to ON, F2 must be intact, and the memory sustaining circuitry must be installed and operative for this feature to function properly. This feature also permits the processor mainframe to be transported from one location to another without being connected to an ac power source, provided that the transportation time does not exceed the 2-hour battery capacity.

(2) **F2** — this 5-ampere, 250-volt fuse provides protection for the memory sustaining circuitry. It also provides protection for the optional battery while it is being charged.

(3) **BATTERY ON/OFF** — this two-position slide switch controls the application of current from the optional battery to the memory sustaining circuitry.

(4) **PWR CONT** — this nine-pin connector provides the means to connect an external memory extender (HP 2108A only), I/O extender, or satellite computer to the main computer. When connected, these units are controlled by the STANDBY/OPERATE/LOCK/R switch located on the main computer. A power failure or error condition in any one of the units will cause all of the units to cease operation until the cause of the power failure or error condition has been corrected.

(5) **BAT. INPUT** — this two-pin connector provides the means to connect the optional battery to the memory sustaining circuitry.

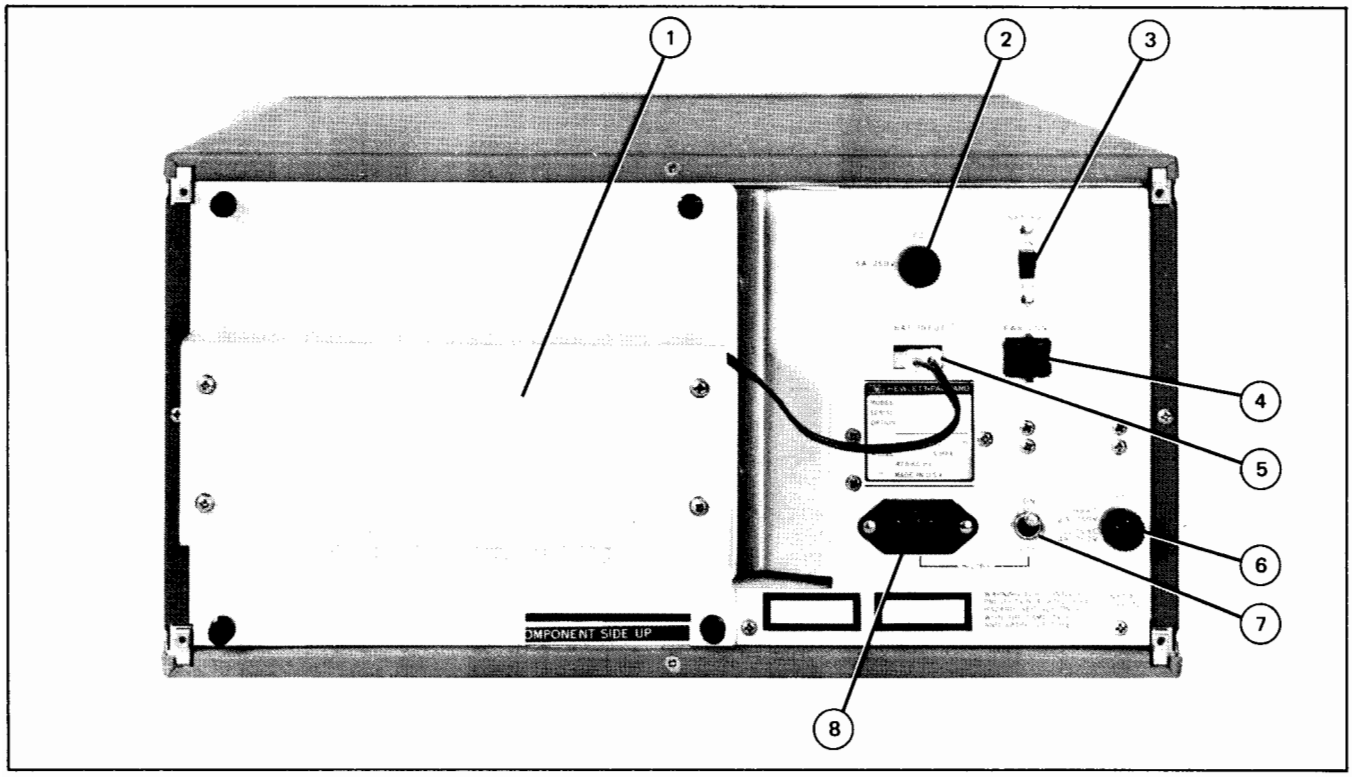

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Figure 3. Rear Panel Controls, Connectors, and Fuses

(6) **F1** — this fuse provides protection from an ac power line overload. The current and voltage ratings of the fuse required are listed in table 2.

Table 2. Fuse Ratings

MODEL	REQUIRED FUSE RATING	
	110 Vac, 60 Hz	220 Vac, 60 Hz
HP 2105	4A, 250V	2A, 250V
HP 2108	6A, 250V	4A, 250V

(7) **~LINE ON/OFF** — this two-position toggle switch controls the application of ac power to the processor power supplies and ventilating fans.

(8) **~LINE Connector** — this three-input power line connector provides the means to connect an ac power source to the processor.

REAR PANEL (HP 2112A)

Figure 4 shows the rear panel of the HP 2112A Processor. The functional descriptions of the rear panel controls, connectors, and fuses given in the preceding paragraphs are applicable to the HP 2112A except as noted below.

F1 — this 1-ampere, 250-volt fuse provides protection for part of the memory sustaining circuitry.

F2 — this 3-ampere, 250-volt fuse provides protection for part of the memory sustaining circuitry. It also provides protection for the optional batteries while they are being charged.

On the HP 2112A, the optional batteries can be mounted on the rear panel in the same position as shown in figure 3 for the HP 2108A. The batteries are part of the optional power fail recovery system and will sustain a 128K memory for a minimum of two hours in the event of a power failure. In order for this feature to function properly, both batteries must be fully charged and connected to the two BAT. INPUT connectors, the BATTERY ON/OFF switch must be set to ON, both F1 and F2 must be intact, and the memory sustaining circuitry must be installed and operative.

PWR CONT IN and PWR CONT OUT — these nine-pin connectors provide the means to connect an external memory extender and an I/O extender or a satellite computer, or two I/O extenders or satellite computers, or one I/O extender and one satellite computer. Each of these connectors is the same as the PWR CONT connector shown in figure 3.

LINE ON/OFF — this two-position circuit breaker controls the application of ac power to the processor power supplies and ventilating fans and provides protection from an ac power line overload.

OPERATING PROCEDURES

The following procedures describe the startup sequence; how to initialize memory; how to load programs manually; how to load programs using paper tape, disc, magnetic tape, or other such media; how to verify and run programs; and how to enter the special register display mode. Each procedure requires that the following conditions be met.

a. The ~LINE ON/OFF switch, located on the processor rear panel, must be set to ON.

b. The processor must be connected to a suitable ac power source and the proper fuse (F1) must be installed.

Two additional procedures are provided which outline the shutdown sequence and describe how to exchange I/O interface PCA's.

STARTUP PROCEDURE

Use the following procedure to return the processor to operating status from a standby condition.

a. Set the key-operated switch to the OPERATE position.

   If none of the operator panel lights are on but the fans are operating or if all six ◄Register Select► lights are on, set the key-operated switch first to the R(reset) position; then to the STANDBY position; then finally to the OPERATE position. (The contents of the memory will be sustained during this operation).

   If none of the operator panel lights are on and the fans are not operating, check to ensure that ac power is available and that the ~LINE ON/OFF switch is set to ON. If the processor is housed in a system cabinet, also ensure that the system power switch is set to provide ac power.

b. Load the contents of the paper tape or optional loader ROM, as desired, using the procedures provided in this manual.

INITIALIZING MEMORY

To clear memory including the A- and B-registers (memory cells 000000 and 000001, respectively) and to restore parity, proceed as follows:

a. Set the key-operated switch to the STANDBY position.

b. If the processor is equipped with the optional power fail recovery system, set the BATTERY ON/OFF switch to OFF.

c. Set the ~LINE ON/OFF switch to OFF.

d. After waiting for approximately 1-second, set the ~LINE ON/OFF switch to ON.

e. Set the BATTERY ON/OFF switch to ON.

f. Set the key-operated switch first to the R(reset) position; then to the STANDBY position; then finally to the OPERATE position.

All of the Display Register lights will be on for approximately 1-second during which time the memory is cleared. When the cycle is complete, the contents of the T-register are automatically selected for display. The contents of the T-, A-, B-, P-, and M-registers will be as follows:

T-register = 000000 (octal)
A-register = 000000 (octal)
B-register = 000000 (octal)
P-register = 100000 (octal)
M-register = 077777 (octal)

If so desired, the contents of these registers may be verified by pressing ◄Register Select►, as required.

LOADING PROGRAMS MANUALLY

Programs may be manually loaded from the operator panel, if so desired. Use the following procedure:

a. Press ◄Register Select►, as required, to select the M-register for display in the Display Register. The light associated with the M-register will be on once the M-register is selected.

b. Change the contents of the Display Register to the desired binary starting address of the program to be loaded. It may be faster to press CLEAR DISPLAY and begin from an all-zero display.

c. Press STORE to store the contents of the Display register in the M-register.

d. Press ◄Register Select►, as required, to select the T-register for display in the Display Register. The light associated with the T-register will be on once the T-register is selected.

e. Change the contents of the Display Register to the binary instruction code of the first instruction of the program to be loaded. It may be faster to press CLEAR DISPLAY and begin from an all-zero display.

f. Press STORE to store the contents of the Display Register in the T-register. Pressing STORE with the T-register selected automatically causes the contents of the M-register to be incremented by one, which is the

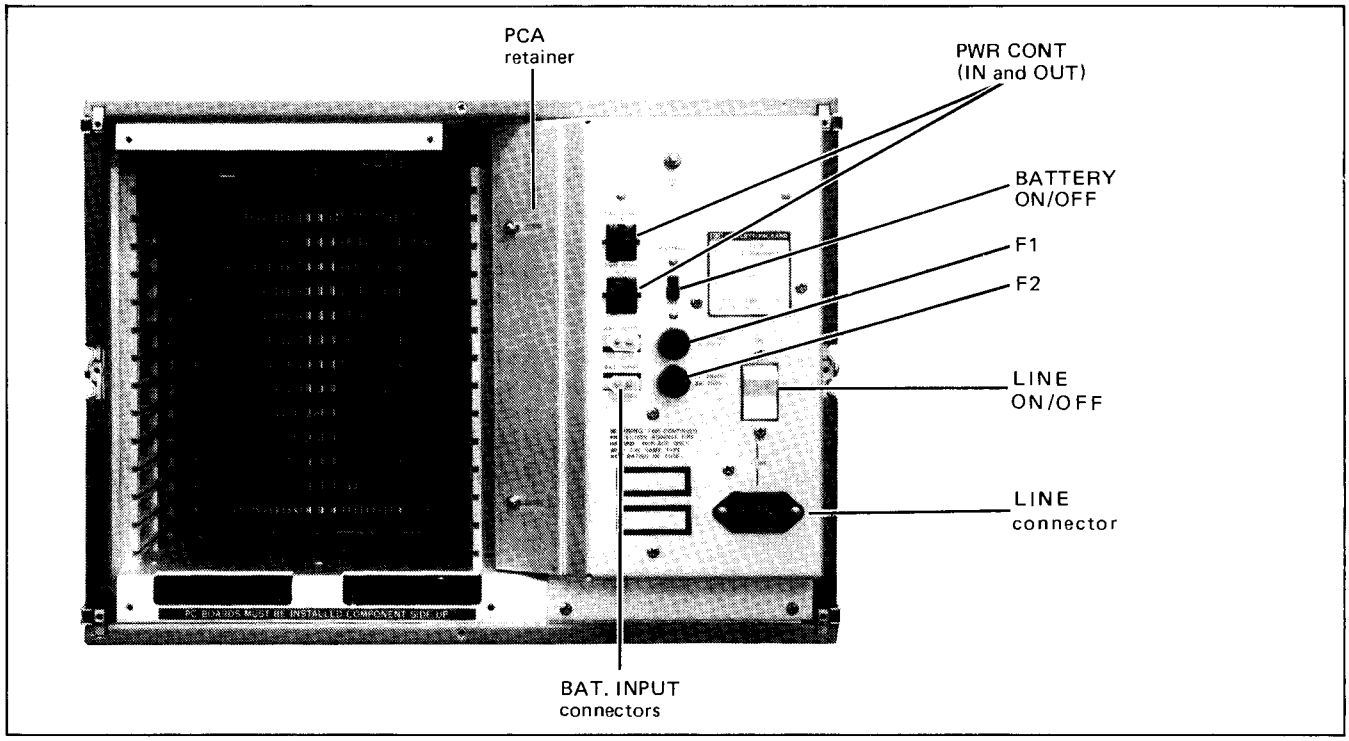

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Figure 4. HP 2112A Microprogrammable Processor - Rear Panel

address of the next instruction to be loaded. The contents of the Display Register are not changed. This feature permits the same data to be loaded into consecutive locations in memory. The current contents of memory cell 'm' can be recalled for verification by pressing DISPLAY.

g. Repeat steps e and f until the entire program has been loaded.

LOADING PROGRAMS FROM A PAPER TAPE READER

The following procedures should be used when loading programs from a paper tape reader. The contents of the paper tape loader ROM must be loaded into memory before programs can be loaded.

LOADING THE PAPER TAPE LOADER. Use the following procedure to load the contents of the paper tape loader ROM into memory.

At the operator panel of the processor, perform the following:

a. Press ◄Register Select►, as required, to select the S-register for display in the Display Register. The light associated with the S-register will be on once the S-register is selected.

b. Press CLEAR DISPLAY to clear the contents of the Display Register. Since bits 15 and 14 are cleared at this time, the paper tape loader ROM will be selected.

c. Change bits 6 through 11 of the Display Register to the octal select code of the paper tape reader. Pressing the upper half of the corresponding Display Register switch sets that bit to a '1' (the associated light will be on), while pressing the lower half of the switch sets that bit to a '0' (the associated light will be off).

   Since bits 0 through 5, 12, and 13 are not used in conjunction with the paper tape loader, they are ignored.

d. Press STORE to store the contents of the Display Register in the S-register.

e. Press IBL to load the contents of the paper tape loader ROM into the uppermost 64 locations in the first 32K of directly addressable memory.

   A successful load is indicated if the OVERFLOW light remains off. An unsuccessful load is indicated if the OVERFLOW light is on; this will occur if the select code programmed in step c was less than 10 (octal) or if a memory hardware fault is detected.

LOADING PROGRAMS. Use the following procedure to load programs from the paper tape reader into memory. Programs must be in binary form and must contain absolute addresses. It is assumed that the contents of the paper tape loader ROM have been previously loaded in memory and that the paper tape reader has been properly prepared for reading before performing these steps.

At the operator panel of the processor, perform the following:

a. Press ◄Register Select►, as required, to select the P-register for display in the Display Register. The P-register contains the address of the first instruction associated with the paper tape loader. This address will depend upon the size of the memory being used. These starting addresses and corresponding memory sizes are listed in table 3. (This step is included for program reference information only and may be omitted, if so desired).

Table 3. Starting Address Vs. Memory Size

MEMORY SIZE	STARTING ADDRESS (in octal) OF THE PAPER TAPE LOADER
4K	007700
8K	017700
12K	027700
16K	037700
24K	057700
32K	077700

b. Press PRESET to initialize the computer.

c. Press RUN to start the paper tape loader program. The associated light will be on and the program will be loaded from the paper tape reader into memory.

   When the processor halts, the associated light will be turned off and the T-register will automatically be selected for display in the Display Register. A successful program load is indicated if the contents of the Display Register are 102077 (octal). If the halt code displayed is not 102077 (octal), one of two possible error condition halt codes will be displayed. If the halt code displayed is 102055 (octal), an address error is indicated. Check to ensure that the proper tape was used or that the tape was not installed backwards. If the halt code displayed is 102011 (octal), a checksum error is indicated. Check for a possible defective or dirty tape or tape reader.

LOADING PROGRAMS FROM OTHER LOADING DEVICES

The following procedures should be used when loading programs from a disc, magnetic tape, or other such media. The contents of the optional loader ROM, associated with the loading device, must be loaded before the program can be loaded. Locations have been provided within the processor to accommodate up to three optional loaders, i.e., optional loader #1, #2, and #3. Each of these loaders is used to control the loading of programs from a particular type of loading device. It is assumed that the optional loader ROM, associated with the loading device to be used, is installed in the processor and that its location is known.

LOADING AN OPTIONAL LOADER. Use the following procedure to load the contents of the associated optional loader ROM into memory.

At the operator panel of the processor, perform the following:

a. Press ◂Register Select▸, as required, to select the S-register for display in the Display Register. The light associated with the S-register will be on once the S-register is selected.

b. Press CLEAR DISPLAY to clear the contents of the Display Register.

c. Change bits 15 and 14 of the Display Register as listed in table 4 to select the optional loader that corresponds to the loading device to be used.

Table 4. Optional Loader Selection

BIT		LOADER SELECTED
15	14	
0	1	Optional Loader #1
1	0	Optional Loader #2
1	1	Optional Loader #3

d. Change bits 6 through 11 of the Display Register to the octal select code of the loading device to be used.

e. Change bits 0 through 5, 12, and 13 as outlined in the instructions included with the optional loader to be used.

f. Press STORE to store the contents of the Display Register in the S-register.

g. Press IBL to load the contents of the selected optional loader ROM into the uppermost 64 locations in the first 32K of directly addressable memory.

A successful load is indicated if the OVERFLOW light remains off. An unsuccessful load is indicated if the OVERFLOW light is on; this will occur if the select code programmed in step c was less than 10 (octal) or if a memory hardware fault is detected.

LOADING PROGRAMS. Use the following procedure to load programs from the loading device into memory. Programs must be in binary form and must contain absolute addresses. It is assumed that the contents of the associated optional loader ROM have been previously loaded in memory and that the loading device has been properly prepared for reading before performing these steps.

At the operator panel of the processor, perform the following:

a. Press ◂Register Select▸, as required, to select the P-register for display in the Display Register. The P-register contains the address of the first instruction associated with the selected optional loader. This address will depend upon the size of the memory being used. These starting addresses and corresponding memory sizes are the same as those listed in table 3. (This step is included for program reference information only and may be omitted, if so desired).

b. Press PRESET to initialize the computer.

c. Press RUN to start the loader program. The associated light will be on and the program will be loaded from the loading device into memory.

When the processor halts, the associated light will be turned off and the T-register will automatically be selected for display in the Display Register. A successful program load is typically indicated if the contents of the Display Register are 102077 (octal). Refer to the instructions included with each optional loader for the specific halt code used.

VERIFYING PROGRAMS

Programs may be verified after loading, if so desired. Use the following procedure:

a. Press ◂Register Select▸, as required, to select the M-register for display in the Display Register. The light associated with the M-register will be on once the M-register is selected.

b. Change the contents of the Display Register to the binary starting address of the program to be verified.

It may be faster to press CLEAR DISPLAY and begin from an all-zero display.

c. Press STORE to store the contents of the Display Register in the M-register.

d. Press ◄Register Select►, as required, to select the T-register for display in the Display Register. The light associated with the T-register will be on once the T-register is selected.

e. Verify that the binary instruction code displayed is as desired for the first programmed instruction.

f. Press INC M to increment the contents of the M-register by one and verify that the binary instruction code displayed is as desired for the next programmed instruction.

g. Repeat step f until all programmed instructions have been verified. Pressing DEC M permits the previous programmed instruction to be verified.

RUNNING PROGRAMS

To run a program after it has been loaded, proceed as follows:

a. Press ◄Register Select►, as required, to select the P-register for display in the Display Register. The light associated with the P-register will be on once the P-register is selected.

b. Change the contents of the Display Register to the binary starting address of the program to be run. It may be faster to press CLEAR DISPLAY and begin from an all-zero display.

c. Press STORE to store the contents of the Display Register in the P-register.

d. Press PRESET to initialize the computer.

e. Press RUN to start the program. The associated light will be on as long as the program is running.

If the key-operated switch is set to OPERATE, all operator panel controls are disabled with the exception of the Display Register, CLEAR DISPLAY, and HALT switches.

During the run mode, the contents of the S-register are automatically selected for display in the Display Register and none of the other registers can be selected. Therefore, the Display Register effectively becomes the S-register and it can be directly addressed as I/O select code 01 (octal) by the program.

If the key-operated switch is set to LOCK, the functions of the RUN/HALT switch are disabled. All other operator panel controls are enabled within the constraints of the run or halt mode of operation.

When the processor halts, the T-register is automatically selected and the contents of the last memory cell accessed are displayed in the Display Register.

ENTERING THE SPECIAL REGISTER DISPLAY MODE

The operator panel microcoded routines permit displaying and/or modifying the contents of the X- and Y-registers, scratch pad registers S3 through S12, counter register, central interrupt register, overflow register, extend register, and all of the optional Dynamic Mapping System (DMS) map registers. The six working registers are accessed, as previously described, in the normal register display mode. The other registers are accessed by entering the special register display mode.

To enter the special register display mode, proceed as follows:

a. Press ◄Register Select►, as required, to select the M-register for display in the Display Register. The light associated with the M-register will be on once the M-register is selected.

b. Press CLEAR DISPLAY to clear the contents of the Display Register.

c. Change bits 15 and 14 of the Display Register as listed in table 5 to select the desired register or DMS maps for display.

Note: Do NOT press STORE. If STORE is pressed, bit 15 will be lost since the M-register only stores bits 0 through 14. This feature prevents accidental entry into the special register display mode during normal operation.

d. Change the low order bits of the Display Register as listed in table 5 to select the desired register for display. The contents of the display form the register pointer.

Note: Again, do NOT press STORE.

e. Press the right-hand half of the ◄Register Select► switch (►) as if to select the T-register. The light associated with the T-register will be on, but in this case, the special register display mode will automatically be entered and the contents of the desired register will be displayed in the Display Register, rather than the T-register. The register pointer will be stored internally and bits 13 through 4 will be cleared in the process.

Once the special register display mode is entered, the register pointer will be displayed whenever the M-register light is on.

Table 5. Register Selection

REGISTER DESIRED	POINTER (15 14 ... 3 2 1 0)
X	1 0 ... 0 0 0 0
Y	1 0 ... 0 0 0 1
COUNTER	1 0 ... 0 0 1 0
S3	1 0 ... 0 0 1 1
S4	1 0 ... 0 1 0 0
S5	1 0 ... 0 1 0 1
S6	1 0 ... 0 1 1 0
S7	1 0 ... 0 1 1 1
S8	1 0 ... 1 0 0 0
S9	1 0 ... 1 0 0 1
S10	1 0 ... 1 0 1 0
S11	1 0 ... 1 0 1 1
S12	1 0 ... 1 1 0 0
CIR	1 0 ... 1 1 0 1
OVERFLOW	1 0 ... 1 1 1 0
EXTEND	1 0 ... 1 1 1 1
DMS MAPS	**POINTER (15 14 ... 6 5 4 3 2 1 0)**
SYSTEM	1 1 ... 0 0 MAP REG NO.
USER	1 1 ... 0 1 MAP REG NO.
PORT A	1 1 ... 1 0 MAP REG NO.
PORT B	1 1 ... 1 1 MAP REG NO.

Note: The contents of the M-register are not affected in the special register display mode unless STORE is accidently pressed.

In the special register display mode, pressing INC M with the M-register light on will increment the register pointer (all 16 bits) by one. Pressing DEC M will decrement only bits 0 through 7 of the register pointer by one. If bits 0 through 7 are all cleared when DEC M is pressed, they will all be set.

In the special register display mode, pressing INC M with the T-register light on will increment bits 0 through 3 of the register pointer by one. Pressing DEC M will decrement bits 0 through 3 of the register pointer by one.

If bits 15 and 14 are both "1", bits 0 through 6 are counted modulo 128 (the number of DMS map registers); if bit 15 is "1" and bit 14 is "0", bits 0 through 3 are counted modulo 16 (the number of displayable registers). If bits 0 through 3 are all cleared when DEC M is pressed, they will all be set. The register pointer will then be pointing to the extend register. Similarly, if bits 0 through 3 are all set when INC M is pressed, they will all be cleared. The register pointer will then be pointing to the X-register. This feature maintains the range of the register pointer within the number of accessible registers (16).

Table 6 lists the effect that each operator panel control will have while operating in the special register display mode and the various ways of re-entering the normal register display mode. Table 7 lists the way each register is displayed or altered in the special register display mode.

SHUTDOWN PROCEDURES

One of the following procedures should be used when the processor is shut down during periods of nonoperation. The first procedure should be used when it is necessary to sustain memory contents. The second procedure should be used when it is not necessary to sustain memory contents.

SHUTDOWN PROCEDURE (MEMORY SUSTAINED). Use the following procedure to shut down the processor when it is necessary to sustain memory contents during periods of nonoperation.

a. Ensure that ac power is available and that the ~LINE ON/OFF switch is set to ON. If the processor is housed in a system cabinet, also ensure that the system power switch is set to provide ac power to the computer.

b. Set the key-operated switch to the STANDBY position. When set to this position, the memory contents are sustained by the internal power supply, a trickle charge is applied to the battery, and CPU and I/O power is off. In the event of a power failure, the contents of memory would be lost. However, if the optional power fail recovery system is installed and operative, the memory contents would be sustained for a minimum of 2 hours.

SHUTDOWN PROCEDURE (MEMORY NOT SUSTAINED). Use the following procedure to shut down the processor when it is not necessary to sustain memory contents during extended periods of nonoperation.

a. Set the key-operated switch to the STANDBY position.

b. If the processor is equipped with the optional power fail recovery system, set the BATTERY ON/OFF switch to OFF to prevent the optional battery from discharging.

c. Set the ~LINE ON/OFF switch to OFF or if the processor is housed in a system cabinet, set the system power switch to remove ac power. All memory contents will be lost during this operation.

Table 6. Special Register Display Mode Control Operations

SELECTED FOR DISPLAY	SWITCH PRESSED	EFFECT
T	*▶	Register Select "dot" shifts to "P". P-register contents are displayed and special register display mode is terminated.
T	◀	Register Select "dot" shifts to "M". Pointer is displayed per figure 2-2.
T	DISPLAY	Contents of register selected by pointer are displayed per table 2-3. Pointer is unchanged.
T	STORE	Register selected by pointer is loaded with data per table 2-3.
T	INC M	Pointer is incremented by one. Contents of register selected by new pointer value are displayed per table 2-3.
T	DEC M	Pointer is decremented by one. Contents of register selected by new pointer value are displayed per table 2-3.
T	*PRESET	Same as for normal register display mode except display is left unaltered; special register display mode is terminated. (The M-register is displayed if "M" is selected by pressing ◀.)
T	*IBL	Same as normal register display mode; special register display mode is terminated. Contents of last referenced memory address are displayed.
T	*INSTR STEP	Executes the next machine instruction; special register display mode is terminated. Contents of last referenced memory address are displayed.
M	▶	Register Select "dot" shifts to "T". Special register select mode is entered (only if bit 15 = 1) and contents of register selected by pointer are displayed.
M	*◀	Register Select "dot" shifts to "B" and contents of B-register are displayed. Special register display mode is terminated.
M	DISPLAY	Contents of the pointer are restored to the display. This is useful for checking the pointer after the display has been changed by the operator.
M	*STORE	Contents of the display are stored into the M-register. Bit 15 is cleared and the special register display mode is terminated.
M	INC M	Pointer is incremented and displayed.
M	DEC M	Low-order bits of pointer are decremented modulo 256_{10} and displayed.
M	*PRESET	Preset is performed. Special register display mode is terminated but display is unchanged. (Special register display mode may be reentered by pressing ▶.)
M	*IBL	Same as normal register display mode except M-register contents are displayed and special register display mode is terminated.
M or T	*RUN	Same as normal register display mode; special register display mode is terminated.
M	*INSTR STEP	Executes the next machine instruction; special register display mode is terminated. Latest value of M-register (last referenced memory address) is displayed.

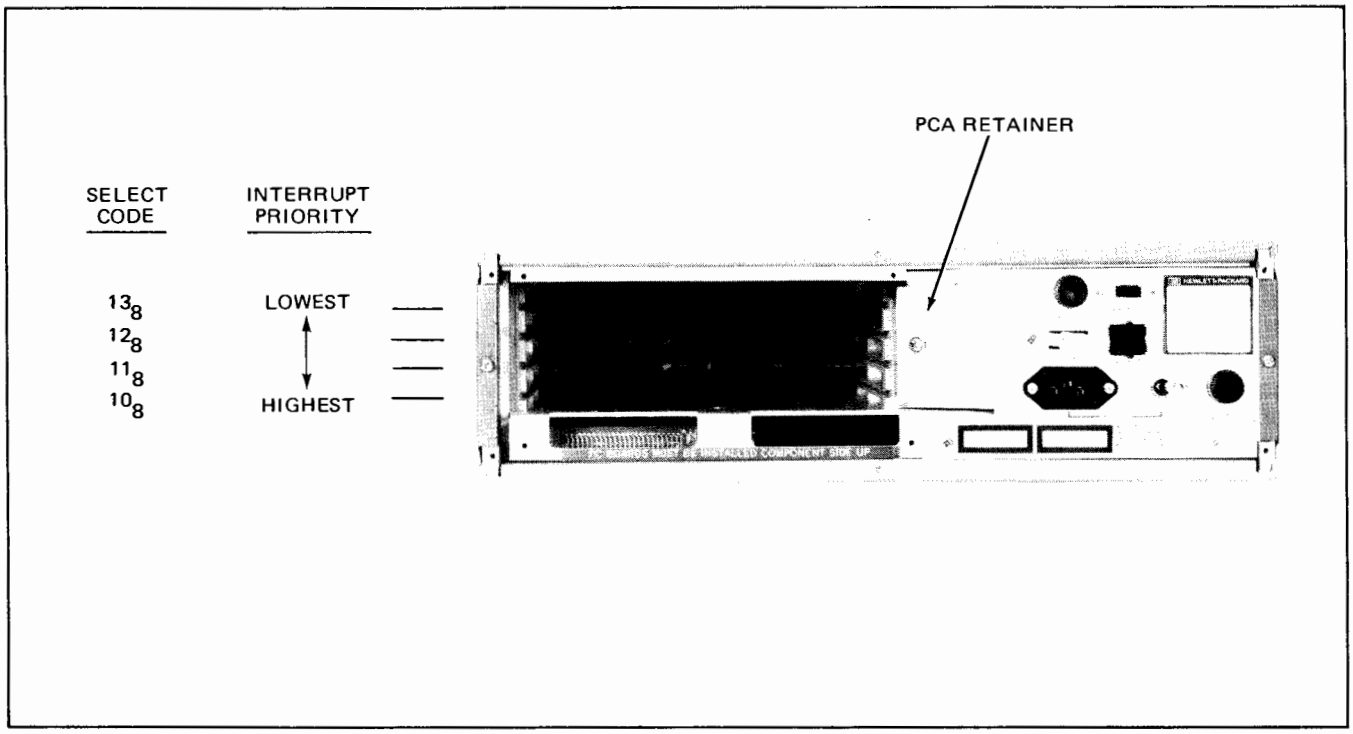
*Indicates conditions that terminate special register display mode.

Table 7. Effects of Displaying and/or Altering Selected Registers

REGISTER	SELECTED BY DISPLAY, INC M, DEC M, ▶	IF STORE PRESSED WHILE SELECTED
X, Y, S3-S12	Contents of selected register (16 bits) displayed.	Contents of display are loaded into selected register. The display is not altered.
Counter	Counter state is displayed modulo 256_{10} in bits 7-0. Bits 15-8 are all ones.	Bits 7-0 of display are loaded into counter. The display is not altered.
Central Interrupt Register (CIR)	Current contents of CIR are displayed in bits 5-0 (the octal select code of the device that last interrupted the processor). The contents of the CIR are unaffected. If Memory Protect is installed, it should be noted that displaying the contents of the CIR will be considered a violation because an I/O type instruction is simulated.	The CIR is loaded with the octal select code of any device that is requesting service. This feature should be used with caution because when this select code is displayed, an IAK (interrupt acknowledge) is issued to stop that device from interrupting. The display will be 00_8 if no device is requesting service.
Overflow and Extend	Display will be 177777_8.	Set bit 0 to the desired state and press STORE. The overflow or extend register will be set equal to bit 0 of the display. The display is not altered.
DMS Map Register	The contents of the map register indicated by bits 6-0 of the pointer are displayed. Bits 9-0 of the display indicate the memory page number. If bit 15 = 1, that page is read-protected; if bit 14 = 1, that page is write-protected. If DMS is not installed, the display will be 177777_8.	The contents of the display are stored into the map register indicated by bits 6-0 of the pointer in the same format as described at left. The display is not altered. Read and write protection may be set with bits 15 and 14, respectively.

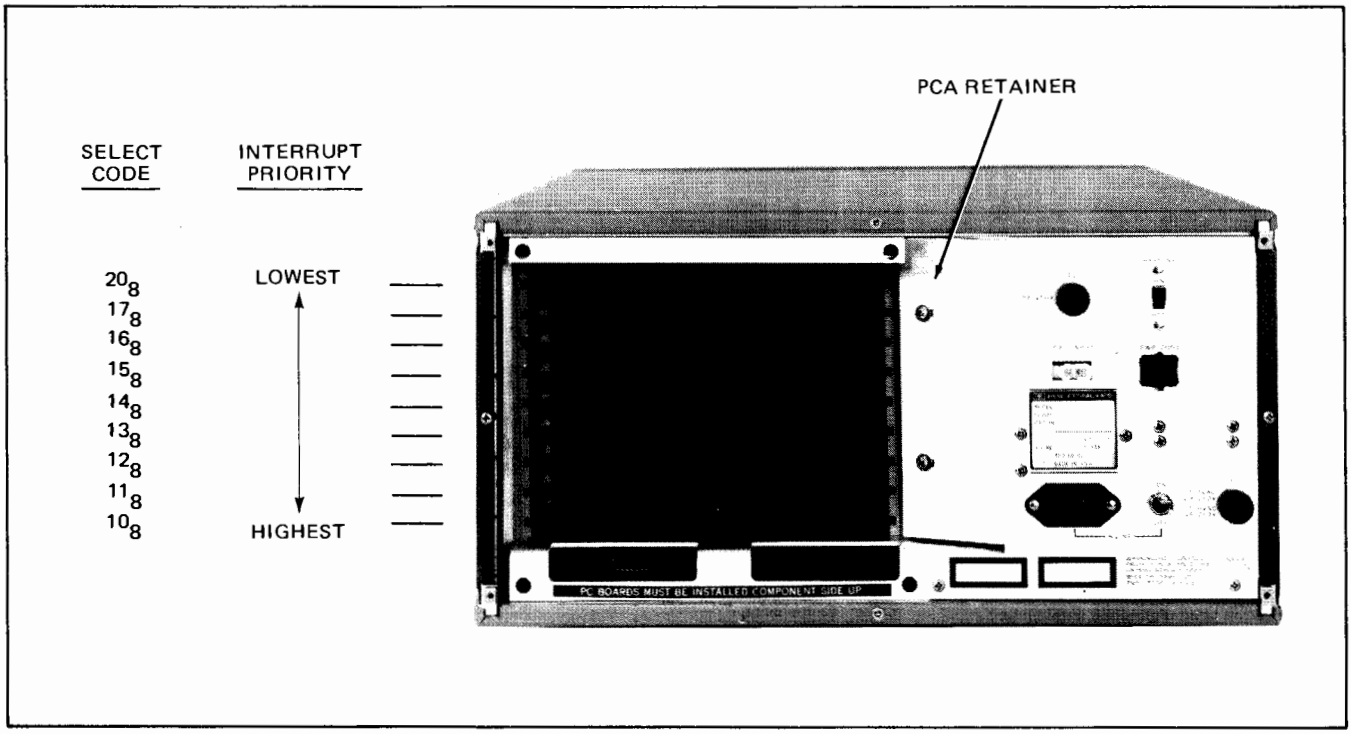
EXCHANGING I/O INTERFACES

Provisions have been made to accommodate up to four I/O interface PCA's in an HP 2105A, up to nine in an HP 2108A, or up to 14 in an HP 2112A. In either case, the location of an I/O interface PCA determines the priority by which the associated device interrupts will be serviced by the processor. Figures 5, 6, and 7 show the location of the I/O slots in an HP 2105A, an HP 2108A, and an HP 2112A Microprogrammable Processor, respectively. Also shown are the select code and interrupt priority associated with each I/O slot.



7023-4

Figure 5. HP 2105A Microprogrammable Processor — I/O Section



7023-5

Figure 6. HP 2108A Microprogrammable Processor — I/O Section

When it becomes necessary to install a new I/O interface PCA or change the location of an existing one, proceed as follows:

Note: Do NOT set the ~LINE ON/OFF switch, located on the processor rear panel, to OFF and if the processor is housed in a system cabinet, do NOT set the system power switch to remove ac power because the power to the memory would be removed and its contents would be lost.

a. Set the key-operated switch to the STANDBY position to remove CPU and I/O power.

b. If the processor is equipped with the optional power fail recovery system, set the BATTERY ON/OFF switch, located on the processor rear panel, to OFF and remove the battery cable from the BAT. INPUT connector.

c. Remove the rear cover from the processor rear panel by loosening the four captive screws (HP 2105A) or pulling the four plungers (HP 2108A and HP 2112A). This provides access to the I/O section of the computer.

d. Loosen the screw (HP 2105A) or screws (HP 2108A and HP 2112A) that secures the PCA retainer to the processor rear panel and slide the PCA retainer to the right to permit installation or exchange of I/O PCA's, as required.

e. Install the new I/O interface PCA or exchange I/O interface PCA's, as required.

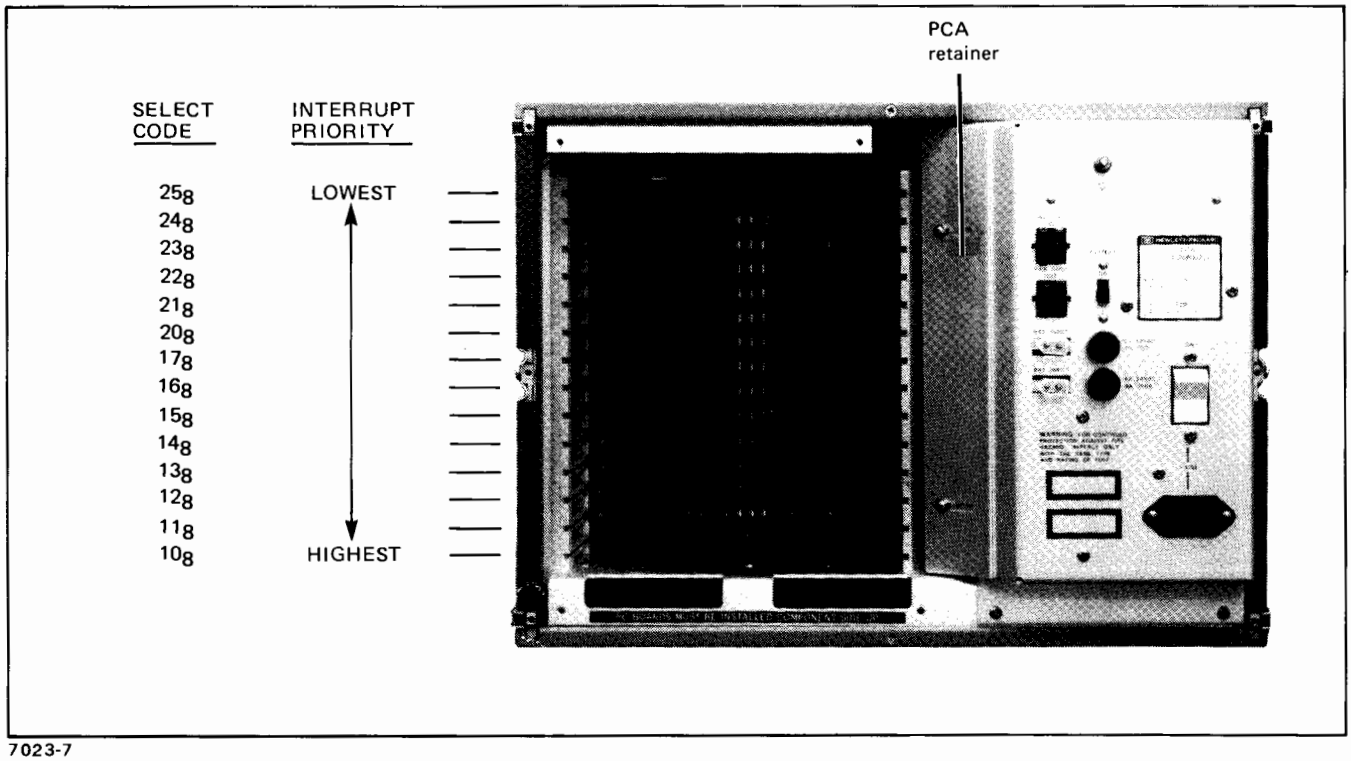
   If an HP 12979A I/O Extender is to be used, install its interface PCA in the first available, lowest priority I/O slot. Up to two of these units may be used with an HP 2105A, HP 2108A, or HP 2112A Microprogrammable Processor.

f. Replace the rear cover.

g. If the processor is equipped with the optional power fail recovery system, connect the battery cable to the BAT. INPUT connector and set the BATTERY ON/OFF switch to ON.

HALT CODES

Table 8 provides a quick reference to those halt codes associated with the paper tape loader. Also included is the halt code displayed when HALT is pressed, a parity error occurs, or a program halt instruction is encountered. These halt codes are displayed in the Display Register, when the processor is in the halt mode.



7023-7

Figure 7. HP 2112A Microprogrammable Processor - I/O Section

Table 8. Halt Codes

HALT CODE (in octal)	COMMENTS
102077	Indicates a successful program load from paper tape and typically indicates a successful program load from disc, magnetic tape, or other such media.
102055	Indicates that an address error occurred while loading from paper tape. Check to ensure that the proper tape was used or that it was not installed backwards.
102011	Indicates that a checksum error occurred while loading from paper tape. Check for a possible defective or dirty tape or tape reader.
XXXXXX	If the halt was manually caused by pressing HALT, the contents of the last accessed memory cell will be displayed. If the halt was caused by a parity error (PARITY light is on), the contents of the last accessed memory cell will be displayed. The displayed memory cell is not necessarily the memory cell that contained the parity error. If the halt was caused by the program, the halt instruction will be displayed.

ABNORMAL INDICATIONS

Table 9 provides a quick reference to the operator panel indications that occur when an abnormal condition exists during operation in the normal register display mode.

Table 9. Abnormal Indications

INDICATION	ABNORMAL CONDITION	REMEDY
POWER FAIL/BATTERY light remains on.	Indicates that power has been restored after a power failure and that the power fail/automatic restart feature is enabled.	Press HALT; then PRESET or execute an STC 04 or CLC 04 instruction.
POWER FAIL/BATTERY light flashes on and off. Note: The battery is completely discharged before shipment. Upon initial application of power, or upon restoration of power after a prolonged power failure, the POWER FAIL/BATTERY light will flash on and off for approximately 16 hours until the battery is sufficiently charged to sustain memory. The battery level is sampled every seven minutes, so sufficient time must be allowed for the light to be turned off once corrective action is taken.	Indicates that: a. The battery is not charged to a sufficient level to sustain the memory contents b. The BATTERY ON/OFF switch is set to OFF. c. The battery is not connected. d. The optional battery is defective.	a. Permit the battery to fully charge. b. Set the BATTERY ON/OFF switch to ON. c. Connect the battery to the BAT. INPUT connector. d. Call your local Hewlett-Packard Sales and Service Office for service.*
PARITY light is on.	Indicates that a parity error occurred while reading from memory.	Call your local Hewlett-Packard Sales and Service Office for service.*
OVERFLOW light is on after IBL is pressed.	Indicates that: a. The presence of memory was not detected. b. The programmed select code was less than 10 (octal). c. The memory was defective.	a. Check that memory modules are installed and programmed correctly. b. Check that the programmed select code is within range. c. Call your local Hewlett-Packard Sales and Service Office for service.*
*Hewlett-Packard Sales and Service Offices are listed at the back of this manual.		

NOTES

NOTES

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Printed in U.S.A. 7/75

PART NO. 02108-90004