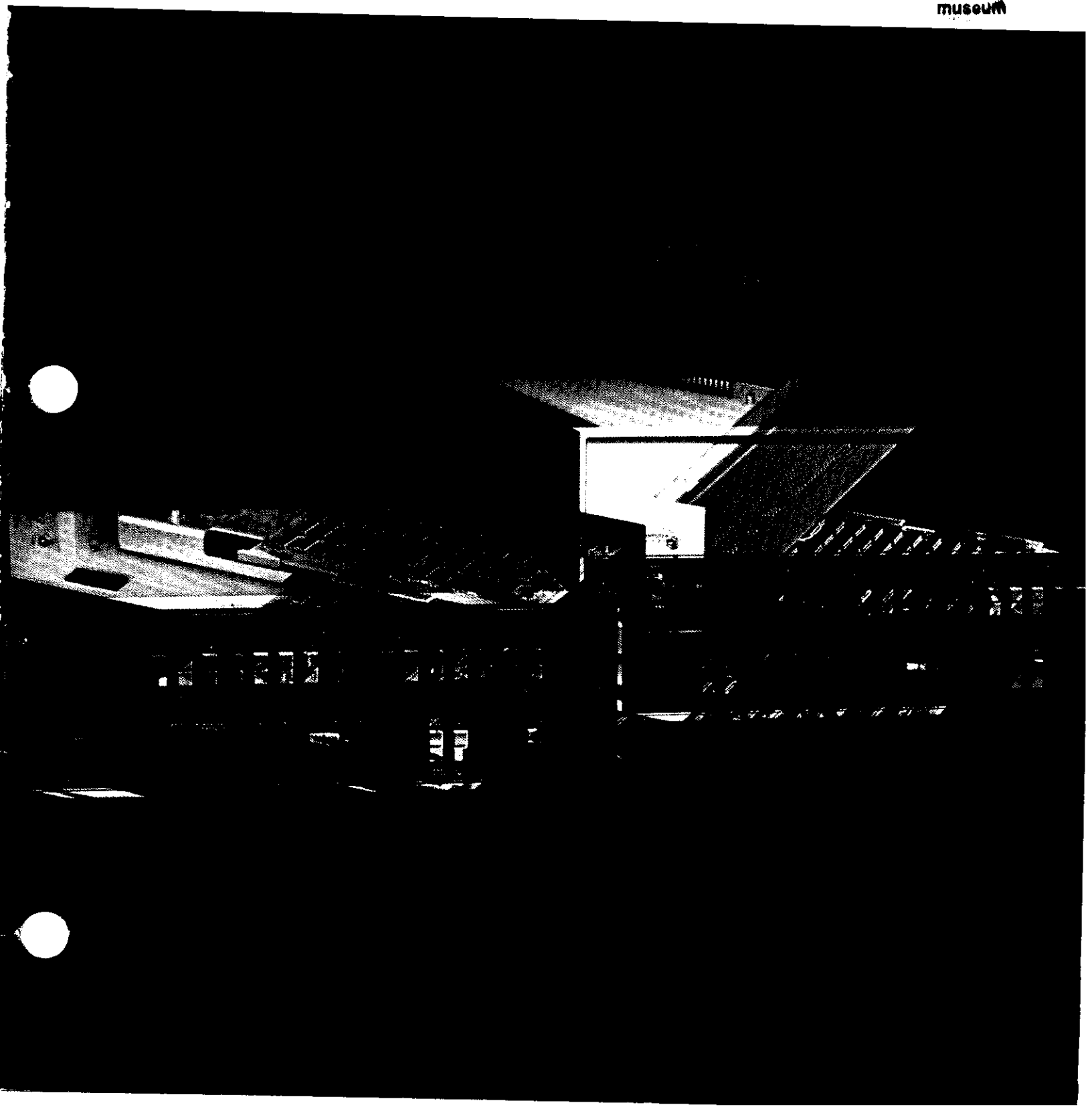
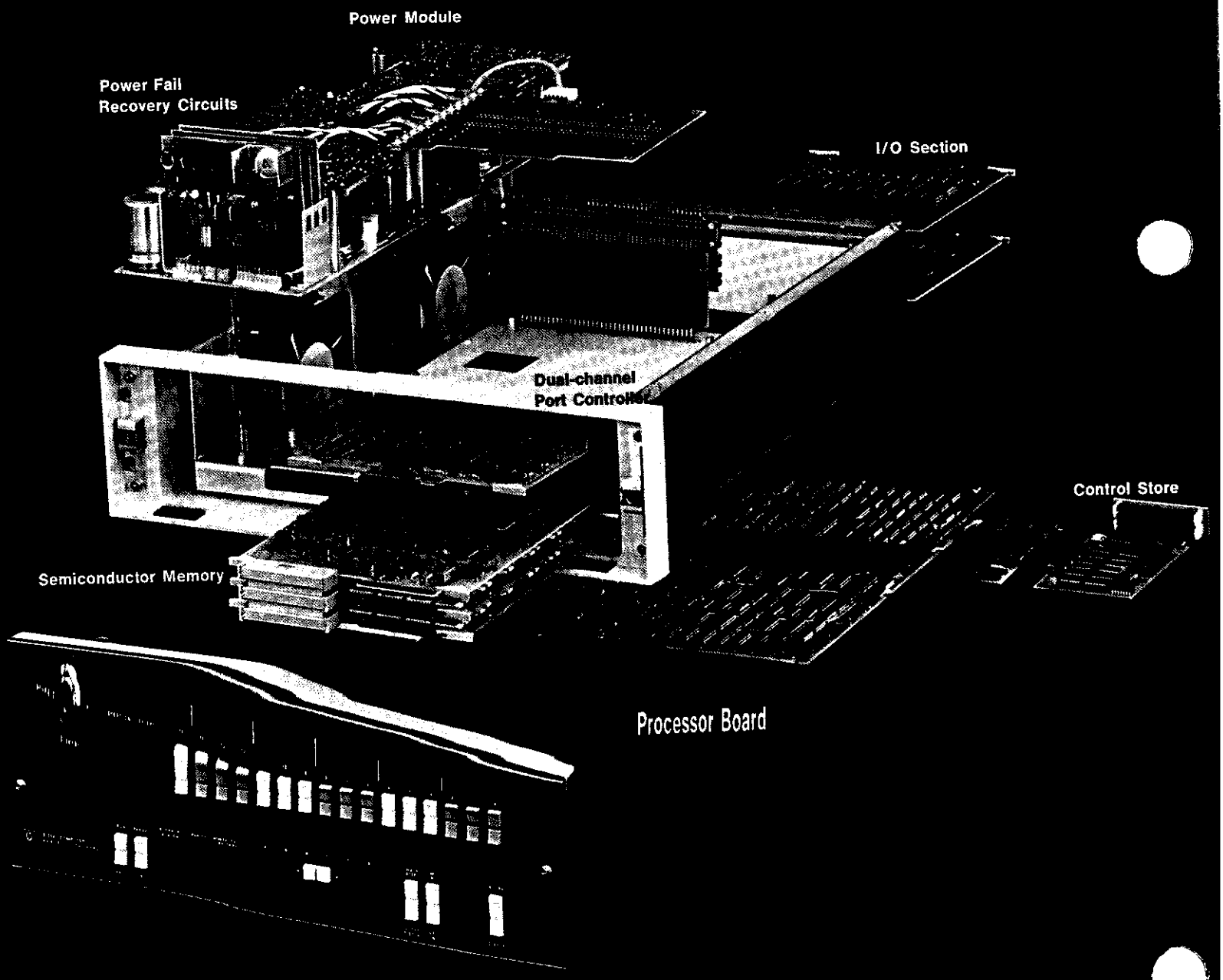
Hewlett-Packard

# HP 21MX
## Computer Series

Leaders in Technology




Power Module
Power Fail
Recovery Circuits
I/O Section
Dual-channel
Port Controller
Control Store
Semiconductor Memory
Processor Board

# A modular family of minicomputers



A true family of minicomputers, the HP 21MX Series features a choice of semiconductor memory systems, user microprogrammable processors, and customized instruction sets. Independent selections of a HP21-M processor, a HP21-X memory system, and common firmware enhancements define a specific computer configuration.

Advanced modular design eliminates the usual series of compromises between memory expansion and I/O configuration. Maximum expansion of memory, I/O, and firmware within a given mainframe are individually determined and not interdependent. In each case the M Series processor totally encases the control processor, control store, memory system, power system, I/O section, and front panel.

Initially, the 21MX Series includes two distinct microprogrammable processors and two distinct semiconductor memory systems:

- The HP 21-M/10 processor is only 5¼ inches high, and has capacity for 2 memory modules and 4 fully powered I/O channels.
- The HP 21-M/20 processor is 8¾ inches high, can accommodate four semiconductor memory modules, and has nine fully powered I/O channels.
- The HP 21-X/1 semiconductor memory system is designed with high density 16-pin MOS memory components. It is offered in both 8,192 16-bit word, and 16,384 16-bit word modules.
- The HP 21-X/2 semiconductor memory system is designed with a 22-pin MOS memory component and offered in 4,096 word and 8,192 word modules.

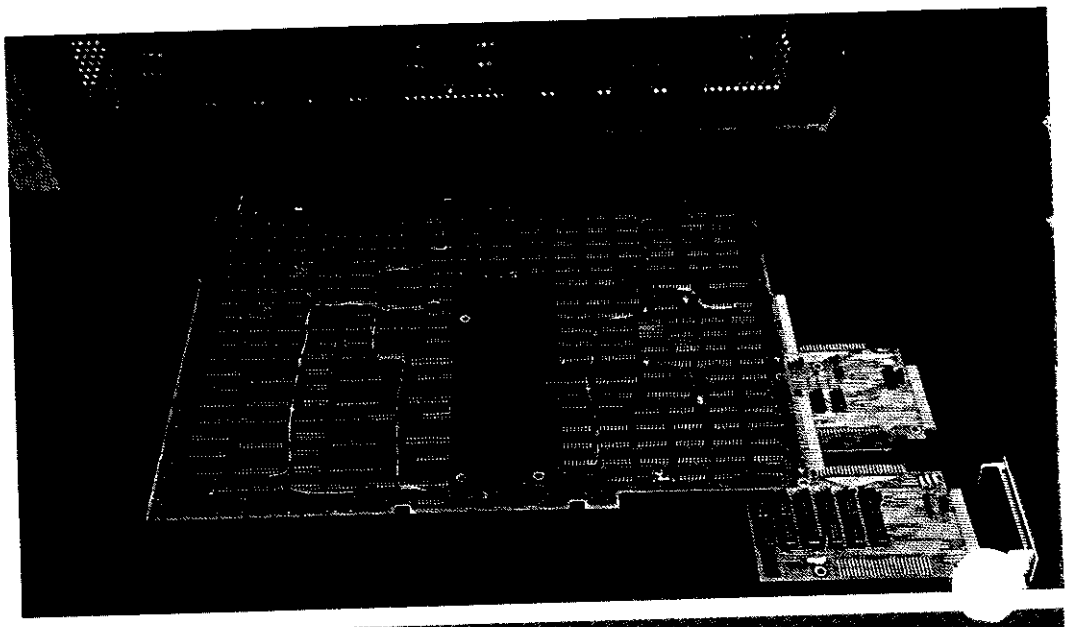
The power system designed into the 21MX Series minicomputers is unique in its ability to function in substandard electrical conditions. Line voltages can fluctuate up or down 20%, and line frequency may vary from 47.5 to 66 hertz without danger of having to initiate a power fail routine. Even in the event of a total line failure, the power system allows up to 500 microseconds to process a power fail routine. The Power Fail Recovery system will sustain the integrity of a 32K word memory system for at least two hours.

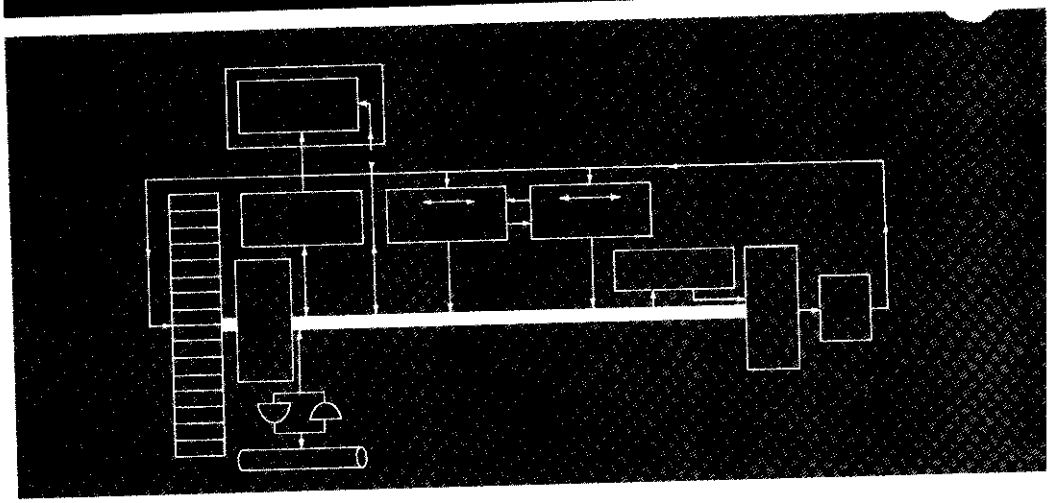
A portion of the control store section of the M Series processor emulates earlier Hewlett-Packard minicomputers, assuring that systems and programs written for more than 9,000 minicomputers will run on the new HP 21MX Series minicomputers.

# Control Processor

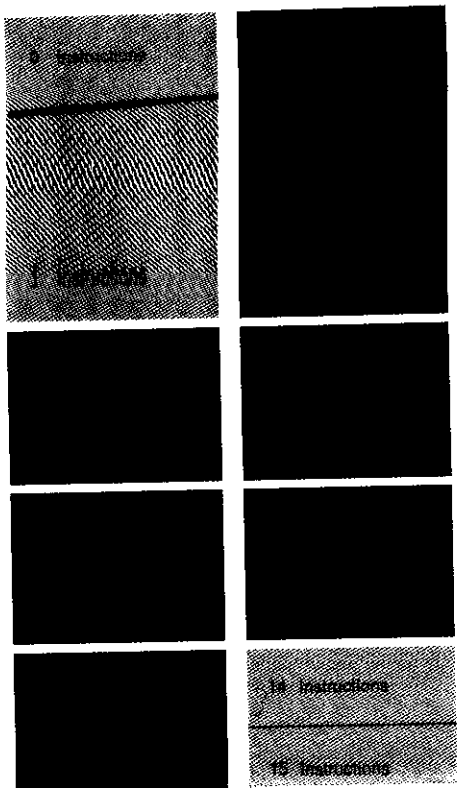
The heart of a 21MX Series minicomputer is a powerful 24 bit microprogrammable processor. The processor provides a powerful 128 word instruction set, seventeen high-speed general purpose registers, two index registers, and two accumulators. The control processor memory, or Control Store, is addressable to 4,096 words of Read Only Memory (ROM). The Control Store is used to define the standard instruction set, optional instruction set enhancements supplied by Hewlett-Packard, and user written routines or instructions.

The Control Store addressing space is logically divided into 16 sections, numbered 0 thru 15. Each of these sections represents a 256 word ROM module. In the standard configuration of the processor, sections 0, 1, 14, and 15 are used for the regular instructions, including floating point instructions. Sections 2 thru 11 will be used for optional enhancements developed by HP, or, if those enhancements are not needed for your application, you may utilize the sections for your own routines. No Hewlett-Packard supplied capabilities will occupy modules 12 and 13, thereby assuring those modules can always be dedicated to your individual system.





**Control Store Layout**



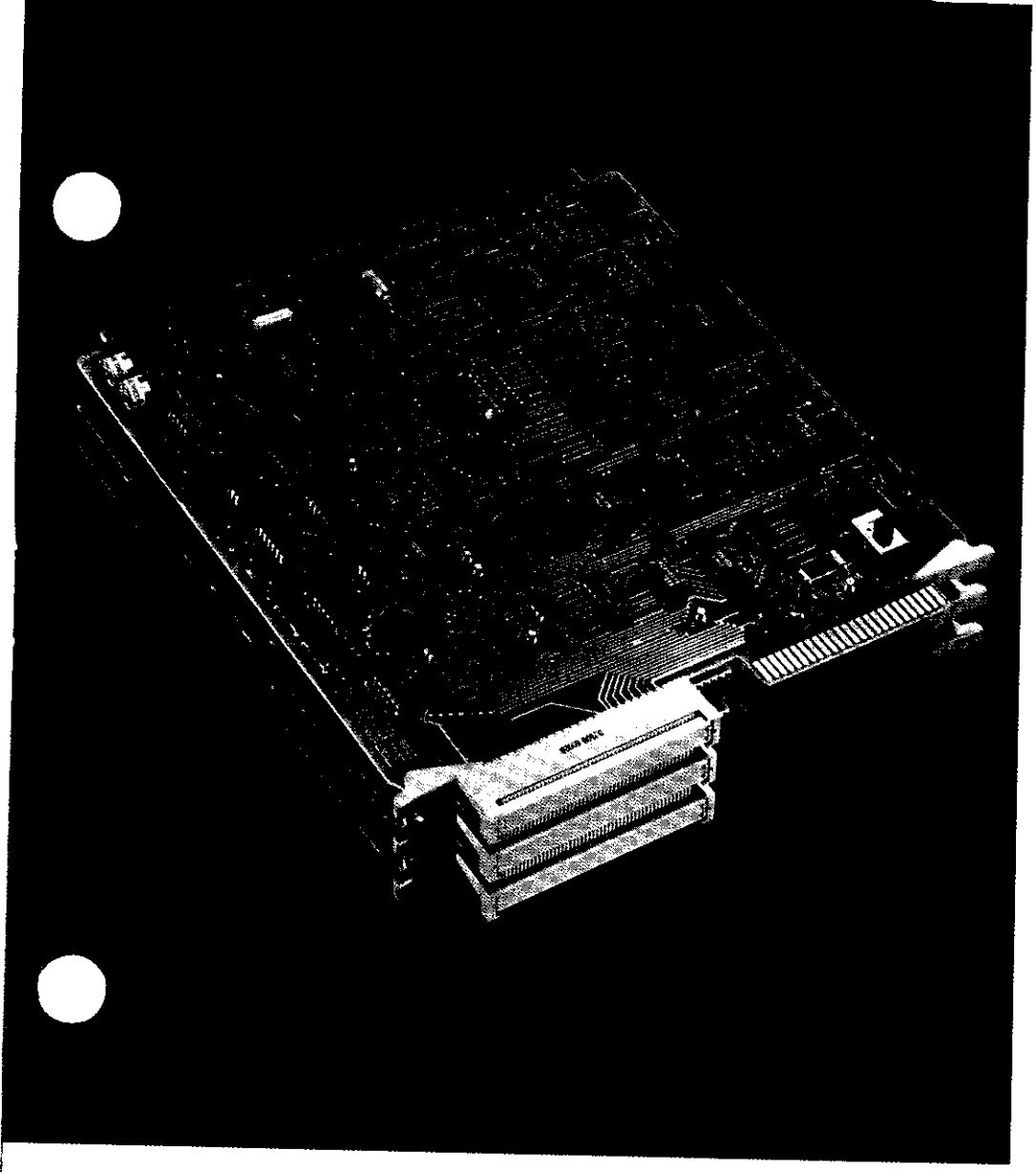

## Multi-Bus Control Processor

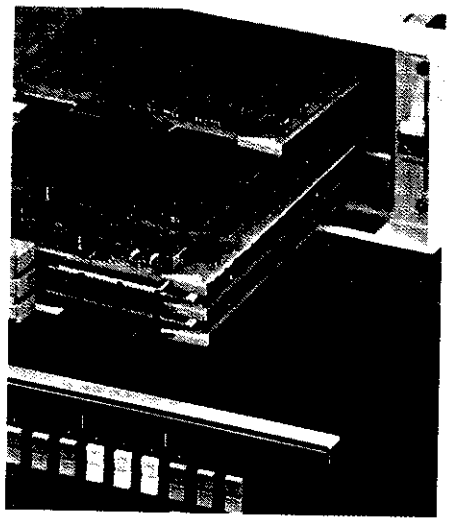
The programmer has complete control of the processor by directing data from all 19 registers and two accumulators onto the S-Bus of the processor and into the Arithmetic Logic Unit or memory. From the ALU, the programmer directs his data into the registers along the T-Bus. The simplicity of microprogramming allows complete control of the processor to quickly and efficiently solve your application needs.

## Powerful Instruction Set

Hewlett-Packard has utilized this control processor and memory to implement a powerful standard instruction set. The HP 21MX Series has 128 instructions standard, including:

- the floating point group
- the memory reference group
- the register reference group
- the I/O group
- the extended arithmetic group
- the indexed group
- the data communications group





**Dual Channel Port Controller**

Beyond the usual DMA, a dual channel memory port controller connects any two peripherals, under program control, directly to the memory system. The controller contains control logic, memory address, and word count registers not contained in the direct memory access (DMA) facilities commonly found in other computers. All Hewlett-Packard device interfaces include the ability to use the dual-channel controller at no extra charge. The controller is dynamically assignable under program control to any two I/O device channels simultaneously. Transfer Rate: 616,666 words per second. Block Size: 1 to 32,768 words.

ory uses low capacitance (5 picofarads) TTL compatible clock inputs and is extremely tolerant of noisy environments.

The X/2 memory system is designed for price sensitive applications where memory density is less important. It is based on a 4096 bit MOS memory chip in a 22 pin ceramic package. The HP21-X/2 memory system cycle time is 650 nanoseconds. The memory component uses a single low capacitance, TTL compatible clock input.

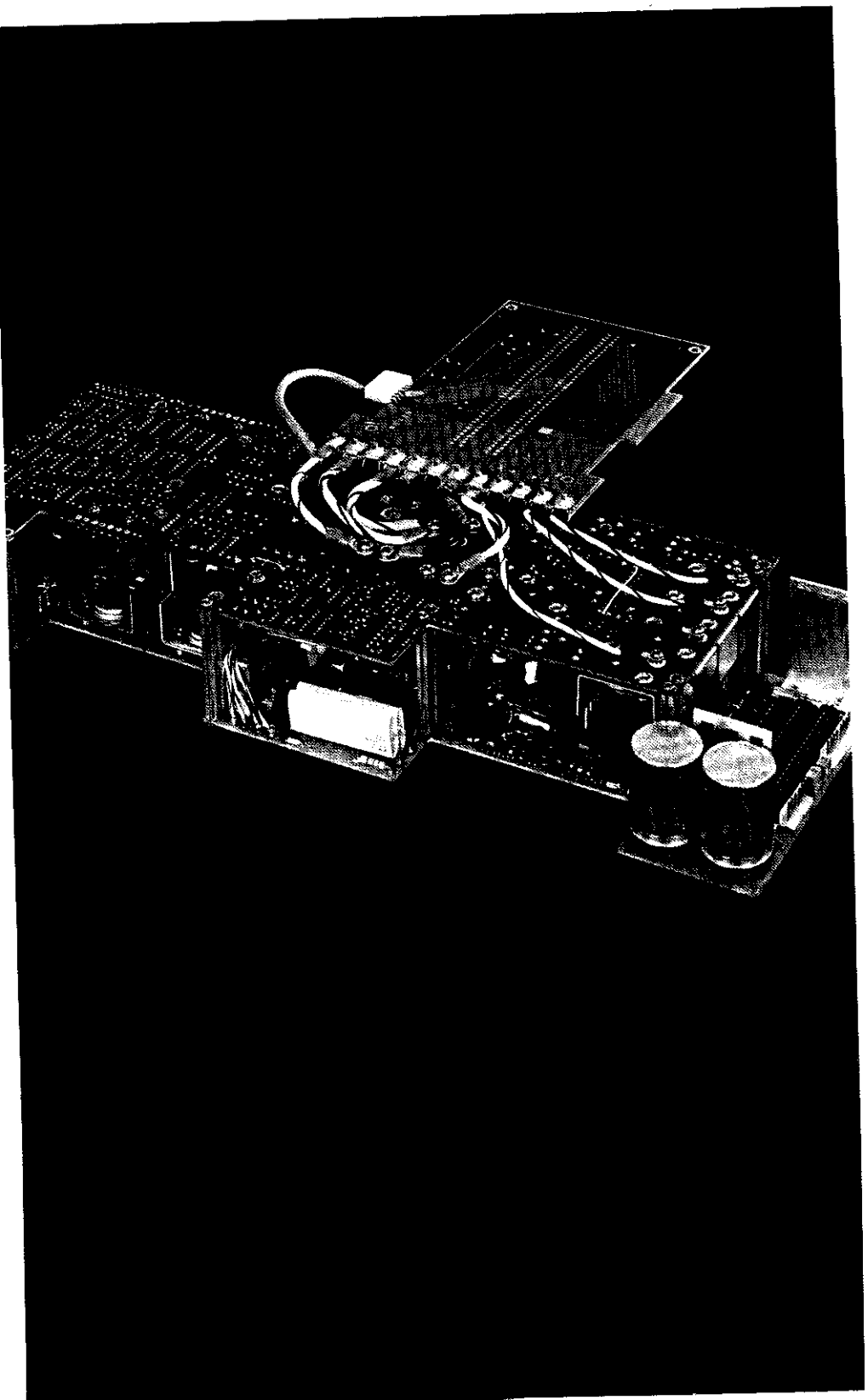
MOS memory greatly reduces the power requirements of the 21MX Series minicomputers. This allows a more versatile power module to be designed into the computer and, at the same time, allows more power for I/O devices at no increase in cost. The active power requirement for a X/1 memory chip is under 100 mW per bit. Standby power is under 2.5 mW per bit. The X/2 requires 100 mW and .5 mW per bit respectively. Because of the power requirements of the memory, the computer has significantly lower heat dissipation. This results in reduced energy consumption and more flexibility in system design for cooling and packaging.

**Memory Protect**

Memory protect is available for use in the M/20 processor. It protects the integrity of operating systems against accidental modifications. Memory protect sets up a fence which divides memory space into two segments, separating the operating system from user programs. If any part of a user program seeks to modify system space, the system interrupts and takes control. This is a necessity for many real time environments, and other highly interactive systems.

# Unique Power Systems





Because OEM systems often must perform in rugged environments, of particular concern to you is the electrical power supplied to your system. Hewlett-Packard has designed into the HP 21-M Series processors power modules which can cope with today's wide range of power fluctuations and brownouts. If the power line should fail for as long as two cycles, Hewlett-Packard's new minicomputers will continue to operate normally. Many minicomputers go into power fail routine with the loss of a single power cycle. Great tolerance has been provided for unusual power conditions. Specified performance is maintained even if line voltage drops to 88 (as low as 176 in 230V connections). Line frequency may vary from 47.5 to 66 Hz. Power system efficiency is above 70%. The usual M/10 configuration consumes less than 300 watts; typical for the HP21-M/20 is 400 watts. This is real security and performance for today's OEM applications.

- Line Voltage:
  110V or 220V AC (±20%), single phase
- Line Frequency:
  47.5 to 66 Hertz
- Power Consumption:
  M/10: 400 Watts maximum
  M/20: 525 Watts maximum
- Cycle Loss Toleration:
  Memory will be sustained through 10 cycles

**Power available for I/O Interfaces***

| Supply | M/10 | M/20 |
|---|---|---|
| +12V | 1.0A | 1.5A |
| + 5V | 6.0A | 13.0A |
| − 2V | 2.0A | 4.0A |
| −12V | 1.0A | 1.5A |

*Assume 32K system with DCPC

## Memory Reference Group (14)

| 15 | 14 | 10 | 9 | 0 |
|---|---|---|---|---|
| D/I | Instruction | Z/C | Memory Address | |

| Mnemonic | Description |
|---|---|
| AND | "AND" (M) to A; result in A |
| XOR | "Exclusive OR" (M) to A; Result in A |
| IOR | "Inclusive OR" (M) to A; Result in A |
| JSB | Jump to subroutine, save P |
| JMP | Jump, unconditionally |
| ISZ | Increment (M); skip if result zero |
| ADA/B | Add (M) to A or B; result in A or B |
| CPA/B | Compare (M) with A or B; skip if unequal |
| LDA/B | Load (M) into A or B |
| STA/B | Store A or B into M; A/B unchanged |

## Register Reference Group (39)

| 15 | 11 | 10 | 9 | 0 |
|---|---|---|---|---|
| Class | A/B | SR/AS | Combined Instruction | |

### Shift-Rotate Group

| Mnemonic | Description |
|---|---|
| NOP | No operation |
| CLE | Clear E (Extend) |
| SLA/B | Skip if least significant bit of A/B is zero |
| A/BLS | A/B arithmetic left shift one bit |
| A/BRS | A/B arithmetic right shift one bit |
| RA/BL | Rotate A/B left one bit |
| RA/BR | Rotate A/B right one bit |
| A/BLR | A/B left shift one bit, sign cleared |
| ERA/B | Rotate E right one bit with A or B |
| ELA/B | Rotate E left one bit with A or B |
| A/BLF | Rotate A or B left four bits |

### Combining Guide

Combine one instruction in a column with any instructions in adjacent columns.
(References to A and B registers cannot be mixed.)
Example: ALS, CLE, ARS is executed in one instruction.

| | | | |
|---|---|---|---|
| ALS | | | ALS |
| ARS | | | ARS |
| RAL | | | RAL |
| RAR | CLE | SLA | RAR |
| ALR | | | ALR |
| ERA | | | ERA |
| ELA | | | ELA |
| ALF | | | ALF |

| | | | |
|---|---|---|---|
| BLS | | | BLS |
| BRS | | | BRS |
| RBL | | | RBL |
| RBR | CLE | SLA | RBR |
| BLR | | | BLR |
| ERB | | | ERB |
| ELB | | | ELB |
| BLF | | | BLF |

### Alter-Skip Group

| Mnemonic | Description |
|---|---|
| CLA/B | Clear A or B |
| CMA/B | Complement A/B (one's complement) |
| CCA/B | Clear-Complement A/B (set to −1) |
| CLE | Clear E (Extend) |
| CME | Complement E |
| CCE | Clear-complement E (set E) |
| SEZ | Skip if E is zero |
| SSA/B | Skip if sign of A/B is zero (positive) |
| SLA/B | Skip if least significant bit of A/B is zero |
| INA/B | Increment A/B by one |
| SZA/B | Skip if A/B is zero |
| RSS | Reverse skip sense |

### Combining Guide

Combine one instruction in a column with any instructions in adjacent columns.
(References to A and B registers cannot be mixed.)
Example: ALS, CLE, ARS is executed in one instruction.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CLA | | CLE | | | | | |
| CMA | SEZ | CME | SSA | SLA | INA | SZA | RSS |
| CCA | | CCE | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CLB | | CLE | | | | | |
| CMB | SEZ | SME | SSB | SLB | INB | SZB | RSS |
| CCB | | CCE | | | | | |

## Input/Output Group (17)

| 15 | 11 | 10 | 5 | 0 |
|---|---|---|---|---|
| Class | A/B | Instruction | Channel No. | |

| Mnemonic | Description |
|---|---|
| HLT | Halt Program |
| STF | Set flag bit of selected I/O channel |
| CLF | Clear flag of selected I/O channel |
| SFC | Skip if flag clear |
| SFS | Skip if flag set |
| MIA/B | Merge "OR" I/O channel into A/B |
| LIA/B | Load I/O channel into A/B |
| OTA/B | Output A/B to I/O channel |
| STC | Set control bit of selected channel |
| CLC | Clear control bit of selected channel |
| STO | Set overflow bit |
| CLO | Clear overflow bit |
| SOC | Skip if overflow bit clear |
| SOS | Skip if overflow bit set |

## Extended Arithmetic Group (10)

### Memory Reference

| 15 | 14 | 12 | 11 | 10 | 3 | 0 |
|---|---|---|---|---|---|---|
| Class | | ± | * | Instruction | (Zeros) | |
| D/I | Memory Address | | | | | |

### Register Reference

| 15 | 11 | 10 | 3 | 0 |
|---|---|---|---|---|
| Class | ± | * | Instructions | No. of Shifts |

| Mnemonic | Description |
|---|---|
| MPY | Multiply |
| DIV | Divide |
| DLD | Double Load |
| DST | Double Store |
| ASR | Arithmetic Shift Right |
| ASL | Arithmetic Shift Left |
| RRR | Rotate B and A Registers Right |
| RRL | Rotate B and A Registers Left |
| LSR | Logically Shift B and A Registers Right |
| LSL | Logically Shift B and A Registers Left |

## Floating Point Group (6)

| 15 | 14 | 8 | 1 | 0 |
|---|---|---|---|---|
| SGN | Mantissa | | | |
| Mantissa (cont.) | | Exponent | SGN | |

| Mnemonic | Description |
|---|---|
| FAD | Floating point addition |
| FSB | Floating point subtraction |
| FMP | Floating point multiplication |
| FDV | Floating point division |
| FLT | Fixed point to floating point conversion |
| FIX | Floating point to fixed point conversion |

## Indexed Group (32)

| 15 | 12 | 11 | 10 | 5 | 4 | 3 | 2 | 0 |
|---|---|---|---|---|---|---|---|---|
| Class | | A/B | Class | | ± | X/Y | Instr. | |

| Mnemonic | Description |
|---|---|
| CA/BX/Y | Copy A/B to X/Y |
| CX/YA/B | Copy X/Y to A/B |
| XA/BX/Y | Exchange Registers A/B↔X/Y |
| ISX/Y | Increment X/Y Skip if Zero |
| DSX/Y | Decrement X/Y Skip if Zero |
| LDX/Y | Load X/Y from Memory |
| STX/Y | Store X/Y to Memory |
| LA/BX/Y | Load A/B Indexed by X/Y |
| SA/BX/Y | Store A/B Indexed by X/Y |
| ADX/Y | Add Memory to X/Y |
| JLY | Jump and Load Y |
| JPY | Jump Indexed by Y |

## Data Communications Group (10)

| 15 | 9 | 8 | 0 |
|---|---|---|---|
| Class | | Instruction | |

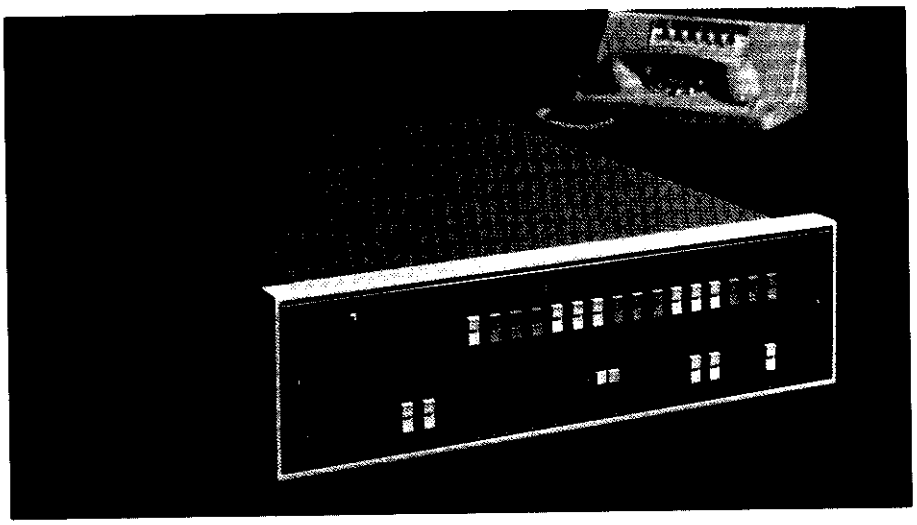
| Mnemonic | Description |
|---|---|
| LBT | Load Byte |
| SBT | Store Byte |
| MBT | Move Bytes |
| MVW | Move Words |
| CBT | Compare Bytes |
| CMW | Compare Words |
| SFB | Scan for Byte |
| SBS | Set Bits |
| CBS | Clear Bits |
| TBS | Test Bits |

*Word Format Symbols Used

D/I Direct/Indirect; Z/C page zero/current;
A/B Register or Accumulator Identifier
SR/AS Shift Rotate/Alter-Skip Identifier
± Instruction Bit
*
* Class Bit

# Semiconductor Memory Systems





### User Microprogrammable

Hewlett-Packard is the industry leader in user microprogrammable computers. Microprogrammability provides five major advantages which, in combination give the OEM additional capability available only from HP.

- Speed
- Simplicity
- Flexibility
- Economy
- Security

Speed enhancements by factors of 2 to 30 can be realized by microprogramming critical routines. An OEM who is bottlenecked by computational problems can remove those bottlenecks with microprogramming.

Microprogramming is simple and straight forward. It is as easy as assembly language to implement. Microprogramming gives the HP 21MX Series minicomputers a degree of flexibility that permits the processors to be enhanced and customized far beyond the versatility of an ordinary machine. Individual routines can be microprogrammed for maximum efficiency. Or a new instruction, specific to your application can be added, giving you, the OEM, a unique advantage in your industry. Through microprogramming, you gain access to 178 micro-orders for a more powerful control tool.

Utilizing the microprogrammability of the HP21-M/10 and M/20, you can save a significant amount of memory space by making programs and routines resident in the Control Store memory.

In addition to increased speed, simplicity, flexibility and economy, microprogramming gives you a degree of program and system security which is unavailable in a conventional machine. For example, you can plug in your firmware enhancement later to maintain/protect your customer base from competition.

Writable Control Store provides more memory for user written control instructions. With 256 24-bit words, a WCS module has enough storage capacity for many new instructions and high speed routines. WCS has a read access time of 60 nanoseconds, the same as the main Control Store. It can be dynamically altered for more extensive needs. One WCS module may be used in the HP21-M/10 processor and two in the HP21-M/20.

### Solid State Memory

The HP 21 MX Series is a minicomputer family completely designed for solid state memory. Semiconductor technology has now matured beyond the capabilities of traditional core memory, and Hewlett-Packard has integrated this new technology into a minicomputer providing the systems supplier with large amount of highly reliable, economic mainframe memory.

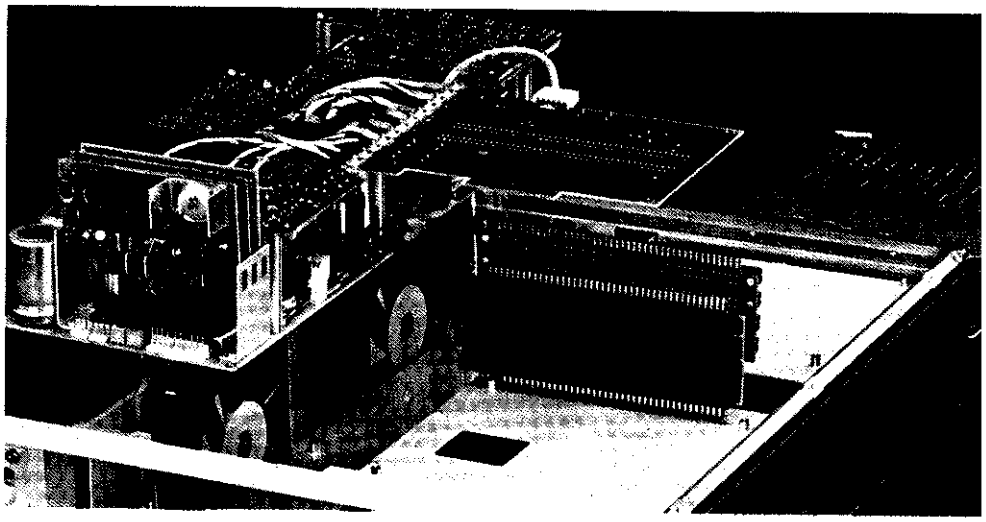
Metal-Oxide Semiconductor (MOS) memory provides several advantages to the OEM that are not available to core memory users. While costs to produce core memory have stabilized, rapid advances in the semiconductor industry will continue to provide performance enhancements, increases in density and price roll-offs. The consequence of these technological advances for the OEM is an end product which will remain highly competitive in price and performance over a long product life cycle.

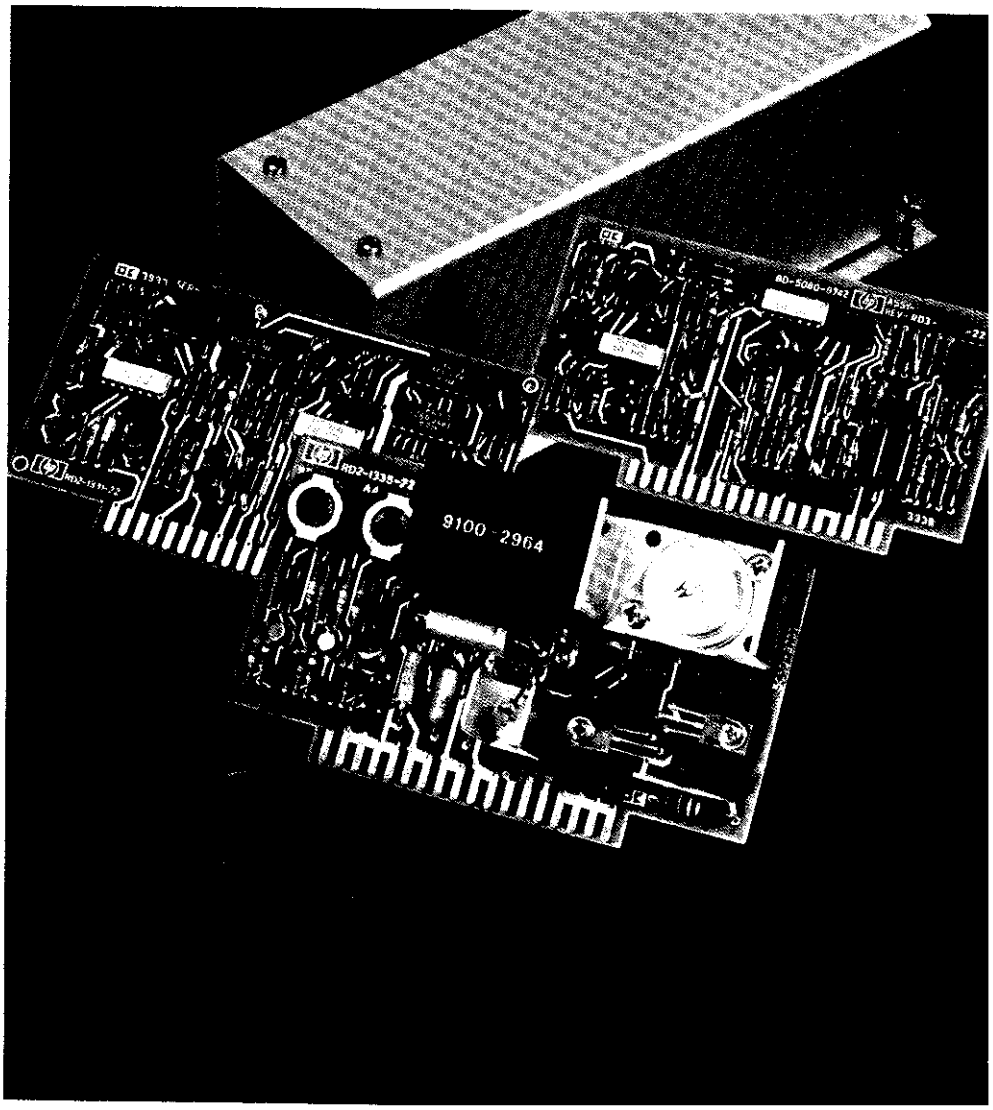
### Memory Systems

Memory parity is standard in all HP 21-X memory systems. Each memory word is 17 bits wide: 16 bits for data and one bit for parity. This feature protects the integrity of your programs and data from the common problem of occasional bit loss and system failure.

The X/1 memory systems provide a choice of 8K or 16K word memory modules, all with memory parity standard, for needs where space is critical and high density memory is an advantage. The HP 21-M/10 processor can be extended to two modules of semiconductor mainframe memory and the HP 21-M/20 processor to four modules. The X/1 memory system is based on a 4096-bit dynamic MOS random access memory chip in a new 16 pin ceramic package. The X/1 memory system cycle time is 650 nanoseconds, insuring highly efficient use of all memory reference operations. The memory design uses an N-channel self-aligned, polysilicon-interconnect process. The mem-

Unusual environmental immunity has been designed into the power system of these new minicomputers. Not only do they operate normally with varying line frequencies or low line voltages, they protect themselves automatically against high-voltage conditions thru a total crowbar protection system. Also they function to specification at temperatures from 0° to 55°C. Furthermore, they are tested to withstand the same shock and vibration conditions as all Hewlett-Packard electronic instruments.






### Environmental specifications

- Ambient Temperature
  Operating:
  0° to 55°C (32° to 131°F)
- Altitude
  Operating:
  15,000 feet (4,573 meters)
  Nonoperating:
  25,000 feet (7,622 meters)
- Vibration:
  1 g at 44 Hz

### Power Fail Recovery System (PFR)

A Power Fail Recovery System is available for situations where total line failure might be experienced. This system, with charging and automatic switching circuitry, provides for automatic computer restart without operator intervention after a power failure. It maintains solid state memory data integrity for up to two hours.

### PFR System Specifications:

- Type:
  12V Nickel-Cadmium
- Charging Rate:
  400 ±50 milliamperes
- Capacity:
  3.5 ampere-hours; capable of sustaining 32K of memory for 2 hours.

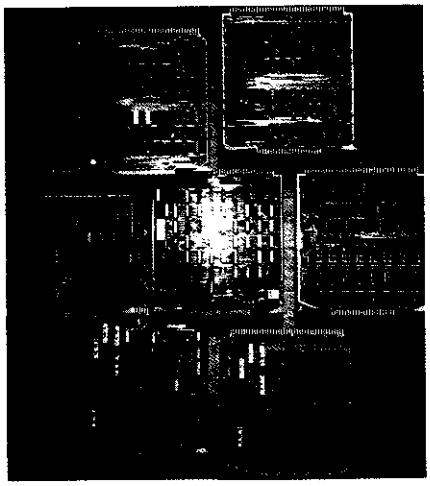
# I/O Power

**Input/Output**

The I/O section of the 21MX Series minicomputers features a multilevel Vectored Priority Interrupt (VPI) structure. The HP 21-M/10 processor has an I/O section with four powered I/O channels; the M/20 has 9 powered I/O channels standard. As many as 33 additional powered channels with VPI may be added to either processor. Hewlett-Packard peripherals are equipped, as a standard feature, with the ability to operate with a Dual Channel Port Controller for rapid data transfer.

Hewlett-Packard offers you a single source for all your I/O needs. A full range of peripherals are available, including:

Cartridge Disc Drives
Disk Pack Drives
Phase Encoded Magnetic Tape Drives
NRZI Magnetic Tape Drives
Plotters
Card Readers
Optical Mark Readers



Paper Tape Readers and Punches
Printing Terminals
CRT Terminals
Line Printers
Card Reader/Punch

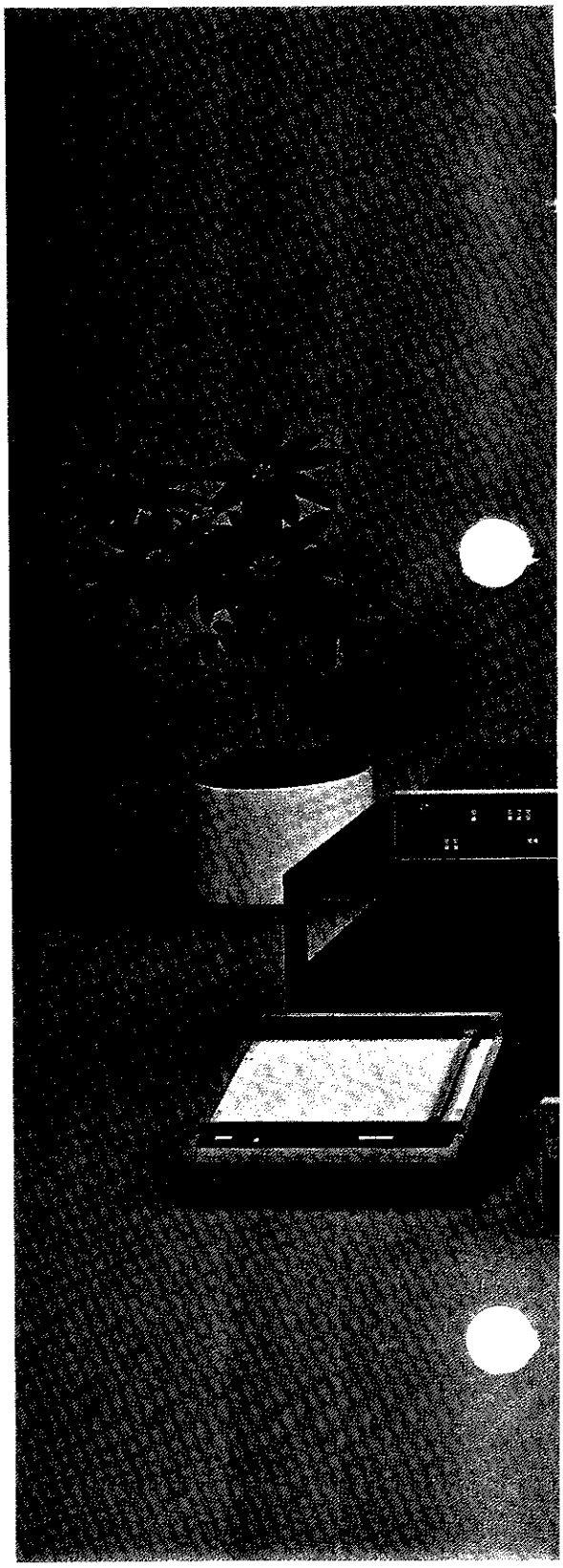
Each of these devices are interfaced with standard hardware, software drivers, diagnostics, and are available to you without need for modification.

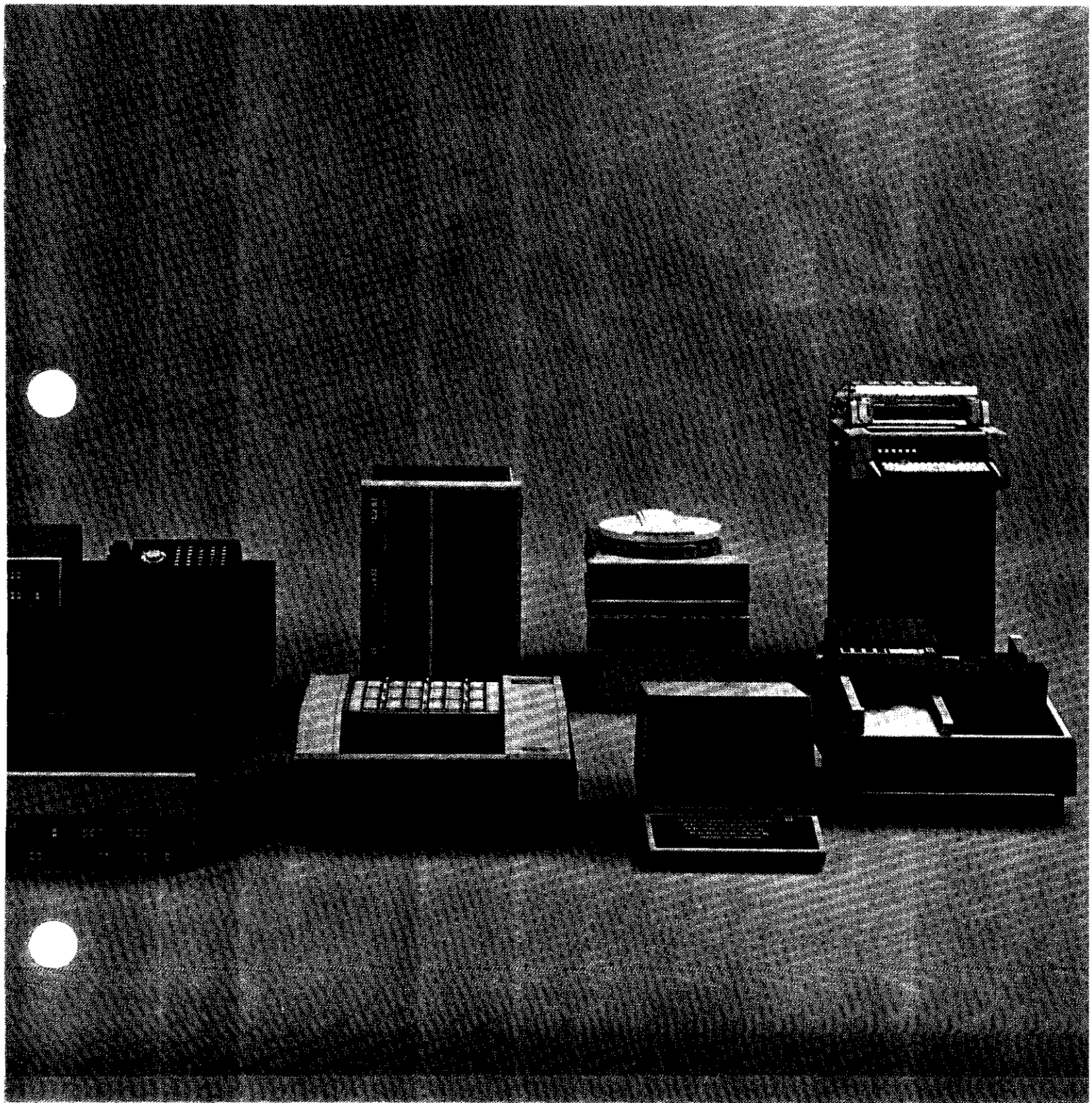
A complete selection of data communication equipment is available to meet all your needs, including:

- 16-channel Asynchronous Multiplexer with programmable character size and speed detection
- Synchronous and Asynchronous Terminal and Data Set interfaces with programmable character size and that operate in half duplex, full duplex, or simplex mode
- High speed interface for communication between Hewlett-Packard minicomputers

To complete your powerful HP 21MX computer system you can choose:

- A Time Base Generator to provide system recognized priority interrupts
- Relay Output Registers for controlling one or more devices
- 8 or 16-bit duplex registers for I/O data transfers of measurement devices with digital output
- Dual 8-bit D-A Converters for driving oscilloscopes, X-Y plotters and many other analog devices
- Microcircuit interfaces to exchange information with most digital measurement devices
- I/O breadboard cards for customized interfacing
- Dual-channel Universal interface cards for high-speed 16-bit duplex differential I/O transmission





# Software Leadership for OEMs

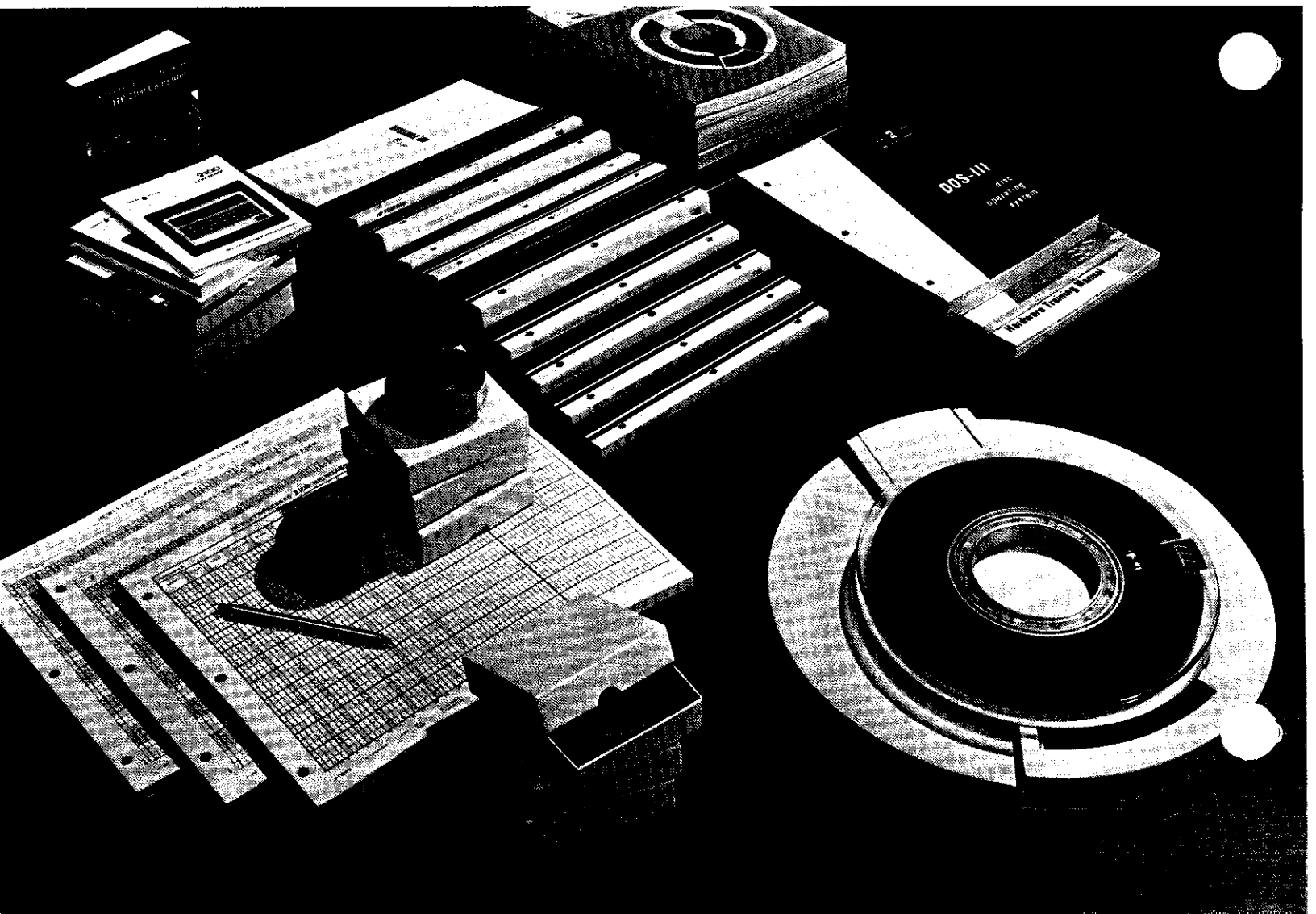
**Software**

By allowing the HP 21-M Series processors to use a portion of their control store to emulate earlier Hewlett-Packard minicomputers, HP is able to offer the OEM 2000 man years of program and system development, all proven reliable in thousands of customer installations. All operating systems and languages are available to the OEM for purchase, to allow you to take full advantage of Hewlett-Packard expertise and world-wide support.

**Systems**

**Basic Control Systems** — BCS handles loading, relocating, program linking, interrupts, and provides and calls library subroutines. BCS simplifies user programming and the execution of I/O routines.

**Disc Operating System** — DOS-III provides system features such as extended file management, program chaining, current page loading and mixing programs of different languages. It includes significant data communication facilities to allow time-critical allocation of machine response time, and can run in batch mode or interactive mode. Up to 94 million bytes of random storage can be directly accessed.



### Languages

**FORTRAN** — The Hewlett-Packard systems use the American Standards Association FORTRAN II and IV. FORTRAN can be used on BCS, DOS and RTE systems.

**Assembly Language** — These 128 instructions include machine operation codes and symbolic addressing. The output may be absolute or relocatable. The assembly language features page-free programming, fixed and floating point pseudo-operations, and the ability to reserve storage with a COM statement.

**ALGOL** — This language allows problem description in an internationally defined language. It includes all the major elements described in ALGOL 60 revised report, Communications of the ACM January 63, plus a number of features such as unrestricted nesting of conditional statements and the intermixing of REAL and INTEGER identifiers.

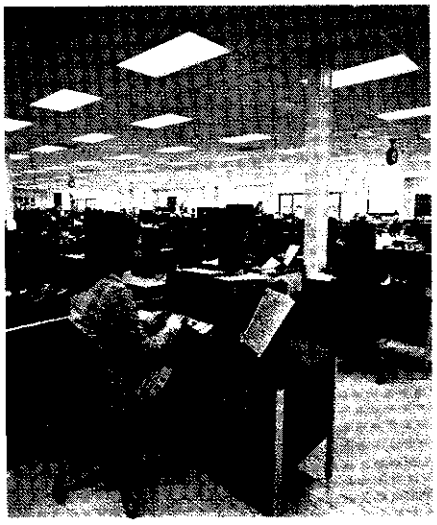
### Application Aids

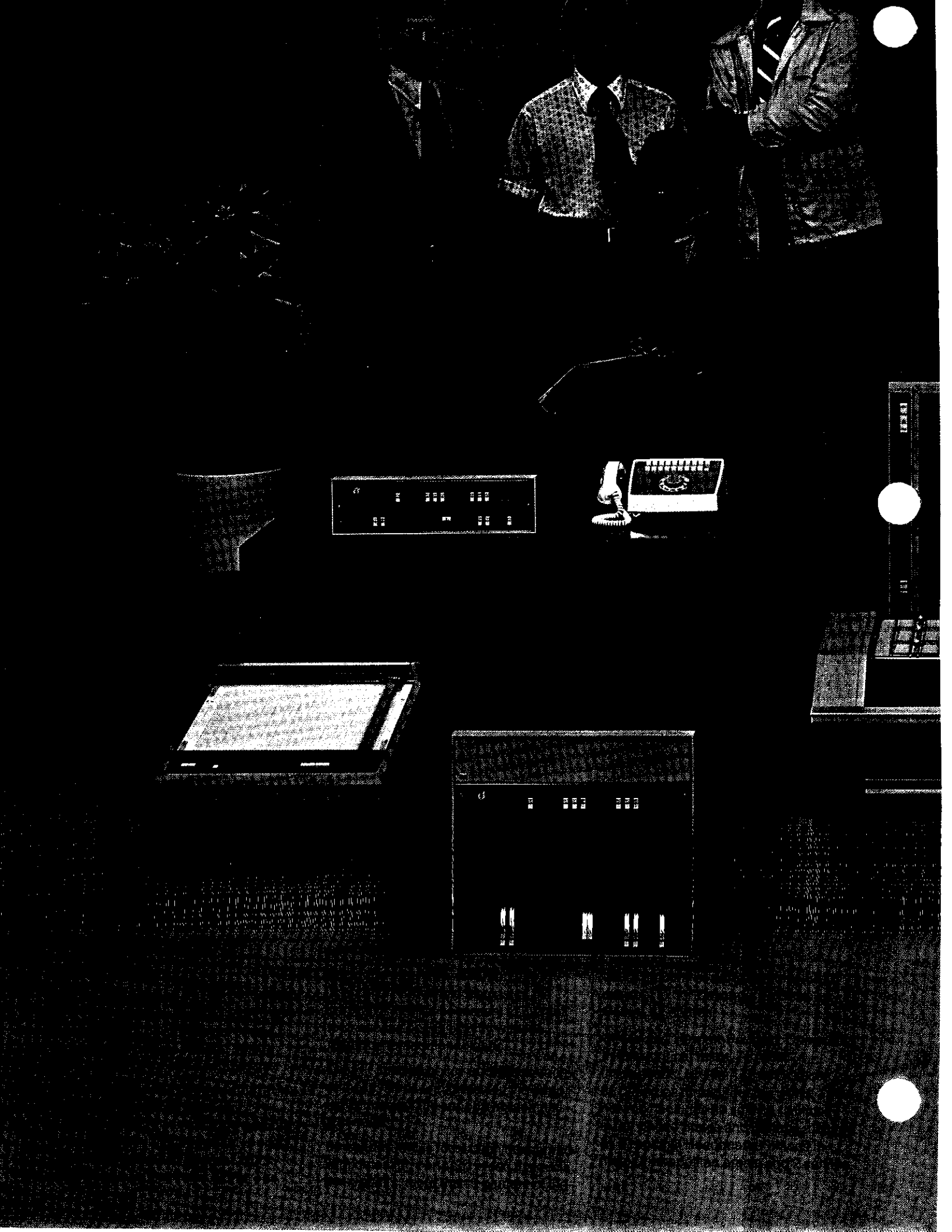
**Terminal Control System** — TCS is a control program which efficiently and effectively handles multiterminal operations on an HP OEM computer system. TCS schedules the input/output processing and the use of hardware resources in a multitasking, multiterminal environment. TCS has extensive system control facilities which shorten the application development cycle, simplify complex programming tasks, and provide for ease of expansion to additional terminal and I/O devices. In conjunction with Hewlett-Packard's thoroughly proven Disc Operating System, TCS opens new avenues to the on-line benefits of control, timeliness and accuracy, utilizing multiple data entry and multiple output stations.

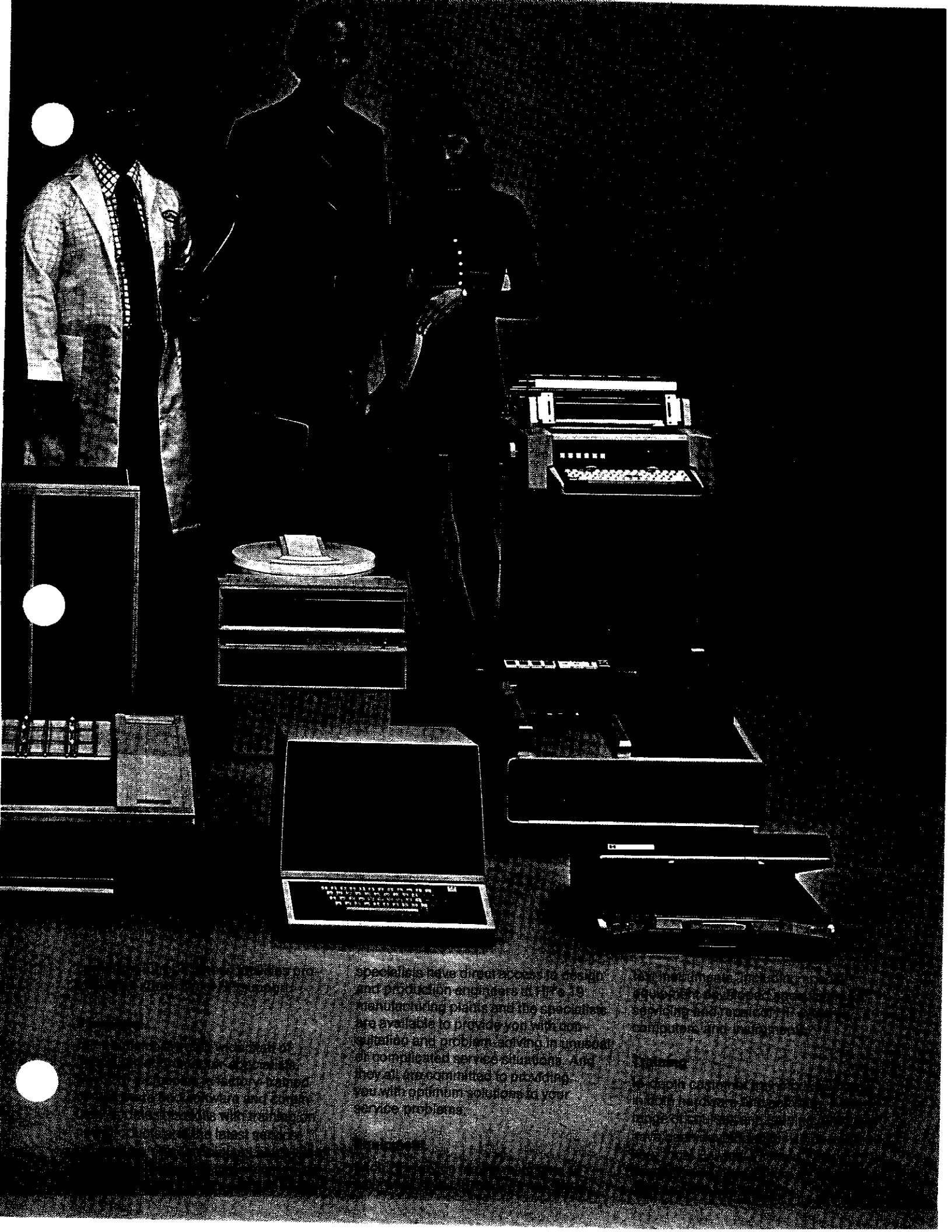
**IMAGE/2000** — enables an OEM to tailor a data base to meet his unique needs. And the fullest possible use of the information in the data base is possible because one set of records can be used by many different people for many different purposes.

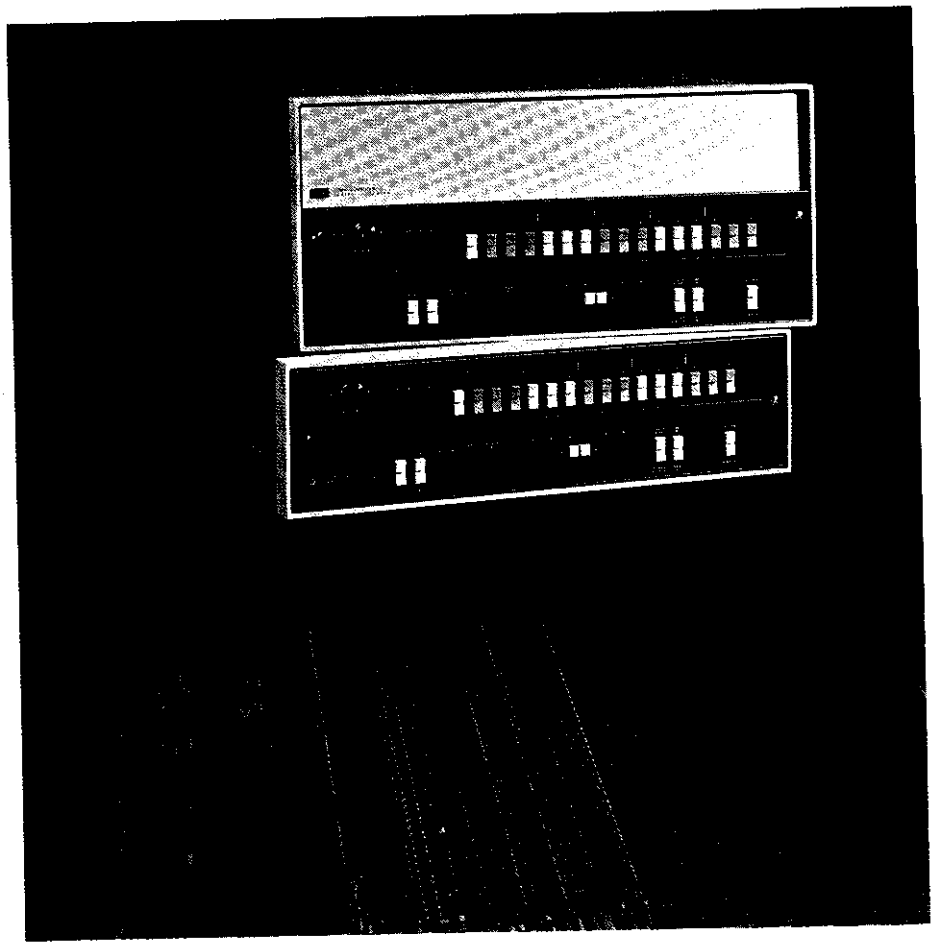
In small to medium-sized organizations, IMAGE/2000 can solve most of the data handling problems likely to be encountered. And it will do it more easily, efficiently, and economically than many other data base management systems currently available.

**Remote Job Entry** — HP RJE allows the OEM of Hewlett-Packard systems to share the resources of a batch oriented IBM 360/370 at a speed of up to 4800 Baud. This enables such tasks as data transmission, report generation, file updating, and the compilation and running of computer programs in COBOL, FORTRAN, or RPG. The processor gives the user access to centrally located data files and access to the power necessary to process those files.









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