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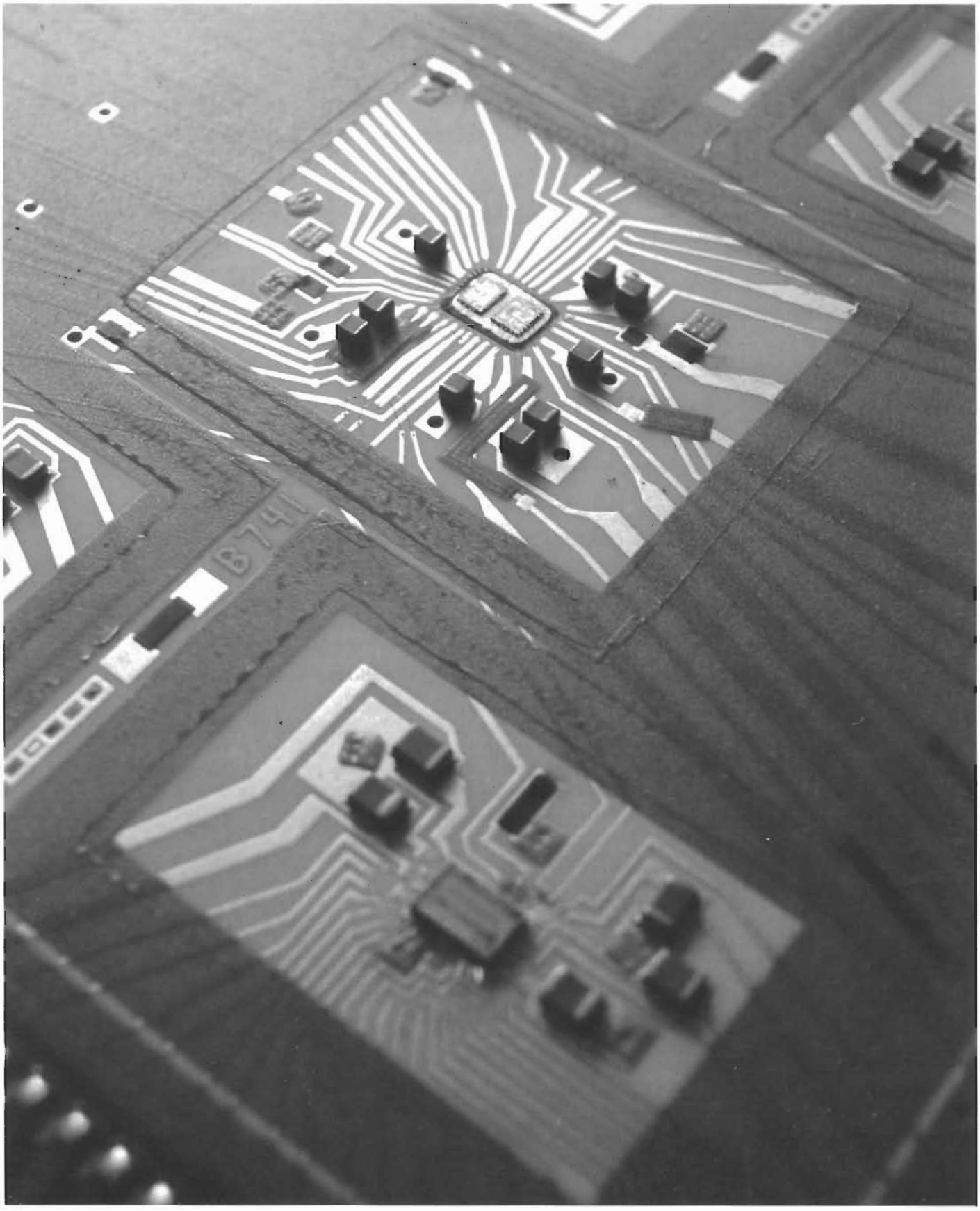

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A Reliable, Autoloading, Streaming Half-Inch Tape Drive

Designed for rack mounting, this compact tape drive cleverly channels air flow to load different-sized half-inch tape reels automatically. It also features higher performance and reliability than its predecessor.

by John W. Dong, Kraig A. Proehl, Ronald L. Abramson, Leslie G. Christie, Jr., and Douglas R. Domel

HP's NEWEST HALF-INCH TAPE DRIVE, the HP 7980A (Fig. 1), is an autoloading, reel-to-reel, horizontally mounted, streaming drive that reads and writes in two standard nine-track formats: 6250 GCR and 1600 PE.[1,2] This maintains compatibility with previous drives and tapes, an important feature because half-inch tape is still a significant standard in the computer industry for backing up, archiving, and interchanging computer data.[3]

The HP 7980A provides computer system users with a reliable, low-cost, backup device for large amounts of on-line disc memory. It does this with higher performance and reliability and lower cost than its predecessor, the HP 7978B, which it replaces. It reads and writes at 125 inches per second, roughly 60 percent faster than the HP 7978B. The HP 7980A can rewind a 2400-foot tape in less than 90 seconds, reducing overall data transfer times significantly. The HP 7980A is 40 percent more reliable, a result of the increased use of VLSI components to reduce parts counts even further than was achieved on the HP 7978B. The monthly maintenance cost of the HP 7980A is half that of the HP 7978B. Horizontally mounted in a standard-width rack cabinet, the HP 7980A is 8.75 inches high, a third the size of the HP 7978B. This saves valuable floor space and allows better use of rack cabinets.

The horizontal mounting means that the user normally cannot access the tape path to load the tape manually. Hence, an autoloading feature was designed into the HP 7980A. The operator simply places the tape reel in the door opening and closes the door. The autoloading sequence starts automatically once the door is closed, leaving the operator free to do other tasks while waiting for the tape to load in a nominal time of half a minute. There is no need for an EZ-LOAD cartridge around the tape reel, which

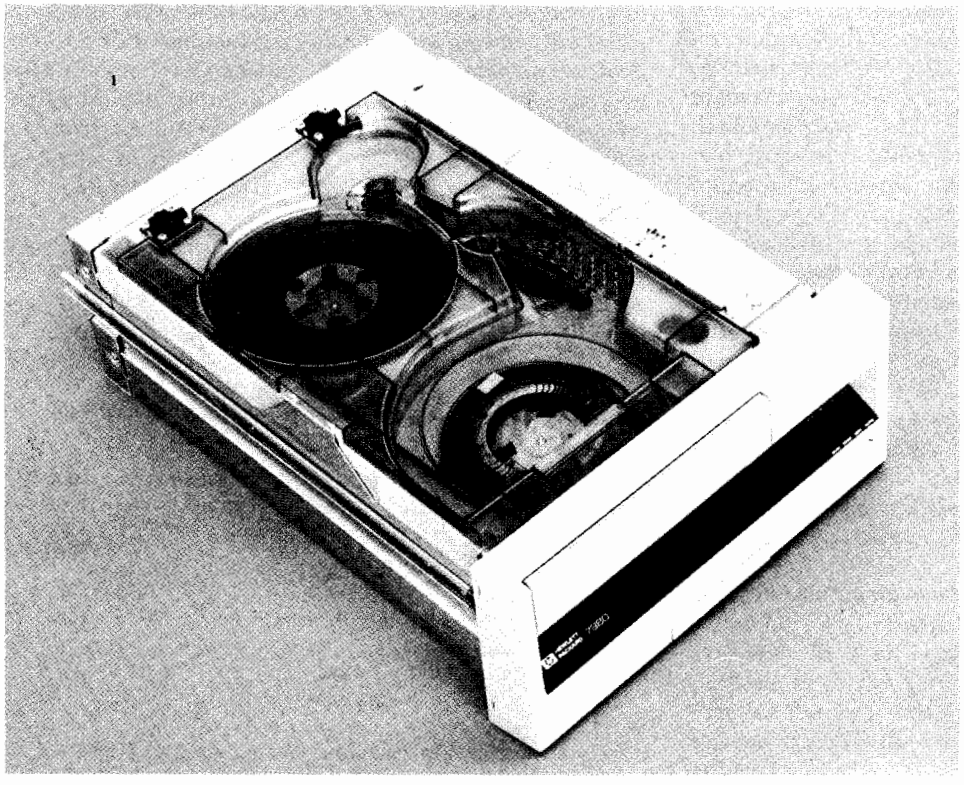

Fig. 1. *The HP 7980A Tape Drive is a half-inch, reel-to-reel, 125-ips streaming tape drive designed for systems with disc backup requirements of greater than 400 megabytes. Like its predecessor, the HP 7978B, this high-performance drive operates with both 6250 GCR and 1600 PE standard formats. The HP 7980A can automatically load and thread any size reel ranging in diameter from six to 10.5 inches. This drive can be horizontally mounted in a 19-inch-wide rack enclosure for better floor-space utilization, and it supports IBM/ANSI-compatible formats for software distribution and data interchange between HP and non-HP systems.*

is required for autoloading on the HP 7976A Tape Drive. The HP 7976A autoloads only 10.5-inch tape reels; the HP 7980A autoloads all standard half-inch tape reels from six to 10.5 inches in diameter. The earlier HP 7978A/B Tape Drive must be loaded manually and cannot autoload tapes.

In addition, the HP 7980A supports the use of 3600-foot half-inch tape, under certain guidelines, which the HP 7978B doesn't. This increases data capacity by 50 percent over standard-length tape reels.

The HP 7980A was developed and released in 40 percent less time than the previous tape drive. This was mainly a result of two factors. The first was keeping together an experienced core group of engineers from the HP 7978A/B development team to architect and design the HP 7980A drive. The second was concentrating on a core system development of the HP 7980A, that is, having a well-defined product and not adding additional features and configurations along the way. Such added features tend to prolong development cycles. This does not mean that these additional features are not eventually added, but they are worked on according to need after the core or base system is released.

Tape Path

The HP 7980A is a totally integrated tape drive, simultaneously incorporating a small form factor, an autoload feature, design-for-assembly concepts, low cost, and high reliability. The major design objective established to accomplish these goals was design simplification.

The HP 7980A has a very simple tape path as shown in Fig. 2. There are only two rolling elements: the speed sensor and the buffer arm roller. There is only one additional fixed tape guide. The oxide side of the tape contacts only the tape cleaner, the magnetic tape head, and the tape displacement unit. The tape displacement unit, located between the tape head and the tape cleaner, contacts the oxide side of the tape only during repositioning and while the tape is stopped! The tape displacement unit pushes the tape off the very smooth surfaces of the head and the tape cleaner to prevent the tape's sticking to these smooth surfaces during high temperature and humidity conditions.

The buffer arm assembly (buffer arm, spring, and roller) helps take up slack in the tape during servo starts and stops. It also establishes the tension on the tape. The buffer arm roller and fixed guide, along with the speed sensor, guide the tape in a precise manner over the head. The speed sensor measures the velocity of the tape and feeds it back to the servo system.

The half-inch tape reel is centered, seated, and locked by the supply hub. The autoload blower forces air through the door. The louvers in the door direct the air onto the tape reel to lift the end of the tape. The tape end is then carried by the air flow around the buffer arm roller and the fixed guide. It then goes over the tape cleaner and the magnetic tape head. The tape is finally sucked onto the take-up reel after passing around the speed sensor.

The drive motors are located directly beneath and are attached to the supply and take-up hubs. The blower is located between the two drive motors.

Integrated Autoload and Tape Path Design

The HP 7980A tape path is very simple. This greatly reduces costs and assists the design of the autoload mechanism. It simplifies the task of blowing the tape end off the supply reel and threading it through the tape path and onto the take-up reel.

The casting is an integral part of the tape path and autoload mechanism. The walls of the casting help determine the way the tape is blown around by the air flow created by the blower. The surface roughness of the casting is very important. The surface of the casting around the supply reel area must provide enough friction to permit the supply hub to autocenter the smaller tape reels. Conversely, the casting surface near the buffer arm assembly must be smooth enough so that the tape doesn't catch on any surface features while autoloading. The buffer arm shape is critical to autoload and servo success. The design of the air deflector on the speed sensor is crucial to how well the tape end moves around the speed sensor roller and attaches to the take-up reel.

The autoload success rate is greatly affected by the design of the door ramp and the door louvers. These are designed so the HP 7980A can autoload all standard half-inch reels with varying amounts of tape on each reel.

Holes in the top cover eliminate the need for gaskets or tight tolerances on the door-to-bezel fit and the top cover-to-casting fit. They do this by eliminating air flow reversal, which can occur when autoload air flows out the door-to-bezel and top-cover-to-casting cracks, rather than down the tape path. The ribs on the top cover fit inside the casting to reduce air leakage and allow loosening of the top-cover-to-casting fit.

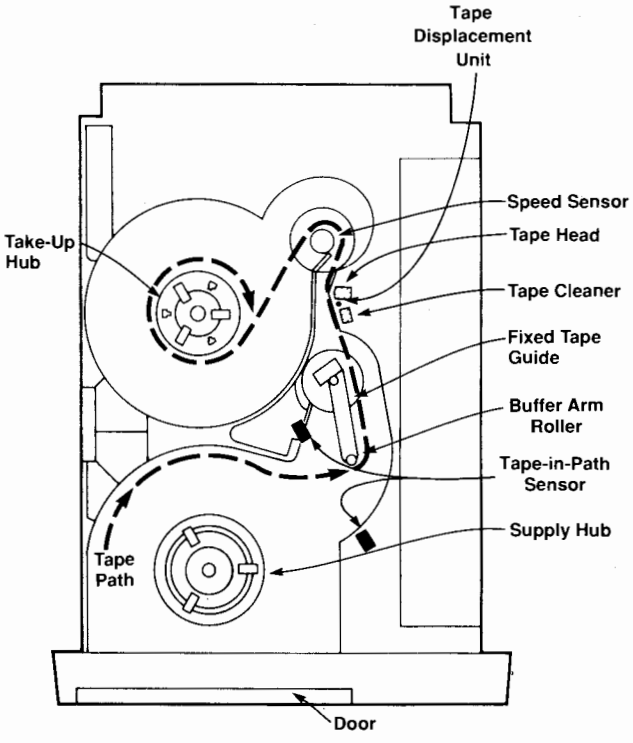

Fig. 2. *HP 7980A tape path components.*

The speed sensor is placed in the tape path for maximum tape wrap on the roller. This prevents the tape from slipping on the roller during tape acceleration and deceleration.

The buffer arm and its spring are designed and placed so that tension variations caused by the tape coming off the supply reel at different angles relative to the arm are minimized. An additional roller could have been used to feed tape at a constant angle to the buffer arm, but was not put in for several reasons: cost, simplicity, and ease of autoloading the tape.

Air System Design. The autoload air system was designed into the deck casting and the tape path from the beginning. Reduction of air ductwork was a major consideration. The less the air has to pass through winding passages, the lower the air pressure and volume requirements. For this reason, the tape path needs to be simple. Reducing the air pressure and volume reduces the autoload air blower's size, noise, and cost.

The blower is placed between the two drive motors since that provides the shortest air passage. The air is sucked into the take-up reel, into the blower, and then blown out of the blower into the door area to repeat the path (see Fig. 3).

The door is used as an air passage for several reasons. No space is taken up by air ducting to blow air into the tape path, thus allowing the maximum amount of width for the card cage. In addition, using the door as an air duct allows the air to blow across the entire front of the tape reel for maximum design flexibility. The door louvers were then designed to blow air to autoload all standard reel sizes.

The air velocity required to move the tape down the tape path was calculated from momentum and Bernouli equations. The pressure drop was calculated in a similar manner. The blower was then selected based on these calculations and the tape path, with the blower, was measured for pressure drops and velocities. The measurements were fairly close to the theoretically calculated pressure drops and air volumes.

Autoload Algorithm. The HP 7980A autoload algorithms are designed to load all sizes of half-inch tape reels in a minimum amount of time, while making sure that the user's tape is treated with as much care as possible. The autoload process is a combined effort of firmware, mechanical design, and electronic sensors. Four sensors are used by the autoload process to monitor its progress and to indicate when an error condition is present. The first of these sensors is the door sensor, which consists of two microswitches connected in series that detect whether the front door or top cover is open. When this sensor detects a door closure, the autoload process begins. Opening the top cover at any point halts the autoload. Under the supply hub is the reel encoder sensor. This optical sensor detects the three reel encoder flags attached to the supply hub. These flags interrupt the sensor beam when a reel is properly seated on the supply hub. The tape-in-path sensor is an optical sensor which is positioned across the tape path preceding the head. The tape leader will interrupt this sensor beam when it enters the tape path. The final sensor is the optically encoded speed sensor. This sensor provides two quadrature pulse trains which are decoded to give position and velocity information.

Once a door closure is sensed, the autoloading operation begins. The first task is to detect whether a reel is already threaded through the tape path, a condition that is most likely to be present after a power failure. This condition is detected by the tape-in-path sensor and by turning both the supply and take-up motors in opposing directions at a low rate. If a tape is already threaded, activity will be seen on the speed sensor. In this case, the tape does not need to be automatically threaded and the servo loops can be closed.

If a tape is not already threaded, the load fan (blower) is turned on and the supply hub is slowly rotated in a counterclockwise direction to center and seat the reel. At this point, the reel encoder sensor is checked continuously for evidence that the reel is seating itself on the hub properly. When the reel is seated correctly, all three reel encoder flags will interrupt the sensor beam once per revolution. Time interval measurements are made to ensure that all three flags (not just one or two) are present, and that they have the correct relationship. If all three flags are not detected, the supply hub is shaken back and forth quickly in an attempt to get the reel to locate itself properly on the hub. A reel that will not properly seat after shaking a second time will be rejected and a MISLOAD will be reported.

The reel encoder sensor and flags are also used to regulate the speed of the supply hub during these open-loop operations. The dc motors must turn at relatively low speeds when centering a reel and feeding the tape. These speeds require relatively low voltages at the motors. Because of voltage offsets, motor constants, and temperature changes, the rotational speed could not be adequately controlled by a single voltage command. Hence, the voltage command is constantly adjusted based on the time measured between each reel encoder flag pulse. This provides rather gross, but sufficient control over the rotational speed of the motor

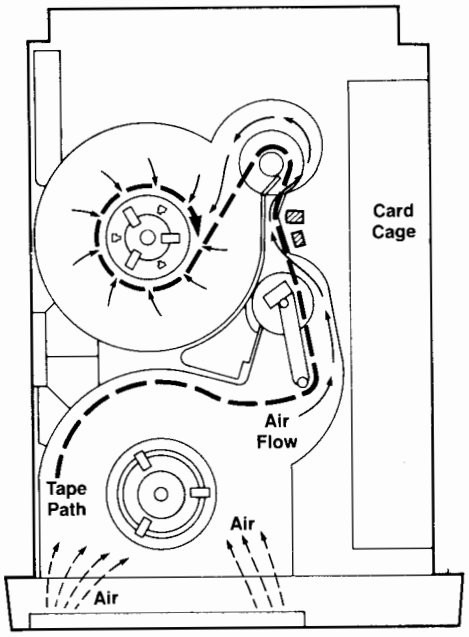

Fig. 3. *HP 7980A tape path showing air flow for automatically loading and threading a tape.*

in its open-loop mode.

After the reel is found to be seated properly on the hub, it is ready to be locked into place. First, however, the tape-in-path sensor is polled to determine if the tape is being seen continuously in the tape path. If this is the case, the reel has been loaded upside down. When the reel is spinning counterclockwise, the tape should only be momentarily flopping into the tape path. If the reel is found to be upside-down, the supply hub is turned in the clockwise direction until the tape clears the path. The door is then opened and the INVERT message is reported.

If the reel is not inverted, the hub locking routine can proceed. The supply hub motion is stopped and the hub lock solenoid is engaged. The hub is then rotated clockwise by applying a voltage ramp. As the hub rotates, three locking feet come up out of the hub and grab the tape reel, holding it securely to the hub. During this locking operation, the reel encoder flags and sensor serve as a check on whether the lock is a success. If the reel is properly locked on the hub, one of the encoder flags will interrupt the sensor beam as the voltage ramp is applied. After a successful lock, the hub lock solenoid is disengaged and the supply hub is free to spin again. This locking cycle is described in more detail later.

The supply hub is now rotated again in the counterclockwise direction in preparation for the inertia check. The inertia check is used to determine the size of the reel being loaded. This information is used to set up some autoload and servo parameters that can be optimized according to the reel size. The inertia check is performed by applying a step voltage to the supply motor at the instant a reel encoder flag breaks the sensor beam. The time it takes for the next reel encoder flag to come around and break the sensor beam is proportional to the inertia of the reel.

As the hub continues spinning counterclockwise, some additional error conditions are checked. The check for an upside-down reel is repeated. A check for the tape leader being stuck to the reel is done. In the same manner that tape continuously in the tape path signals an inverted reel, a tape that never breaks the tape-in-path sensor beam indicates that the leader is stuck to the reel. This can often occur because of static electricity or because the leader is jammed under the reel flange. If the tape leader is indeed stuck, the supply reel is spun counterclockwise at high speed in an attempt to free the tape end. Failure to free the tape leader at this point will abort the load process.

Next, the tape is ready to be threaded. The supply hub continues to spin in the counterclockwise direction, and the tape-in-path sensor is monitored for the tape leader. Once the tape leader is sensed in the tape path, the supply reel continues to spin for another half second (to pull the end of the tape back to the beginning of the tape path), at which point it reverses direction and starts feeding the tape down the tape path assisted by the air flow. The tape-in-path sensor is checked continuously to make sure the tape stays in the path during the feeding operation. If the sensor fails to detect the tape in the path, an error condition is flagged and the load is aborted.

As the threading proceeds, the speed sensor is monitored for activity. If the tape has been correctly fed down the tape path and has caught onto the take-up reel, the speed sensor begins to spin. The speed sensor is then used to calculate the amount of tape that is wrapping around the take-up reel. If activity is not seen at the speed sensor within a certain period, or the required number of wraps are not completed within another certain period, the tape will be pulled back out of the tape path by the supply reel and the autoload will be retried. The HP 7980A will attempt to load the tape in this manner five times before reporting failure to do so.

After it has been determined that the tape is properly threaded, the load fan can be turned off and the servo loops closed. The take-up and supply motors are driven slowly in opposition to tension the tape. The tension arm position is monitored by an analog-to-digital converter (ADC) and, once it has reached the center (0V) position, the tension loop is closed. The tension integrator is turned on and the loop is given about a half second to stabilize. Next, the microprocessor closes the velocity loop and digitally controls its operation. The tension shutdown circuitry is enabled to prevent the drive from damaging itself or the tape during some sort of catastrophic failure. Any failure to establish tension during this process will cause the load operation to be aborted and a MISLOAD reported.

The autoload process takes 30 seconds if all goes well. Then the drive can be put on-line and all normal reading

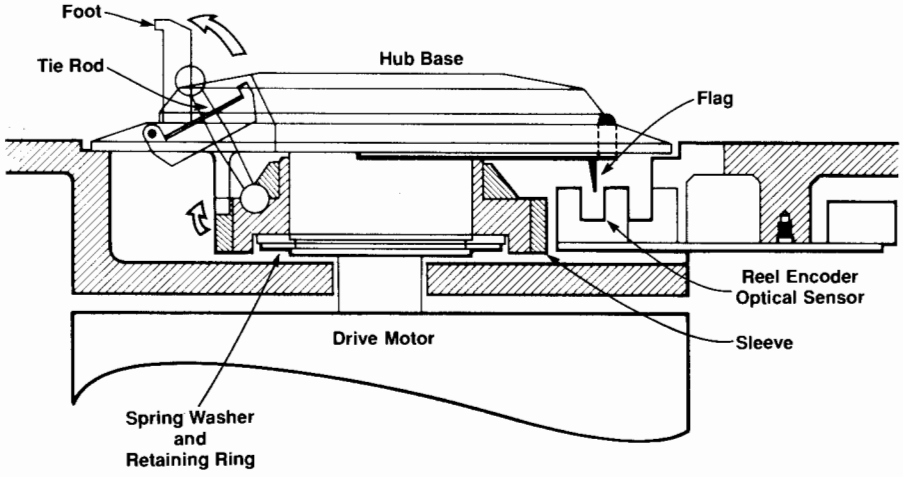

Fig. 4. *Cross section of supply hub. The foot is rotated upward and outward from the supply hub by holding the hub fixed and rotating the sleeve underneath. This causes the dumbbell-shaped tie rod to move from a slanted position to a position more upright, thus pushing the foot up and out. Reel encoder flags pushed down by the presence of a reel are sensed by the optical sensor to verify proper reel loading.*

and writing operations can be performed.

Hub Lock Mechanism

The first major objective in the autoload process is to determine the presence of, seat, and secure reels of tape. This process is complicated by the availability of four different sizes of half-inch-tape reels ranging in diameter from six inches to 10.5 inches, the latter being the most common size. The tape reel is secured onto a supply hub which suspends the reel at the proper height, holds it secure, and rotates the reel.

When the door of the tape drive is closed, the autoload algorithm starts immediately. The supply hub rotates in a clockwise direction and an off-center protrusion atop the hub contacts the inner race of the reel of tape. The rotational motion drags the reel in an inward spiral pattern until the reel eventually drops onto the hub's mounting plane. Three small plastic springs (the reel encoder flags mentioned earlier) mounted around the mounting plane are pushed down by the weight of the reel and trip the reel encoder optical sensor. The use of three springs assures planar contact of the reel on the hub, which helps prevent tape edge damage by keeping the reel as parallel as possible to the tape path. A fourth spring may be deflected by the write enable ring on the reel of tape to relay that status as well.

At this point, the reel is secured to the hub by means of three feet that rotate up and out of the hub to clamp the inner race of the reel. The feet are driven by a four-bar linkage that translates the rotational motion of the hub into a vertical rotation of the feet. At the end of their travel, the feet are locked into position in much the same manner as a toggle switch with an overcenter design.

The mechanism that drives the feet up and into place has four basic parts (Fig. 4). The first is the foot itself, which pivots about an axle swaged into the hub base. The foot is driven by a barbell-shaped tie rod which translates the horizontal rotation of the hub into the vertical rotation of the foot. The barbell, in turn, is driven by a sleeve-shaped part that fits around the base of the hub and is held in place by a spring and retaining ring. In normal operation, the sleeve rotates with the hub. During the reel locking stage, a solenoid engages an arm that stops the motion of the sleeve, and while the hub is rotated, causes the sleeve to rotate relative to the hub. The foot is pushed up and into place, depressing the wave spring when the foot contacts the tape reel. As the hub rotation continues, the barbell pops over center and starts to retreat. The relative motion at this point is ended by stops in the hub that limit the motion of the sleeve. The lock cycle is double-checked by the reel encoder optical sensors. Sensor placement is such that one of the plastic springs always interrupts the sensor at the moment the sleeve hits its stops. A neoprene pad embedded in the surface of the foot ensures that the reel does not slip relative to the hub. The hub is unlocked by simply reversing the process. In the case of a power failure, the entire lock or unlock cycle can be performed by manually turning the reel and engaging the arm.

Many obstacles had to be overcome to ensure a successful design. The first of these was materials selection. The material for the plastic springs must have a high endurance limit, low creep at moderately high temperatures, and a consistent and high spring constant. The material chosen was ULTEM 1000 by General Electric. Material for the sliding parts on the hub was tailored to minimize wear and friction, and to resist deformation under load. The second obstacle was cost. We made extensive use of design for manufacturability to decrease part count and minimize assembly time. The result is a hub with no screws that is completely assembled from one side.

Integrated Tape Path

All the tape path components, except for the reel motors, are mounted onto a precision head plate which is mounted on the deck casting. The magnetic tape head and the tape cleaner are permanently mounted onto the head plate in a manner similar to that used for the earlier HP 7978A Tape Drive.[4] This greatly reduces the number of tight tolerances required on the deck casting because of tape path requirements. The buffer arm and speed sensor assemblies are removable. This allows for easy replacement of the head plate, speed sensor, and buffer arm assemblies. Each of these assemblies is designed to be modular and interchangeable. There are no service adjustments on the HP 7980A because any adjustments required are done at the factory. No routine maintenance is required, except for regular cleaning of the tape path.

The tape path components perform several tasks in guiding the tape over the magnetic tape head. They make sure the tape is wrapped around the head properly and consistently. They also guide the tape past the head at a precise angle (skew) and at a proper height (tracking) so that the written tape is interchangeable with other tape drives. Normally, there are two precision stationary or fixed guides that perform these functions. The HP 7980A tape path incorporates one precision guide into the buffer arm assembly and the other guide is integrated with the speed sensor roller.

Speed Sensor

The speed sensor integrates the functions of an optical

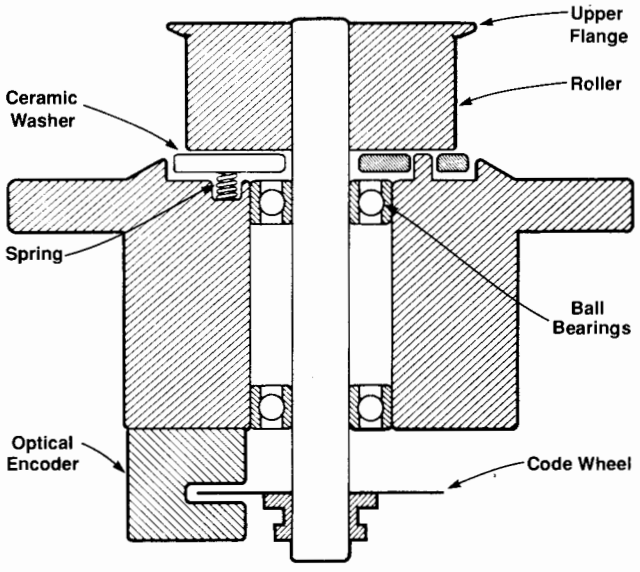

Fig. 5. *Cross section of speed sensor.*

encoder and a precision tape guide. The particular challenge was to create a rolling element, needed for transmitting tape speed to the encoder, that would guide the tape with the accuracy of a fixed guide.

Fundamentally, a rolling guide is simply a vertical cylinder with flanges on the top and bottom. The upper and lower flanges restrict the vertical limits of the tape's travel. According to the ANSI standard, the width of a half-inch tape must be between 0.496 and 0.500 inch. Clearly, the distance between the roller flanges must be at least 0.500 inch not to damage maximum-width tapes, but this allows a 0.496-inch-wide tape to wander 0.004 inch between flanges. However, in the simplified tape path the speed sensor must also guide the tape for proper skew and tracking across the head. This makes 0.004 inch of vertical wander unacceptable.

A traditional solution of this problem is to put a fixed guide between the roller and the head. A fixed guide is a nonrotating cylinder with a top flange set to a precise height. A spring-loaded washer pushes the bottom edge of the tape so that the top reference edge of the tape stays in contact with the top flange. This eliminates tape wander since the distance between the washer and the top flange can vary with tape width.

The HP 7980A speed sensor combines features of both rolling and fixed guides. Fig. 5 shows a cross section of the speed sensor. The roller, which includes a top flange, spins with the tape and transmits tape speed (through the shaft) to the optical encoder. The roller has no bottom flange, but there is a spring-loaded ceramic washer below the roller. The washer is restrained from rotating, but can move vertically to push the tape against the fixed height of the roller's upper flange. Thus, the roller is fixed vertically, but moves rotationally, while the washer is fixed rotationally and moves vertically.

To keep the bottom of the spinning roller from rubbing on the non-spinning washer, the roller width is slightly smaller than the minimum tape width. Thus, the semicircular arc of tape wrapped around the roller pushes the ceramic washer down and away from the roller. The spring is placed under the center of gravity of this semicircular arc of tape. This balances the forces on the washer so that it remains horizontal and does not damage the bottom edge of the tape.

Buffer Arm Assembly

The design of the buffer arm assembly presented several special challenges. The buffer arm assembly must provide tape buffering, proper tape tension, a servo position signal, proper tape guidance, and an overtension shutdown signal. The buffer must be lightweight enough to maintain servo bandwidth, but strong enough to hold the tape height within a tenth of a millimeter. Because the HP 7980A is an autoloading drive, the buffer arm must also act as an air dam to load the tape correctly. To achieve these requirements, a thin-wall aluminum die-cast part is used. Its flexibility allows an air baffle, a spring post, a stop, and a slot for overtension shutdown to be incorporated into a single part.

During testing, it was discovered that the tape resonant frequency dropped when the drive repositioned frequently. It was determined that during such reposition cycles more air became entrapped in the tape stack. As a result, the effective tape length was increased, decreasing its spring constant. To overcome this problem, a Coulomb damper is used. A cantilever spring is placed between the buffer arm and fixed guide so that it produces approximately four inch-ounces of frictional torque. This dissipates enough energy from the system to allow servo stability without affecting other parameters.

In a typical tape drive, the tape, after leaving the buffer assembly, enters a fixed guide for proper skew alignment. To minimize space requirements, simplify service, and reduce parts count, the fixed guide is combined with the buffer assembly. The buffer arm pivots about the center of the fixed guide as can be seen in Fig. 6. The fixed guide, made of a stainless-steel ring and two ceramic washers, is bonded on the buffer base to a 0.015-mm tolerance. This allows the buffer assembly to provide all the tape guidance in the front half of the tape path, but still be removed by loosening only three screws.

Another feature is the way the position of the buffer arm is sensed. The sensing assembly had to be small enough to pass through a 40-mm-diameter hole in the head plate, but require no adjustment if the buffer is replaced. To satisfy these requirements, a small ceramic magnet is mounted on the buffer shaft. Changes in the rotating magnetic field are sensed by a linear Hall-effect IC. The plastic magnet holder allows each magnet to be bonded in its correct calibrated position. With this arrangement a signal that is linear within ±8% over the buffer arm range is achieved, requiring no further calibration for interchange.

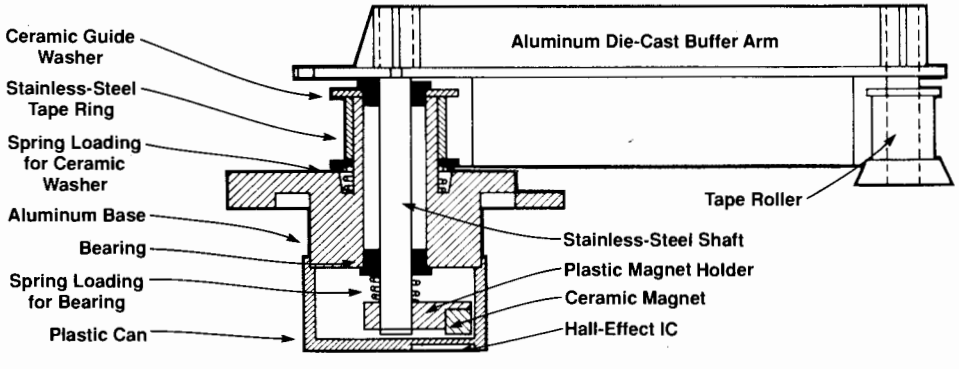

Fig. 6. *Cross section of buffer arm assembly.*

Design for Manufacturability

The HP 7980A tape drive is designed to be built easily. The major improvement over the previous HP 7978B drive is its size. The HP 7980A is about a third the size and half the weight of the HP 7978B. This makes it much easier to build and handle.

All of the major components are attached to the main deck casting. The main deck casting is moved down the manufacturing line as major components and assemblies are attached to it. It is then flipped over to add components onto the top and tested. Most of the components and assemblies are attached to the casting in a downward movement and fastened with a common self-tapping screw.

Reduction of parts is another major improvement. The number of mechanical parts was reduced from approximately 610 on the HP 7978B to 340 on the HP 7980A. The number of unique mechanical parts was reduced from approximately 260 to 140. All these factors help substantially reduce the time to build the HP 7980A. It is, therefore, a much more manufacturable machine than its predecessor, the HP 7978B.

Acknowledgments

Thanks to Hoyle Curtis and Don DiTommaso for obtaining the necessary funding for the success of the HP 7980A and for fending off additional features and configurations so the core system could be delivered on time.

There were many difficult mechanical issues during the design of the HP 7980A Tape Drive. Thanks to Tom Bendon for managing the resolutions to these issues. The many inputs from our manufacturing team were invaluable and contributed greatly to the manufacturability of the HP 7980A. Thanks to John Meredith, Gregg Schmidtke, Mel Crane, and Lee Devlin, our manufacturing team. Our tooling engineers, Dave Halbert and Jesse Gerrard, provided much needed input into the tooling and design of the many metal and molded plastic parts in the drive. Robert "Bob" Archer and Dave Lundgren did the early product design and Jim Dow did the industrial design. Dave Jones did the rack design and the HP 7980A rack slides. Many thanks to Dan Dauner for finishing the latter stage of the product design, which is the most difficult phase, and for wrapping it up for manufacturing.

To those not specifically mentioned, thank you for your contribution to the success of the HP 7980A.

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Streaming Tape Drive Control Electronics

by Bradfred W. Culp, Douglas R. Domel, Wayne T. Gregory, Jeffery J. Kato, Gerod C. Melton, Kraig A. Proehl, David W. Ruska, Virgil K. Russon, and Peter Way

IN DEVELOPING THE HP 7980A Tape Drive, the design team leveraged its expertise gained from the development of previous streaming tape drives. Design goals included a low factory cost, a small form factor, an autoloading capability, and a selection of interfaces. To achieve these goals, advancements were made in many key areas of tape drive design. These areas included the drive architecture, controller software, read/write electronics, tape servo system, and front panel.

Three-Box Control Architecture

The HP 7980A Tape Drive incorporates a control architecture based on the three major functional blocks of a streaming tape drive: interface, buffer, and drive. Each functional block contains a microprocessor-based controller and data path electronics to handle user data. Fig. 1 shows the three-box architecture of the HP 7980A.

Interface. The interface block handles all communications with the host computer. The HP 7980A contains an HP-IB (IEEE 488) interface. Currently, two other interfaces (PERTEC and SCSI) have been developed. Drives with one or the other of these interfaces are available as the HP 88780A. Each interface accepts tape commands from the host, transfers the user data, and returns the appropriate status. To perform a task, the interface first relays the tape command to the buffer controller. User data is then sent to or obtained from the buffer memory. Upon completion of the task, status is obtained from the buffer controller.

Buffer. The buffer block is responsible for streaming performance. The buffer controller oversees the use of the 512K-byte buffer memory. The buffer accepts tape commands from the interface and forwards them to the drive controller. The controller transfers user data between the interface, the buffer memory, and the drive's formatter. Status is obtained from the drive controller and forwarded back to the interface. Streaming performance is maintained through the use of immediate response on write operations and read-ahead on read operations. Immediate response on writes is implemented by the return of status as soon as a full record of data is accepted into the buffer, but before it is written onto the tape. This allows the host to free its memory and begin transferring the next record. When a write error occurs on the tape, the buffer will perform the necessary write retries independently of the interface and host computer. Read-ahead on reads is implemented by issuing additional read commands to the drive so that streaming is maintained until either the buffer is full, a command other than a read is received from the interface, or a read error occurs. This frees the host and interface from the constraint of performing all command and status processing overhead within the interblock gap time. Overhead processing time can be averaged out over several records. The buffer also performs all necessary read retries independently of the interface and host computer. Incorrect data is not sent to the host.

Drive. The drive block executes all tape commands. The drive controller oversees the servo system, motor drive, tape path, formatter, read/write, and front panel. The drive controller accepts tape commands from the buffer controller and executes them. User read data is read from the tape, corrected and checked by the formatter, and then sent to the buffer memory. User write data is accepted from the buffer memory, encoded by the formatter, and then written to the tape. Read-after-write occurs on all write commands to ensure error-free writes. Status is sent to the buffer controller. In executing a tape command, the drive controller must control tape speed, tension, and position. The drive controller relies upon the servo system electronics for closed-loop control of tape speed and tension. Tape positioning is performed in conjunction with the read electronics and formatter and is based on block boundaries. The drive controller also manages user requests and information through the front panel. User requests requiring buffer and/or interface involvement are passed to these functional blocks.

Each functional block is connected by a common communication link (CCL) to an adjacent functional block. The CCL encompasses common hardware and common soft-

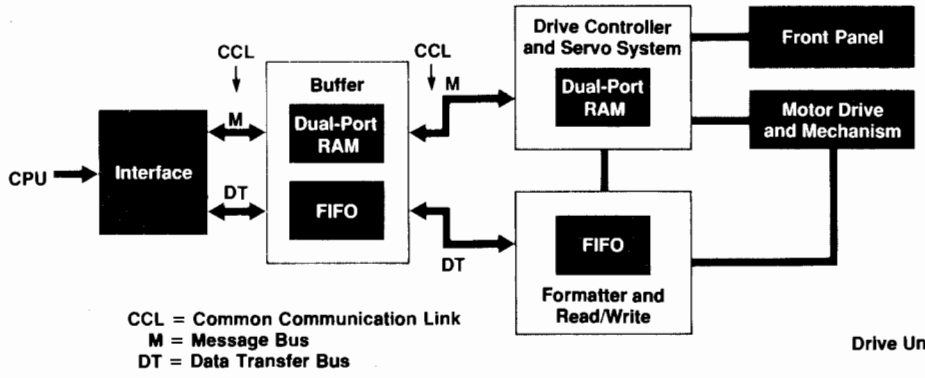

Fig. 1. *HP 7980A architecture.*

ware definitions. All of the optional interfaces communicate with the buffer using the same CCL. The buffer communicates with the drive using a similar CCL. The CCL software definition will be discussed later.

The CCL hardware uses a message bus for the transfer of commands and status, and a data transfer bus for the transfer of user data to and from the tape. The message bus interfaces the controller of a master functional block (closer to the host) to a dual-port RAM located on the controller of a subordinate functional block (closer to the drive). Fig. 1 shows the location of the dual-port RAM for each CCL. This dual-port RAM is directly and fully addressable by the microprocessors of both controllers. Commands and status are passed between the controllers by writing and reading specific memory locations. The data transfer bus interfaces the data path of a master functional block to FIFO (first-in, first-out) buffers located on the data path of a subordinate functional block. Separate inbound and outbound FIFOs are used to facilitate loopback testing. User data is passed along the data transfer bus in a sequential manner. Odd parity is maintained throughout with parity checking occurring as data is received across a functional boundary. An end-of-data bit is asserted to flag the last byte of each data record.

Interfaces

Important to the tape drive's acceptance by OEM customers (as the HP 88780A) is a selection of interfaces. The drive currently supports HP-IB, SCSI, and PERTEC. In the development of these interfaces, common hardware and software designs were shared. All three interfaces contain a 6809 microprocessor-based controller. About 30 percent of the circuitry is common to all three interfaces. As mentioned above, a common communication link definition is used to connect an interface to the buffer. Each interface completely isolates the rest of the drive from host, interface, and protocol specific requirements. By developing these interfaces in parallel it became clear what functionality belonged in the interface as opposed to the buffer or drive functional blocks.

The development of three sets of interface code in the time allotted for one was a major undertaking. There are 24K bytes of HP-IB code, 40K bytes of SCSI code, and 17K bytes of PERTEC code. Design time was reduced through the use of a common firmware architecture and the leveraging of common code. These interfaces share the same top-level firmware structure. About 6K bytes of code is common among the interfaces. The common code contains dual-port RAM communication routines and command processing of front-panel requests including diagnostics. With the exception of a power-on routine and a table-access module, all of the code is written in high-level languages. The use of high-level languages increased design efficiency and code readability. Overhead processing time became an issue with the PERTEC interface. Instead of rewriting the code in assembly language, overhead time was removed by rearranging the order of tasks during reads and writes. An increase in parallelism between interface and buffer was obtained, saving about two milliseconds per command.

The three-box architecture gives the HP 7980A and HP 88780A designers flexibility. Not only can new interfaces be easily designed and supported, but also options and enhancements can be added easily. For example, a new buffer design can be integrated without affecting any of the interfaces or the drive. Parallel development, debug, and test of the functional boxes increased design efficiency by minimizing the impact that problems in any one area had on the entire project. Because these boxes are functional entities, they could be turned on and debugged separately. Separate turn-on and debug included functional testing as well as the testing of communications with neighboring blocks. The integration of the first complete HP 7980A produced a working drive within a month.

Common Communication Link Software

The common communication link (CCL) is a single interface definition for two separate interface links. The HP 7980A contains three processors, a host interface controller, a buffer controller, and a device controller, performing specific tasks. The main function of the buffer controller is to intercept read and write commands and buffer the data within its data buffer to provide fast data access. For operations not involving data buffering or command queueing, the buffer controller typically passes the operation (command) directly through. By having common interface links on both the interface and the drive, the complexity of executing unbuffered commands is greatly reduced.

The CCL is designed to have a common command set for the half-inch tape format. Although the HP-IB interface is the primary host interface for the HP 7980A, the CCL command set does not preclude support of other interfaces such as SCSI, PERTEC, or a future high-performance interface. The buffer controller and drive controller implement a superset of commands that represents the operations needed to support most half-inch tape interface protocols.

CCL protocol is implemented by a 1K-byte dual-port RAM. This dual-port RAM is accessible by both the master (closer to the host CPU) and the subordinate (closer to the drive). Access is controlled by message control locations which synchronize the passage of messages across the CCL.

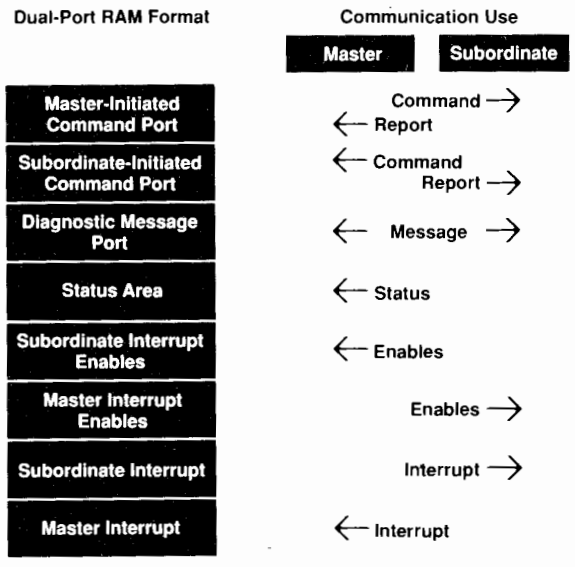

Fig. 2. *Dual-port RAM use.*

The dual-port RAM is divided into two command ports, a diagnostic message port, a status area, two interrupt controls, and two interrupt locations (see Fig. 2). The command ports support bidirectional command transfers. A master-initiated command port passes commands from the master to the subordinate, while the subordinate-initiated command port passes commands from the subordinate to the master. The master-initiated command port typically executes commands generated by the host, while the subordinate-initiated command port typically executes commands generated from the front panel.

A command port contains one of two message types: a command sent from the initiator or the report returned by the target. The contents of the command port are determined by a message control location.

The diagnostic message area is used during certain diagnostic operations when data messages larger than the command ports (64 bytes) need to be passed. A diagnostic message can be up to 512 bytes long, followed by a two-byte checksum.

The status area is used to maintain information on the drive that changes infrequently. This area contains information such as tape loaded, write protected tape, and the density of the current tape.

The interrupt control locations are used to specify areas of the dual-port RAM that require that an interrupt be sent notifying the other controller of any change in their contents. Interrupts are most often requested on changes to the command port message controls (indicating that a command is ready or a report has been returned) and changes to the status area. The use of programmable interrupts gives more freedom for each controller's implementation. The interrupt locations allow the master and subordinate to interrupt each other independently. The interrupt location is written with a value that indicates the area of dual-port RAM that has been changed.

The CCL commands are divided into six major opcode ranges: write, read, space, general, configuration, and diagnostic commands. Each command range is further subdivided into the individual commands supported within that group. For example, the write command group consists of write data record, write file mark, write gap, and write density ID. The opcode ranges simplify command decoding. Parameters on CCL commands are dependent on the opcode and vary in size from none to 57 bytes. For most opcodes, the number of parameter bytes is fixed. For example, the write record request opcode contains one three-byte parameter specifying the maximum length of the data to be sent, the write tape mark opcode contains no parameters, and the write density ID contains a one-byte parameter specifying the density to be written.

The report type returned on a CCL command depends on the command sent. All tape commands return a normal report containing status flags, tape position flags, a byte count field, a retry count, and an error code. The status flags quickly tell whether the command was successful, successful with error recovery, unsuccessful, or rejected. The tape position flags indicate the current position with regard to beginning of tape (BOT), end of tape (EOT), and end of file (EOF). The byte count contains the length of a write record or read record. The retry count indicates whether physical retries were needed during the operation, and the error code contains detail on a command failure or command rejection.

Non-tape commands return report types specific to their operation. For example, the diagnostic test commands return a diagnostic report that can contain the test number that failed, the failure code, and up to two field-replaceable units (FRUs) that could have caused the failure.

High-Performance Buffer Software

The HP 7980A is a high-performance streaming tape drive. It is also very flexible in its ability to be adapted to different environments and to use performance features in a variety of ways. High performance and flexibility of use in the HP 7980A are achieved by the features provided within the data buffer.

A streaming tape drive mechanism such as the drive controller requires a constant stream of data if it is to maintain high performance. In a typical host-drive interaction, irregular or slow data rates can interrupt the constant stream of data and cause the tape to stop and perform a costly repositioning cycle. The data buffer addresses the data rate problems by providing an asynchronous link between the interface and drive, allowing each to operate independently at its own data and command rates for limited time intervals. The HP 7980A has a large buffer in which to hold data as data rates are matched, making the asynchronous link possible. The buffer holds 512K bytes of data, enough not only to match variations in data rates, but also to allow the data buffer subsystem to accept data throughout a repositioning cycle at an average rate of 400 kilobytes/second.

The data buffer packs variable-sized records into its buffer and places an entry in a queue indicating the location and size of the corresponding record within the data buffer. The queue is large enough to allow the buffer to be completely filled without reaching queue limitations except on small records.

The buffer maintains two independent processes, one that interacts with the drive and another that interacts with the interface. Any transactions the host computer makes with the HP 7980A Tape Drive are made with the interface side of the data buffer. The host transaction is complete when data has passed between the host and the buffer and necessary reporting and status information has passed. The operations necessary to write or read the data from the tape occur independently of the host interactions.

During write operations data passes into the buffer from the host. As soon as data is in the buffer, the command is reported on with an immediate response report indicating that the operation is complete. The queue contains the size of each record. Data held in the buffer is then written to the tape automatically when a sufficient amount of data has been accumulated or when an appropriate time-out has occurred. The drive is streamed as long as data is available in the buffer.

When a read command is received from the host, the buffer goes into a read-ahead mode during which the drive side of the buffer controller issues continuous reads to the drive controller. Data passes into the buffer and reports are placed into the queue. This time they contain not only

record size, but also information regarding the success of the read attempt. Data is taken from the buffer and reports are taken from the queue to satisfy all read commands from the host. As data is removed by the interface, the drive tries to keep the buffer full, managing tape motion as necessary.

The queuing/buffering algorithm implemented in the HP 7980A allows a great deal of flexibility with the contents of the buffer. When data is read from the buffer, pointers are moved forward in both the data buffer and queue. Until the information is physically overwritten, it is possible to recover the information by moving the pointers back again. This capability is built into the read-ahead functions of the buffer controller. If a backspace command is received while the drive has been performing read-aheads, the buffer first attempts to recover the data by moving pointers back. This electronic backspace, as it is termed, gives a great performance advantage in that it eliminates the need to reverse the tape physically to position back one record.

Increased Buffer Flexibility. The data buffer has other features that provide greater flexibility in the use of its performance capabilities. Two of these features are greater access to buffer functions and the ability to change key performance parameters. Flexibility is also obtained through the use of manual buffer operations and through configurability.

Buffer operations described to this point involve two sides of the buffer. The drive side performs either delayed or anticipatory actions automatically to provide quick response to the host. Data is disposed of according to conventions in streaming conditions.

Manual commands offered by the buffer provide the same capabilities that occur automatically during a read or write operation, with each operation broken down into suboperations. During manual operations, only the specified suboperations are performed, with no automatic actions taken and with data disposition specified, not assumed. For example, a single write command is broken down into write-to-buffer, write-to-tape, and remove-record-from-buffer suboperations. Manual buffer operations are much more cumbersome to use and are not optimized for high-performance streaming, but offer flexibility in certain key areas such as diagnostics and in recovering buffered data.

Diagnostics make heavy use of manual commands. Data loopback operations are performed by writing to the buffer and then reading data back to the interface. The drive provides wellness and error rate tests using manual commands to write and read tapes locally. Diagnostic access to manual commands also allows access to buffer and tape operations from the front panel.

Recovering buffered data also uses manual commands. When a hard error occurs, or if the tape is stopped at EOT with unwritten data, the data in the buffer can be recovered by issuing read-from-buffer commands. Data recovery is not a typical operation, but is possible using manual commands. The flexibility of manual commands also allows current and future interfaces to implement interface specific operations.

The performance of the drive is dependent not only on the large buffer, but also on how the drive is set up to use the buffer. For example, parameters such as the trip point at which the drive starts writing data out of the buffer to the tape, the maximum record size to be written, or the length of time writes are held can all affect performance.

The HP 7980A is a highly configurable drive. Most variables that can affect performance and many that determine the personality of the drive can be configured and maintained within nonvolatile RAM on the buffer board. Configurations are used by the drive controller, the buffer controller, and the interface controller. A section of configurations is maintained and defined differently for each interface.

The configuration values are distributed to the appropriate subsystems when the drive is powered up. The interface also maintains default ROM configuration values. In the event that battery backup power is removed from the nonvolatile memory, default values are obtained from the interface.

Through configurations, a drive can be set up with a distinct personality and set of performance features for a particular user. The configuration system also maintains a set of locks which can be used to lock the configuration to the current value and prevent it from being changed.

Concurrent State Machines. The data buffer holds a special position within the drive in that it maintains CCL communications with four ports, three of them entirely independent. Each port has its own characteristics and needs.

The downstream interface port is the source of all host commands. Commands received here must be processed quickly since all streaming operations into and out of the buffer occur here. Streaming commands also have the characteristic that when one is received, the next command will probably be the same.

All streaming commands pass to the drive through the downstream device port. Quick response at this port is critical. If a command is not sent to the drive when a report is received, the drive controller may be forced to stop streaming and reposition the tape.

The upstream drive and interface ports are not independent since there is no queuing of upstream commands. Commands received from the drive are either fully or partially processed by the buffer controller. If necessary, they are then passed up to the interface controller. Commands received from the drive are irregular and are typically initiated as a result of human interactions. Hence, processing speed only needs to be fast enough for human response.

Resets can also be received as asynchronous events from either the drive or the interface. Resets are infrequent and, like upstream commands, do not require fast processing response like downstream commands.

The processing needs of the different ports led to an architecture within the buffer controller that allows maximum independence and specialization for the processing of each of the ports. Each major input source is handled by a separate program which controls the source and can be tailored to meet the streaming or background needs of each port. An operating system provides a set of concurrent processes for the programs to run within. Each program runs independently within its own time slice, with time apportioned for critical needs as they arise.

The programs are implemented as state machines and the operating system as a concurrent state machine driver. State machines have the characteristic that they perform an action when a particular event occurs, then proceed to the next state and wait for another event to occur. State

machines can be controlled effectively by an operating system. The operating system performs state transitions and calls to state execution modules. It also allocates time appropriately between the different processes during the waiting periods. Within the time slice given to each process, each of the potential events for the current state can be checked. If an event has occurred, the associated action for that event is also taken. Actions are coded as straight-line operations without loops. At the conclusion of an action, processing returns to the operating system for state transitions and for other processes.

The interface state machine handles all communication between the downstream interface port and the queue and buffer hardware. The drive state machine handles downstream communication between queue and drive port, including all automatic retries of tape operations. The subordinate state machine handles upstream commands in both the interface and drive ports. The reset state machine handles all resets regardless of location.

The operating system has no watchdog timer nor the associated timing and communication race conditions associated with unexpectedly losing the processor to another time slice. Instead, the operating system allows each process to complete its action before passing control to the next process. Time for the heavy needs of the interface state machine and the drive state machine is automatically allocated by allowing the processes to take the time that they need. Processes such as the subordinate state machine and the reset state machine are effectively turned off by having only a single event to check on. They have no complexity until the event occurs.

Each of the processes is independent, but each can have communication with other processes and affect their operation by passing messages or commands. All communication between processes occurs as events in the receiving process caused by actions in the sending process. Communication locations are tightly controlled data structures, the queue being a prime example. The receiving process looks at the communication locations for conditions that trigger events in themselves and that require action to be taken.

The buffer controller functions are divided into individual programs, which are independent, have their own specialization and definition of tasks, and have localized access to hardware, ports, and internal communication locations. This provides the structure needed to tackle the complex tasks of the buffer controller. Each of the pieces has defined functions and boundaries for good process definition and implementation.

Integrated Read/Write System

The design objective for the HP 7980A read/write system was to lower cost while improving performance over previous tape products. This objective was met through the reduction of printed circuit board space, the real-time optimization of read gains, the calibration of each read channel, and the simplification of the write electronics.

The HP 7980A read/write board replaces the equivalent functions of earlier read, write, and write formatter boards. This reduction in printed circuit board space was achieved

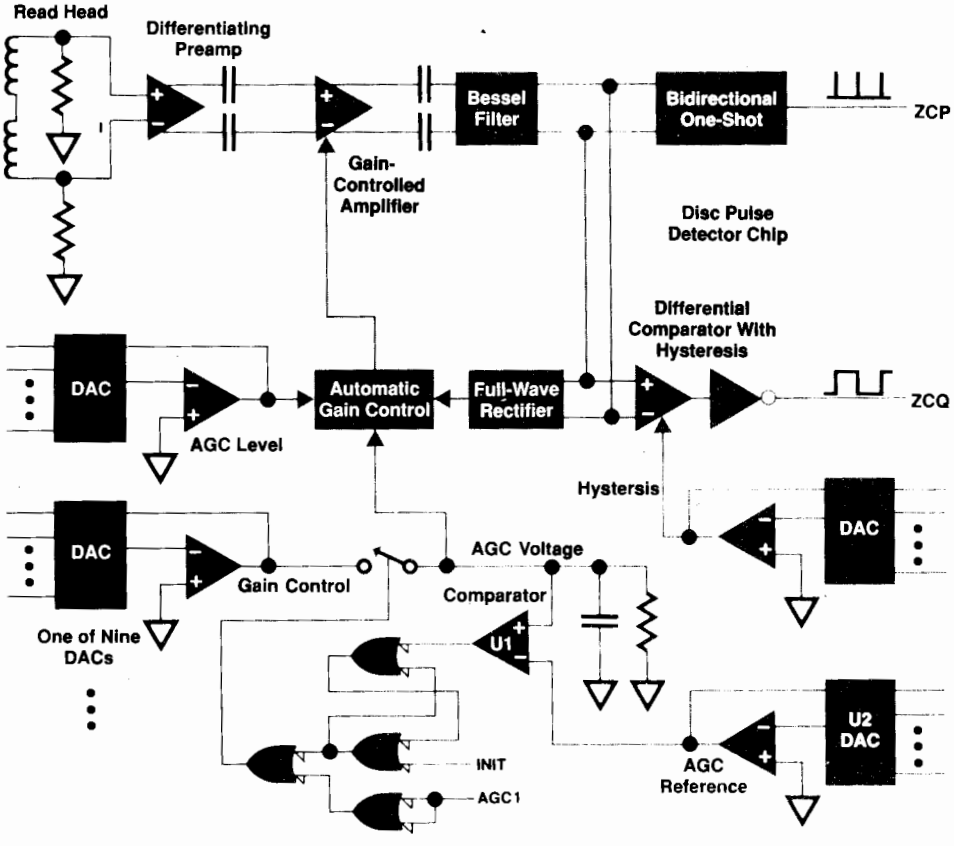

Fig. 3. *Analog read channel.*

by using surface-mount components, combining the preamplification and differentiation functions into one stage, using an integrated disc pulse detector chip, and developing a semicustom phase-locked loop chip.

The read channel shown in Fig. 3 consists of a differentiating preamplifier, a gain-controlled amplifier, an automatic gain control circuit, a gap clamp circuit, a zero-cross pulse circuit, a zero-cross qualifier circuit, a calibration circuit, and a fourth-order Bessel filter. The input to each channel is the output of a single-track read coil. Two signals, a zero-cross pulse ZCP and a zero-cross qualifier ZCQ, make up the output of each read channel. The zero-cross pulse is generated each time the differentiated input signal passes through zero. The zero-cross qualifier goes to a logical zero when the differentiated input signal becomes more negative than the lower hysteresis level and goes to a logical one when the differentiated input signal becomes more positive than the upper hysteresis level. This information is used by the phase-locked loop to recreate the digital data as it was recorded.

Differentiating Preamplifier. The preamplifier is an NE592 differential video amplifier configured as a differentiator. The 200-kHz (PE format) gain is set for 32 dB with a phase shift of 88 degrees, and the 555-kHz (GCR format) gain is set for 40 dB with a phase shift of 86 degrees.

A typical read channel has a preamplifier stage followed by an AGC amplifier and differentiating amplifier. To reduce board space and parts count, the preamplifier and differentiating amplifier are combined. The layout of the differentiating preamplifier is very critical to achieving high common-mode rejection and retaining a high signal-to-noise ratio. Fig. 4 shows the difference between the constant gain and the differentiating configurations for the NE592. In the differentiating configuration, any leakage capacitance from the junction of capacitor C1 and resistor R1 results in the two emitters seeing different impedances to ground. This unbalances the differential front end of the NE592, resulting in a decrease in common-mode rejection. The board layout techniques shown in Fig. 5 are used to reduce the noise level and retain the common-mode rejection of the NE592. The read and write sections have board-level isolation of 5V, ±12V, and ground. Each of the read-channel NE592 front ends has individual paths to the bottom ground plane, individual lines for power, and minimum trace runs near the differentiating preamplifiers. The head signals from the J2 connector to the NE592 inputs alternate between layers 2 and 3 which are located between ground plane layers 1 and 4.

Disc Pulse Detector Chip. The preamplifier is ac coupled to the AGC amplifier, which drives a differential input, fourth-order, passive Bessel filter. The output of this filter drives the AGC, zero-cross pulse, and zero-cross qualifier circuits. The AGC circuit measures the input signal and compares it against the AGC level (an external dc voltage). This voltage difference controls the gain of the AGC amplifier to make the peak-to-peak differential voltage output of the Bessel filter equal to four times that of the AGC level. The differentiating preamplifier turns peaks into zero-cross data so that a comparator can be used to locate the read signal peaks. If the read signal exhibits a tendency to return to the baseline between peaks, the comparator could respond to noise near the baseline. To avoid this problem, a zero-cross qualifier circuit is used. This circuit is a comparator with externally controlled hysteresis. The differential signal must go above or below the dc hysteresis value before the comparator will switch states. The comparator output is fed to the phase-locked loop as zero-cross qualified data. The output of a bidirectional one-shot is fed to the phase-locked loop as zero-cross data that indicates the start of a data window. The phase-locked loop uses the zero-cross data to generate a pulse that is half a bit window long. This pulse is used to clock the zero-cross qualified data into a latch. The output of this latch represents the data as it was put on the tape.

Automatic Calibration. During track activity (data records), each track independently adjusts its gain via the AGC voltage to an optimum amplitude. The AGC voltage required by each channel while reading data is determined using comparator U1 and DAC U2 as shown in Fig. 3. During gap conditions (no track activity), the AGC voltage is overridden by individual gain control DACs. This allows each channel to be preset to a gain that produces an output signal of optimum amplitude if a nominal input signal is present. Detection of data by the phase-locked loop signals the channel to enter the AGC mode until another gap is detected or the gain increases above a predetermined value. DAC U2 and comparator U1 in Fig. 3 are used to determine when the gain is above the predetermined value. During writes the gain is also held constant so that low-amplitude read signals cause a write retry.

Track-to-track variation in the AGC voltage is dependent on the head and read channel combination and is independent of tape-to-tape variation. Track-to-track variation (gain profile) from a high-output tape to a low-output tape can be closely modeled using a single gain offset value across all tracks. Gain profiles of GCR and PE densities differ, and therefore require separate gain profiles for each density. Automatic calibration is performed at the beginning of each tape when the tape density is being identified or being written. This calibration in GCR involves all nine tracks

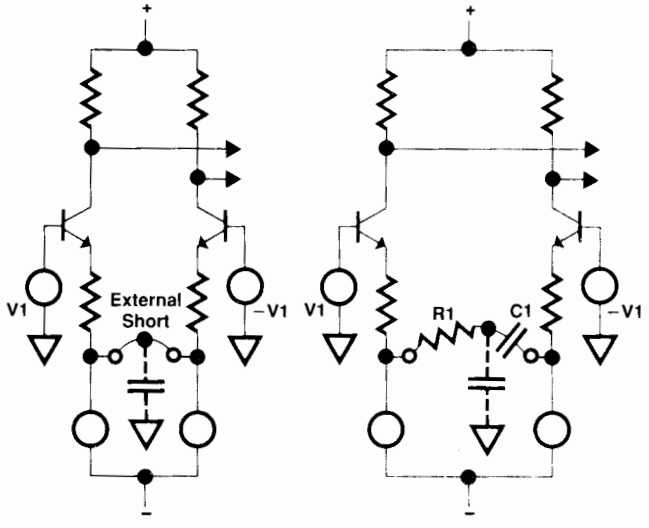

Fig. 4. *Constant gain (left) and dv/dt (right) configurations for NE592 preamplifier.*

during the ARA burst portion of the GCR density ID, while in PE it involves only the PE density identification track. Reference DAC U2 in Fig. 3 is stepped upwards until comparator U1 indicates the reference voltage is equal to the AGC voltage for this track. This procedure is repeated two more times and the median voltage for each track is saved as one of the raw gain voltage levels for the current tape. The average gain of the raw gain voltage levels is calculated and saved as one of the average gain voltage levels for the current tape. A gain profile calibration is performed using the tape drive diagnostics. An all-ones pattern at the appropriate density is written for 100 feet beginning at BOT. The pattern is read and the gain voltage for each track is determined 256 times. The average gain voltage for each track is the gain profile for the specific density. Each time the average gain voltage level is calculated during a tape ID routine, the gain profile for the specific density is normalized such that its average value across all nine tracks matches the average gain voltage level for the current tape.

Standard Cell Phase-Locked Loop. When we decided to do a follow-on design to the HP 7978A Tape Drive, our experience with its design afforded us a great opportunity to make technological advancements in the areas of price, performance, and reliability. With this in mind, we selected areas of the HP 7978A design where we could get the best return using some sort of LSI integration. One area was in the clock recovery section of the HP 7978A.

Designing a multidensity phase-locked loop for a nine-track tape drive presents a problem when one is trying to minimize cost and maximize performance. However, with this as a design criterion, it was evident that some sort of integration was needed. What we decided on was a digital/analog hybrid phase-locked loop design. This gave us the flexibility to set important third-order loop parameters using normal analog loop parts, that is, an op amp, filter, and VCO. We then wanted to use LSI technology to integrate all the digital logic associated with the recovery scheme. We chose HP's own CMOS standard cell process whose density allowed us to put three tracks of phase-locked loop logic into one chip, and thus use only three chips per system.

The major elements of the standard cell are shown in Fig. 6. Two programmable digital delay lines are used in the multidensity design, one for qualification of incoming read channel flux data, the other for calculating the phase error to be used by the phase detector. A pattern detector is used to detect the presence of data to control the phase-locked loop as well as the automatic gain control circuitry of the read channel. A two-state phase detector that can switch between frequency-lock and phase-lock modes virtually eliminates the chances of a harmonic lockup. An output encoder is used to synchronize all the channel out-

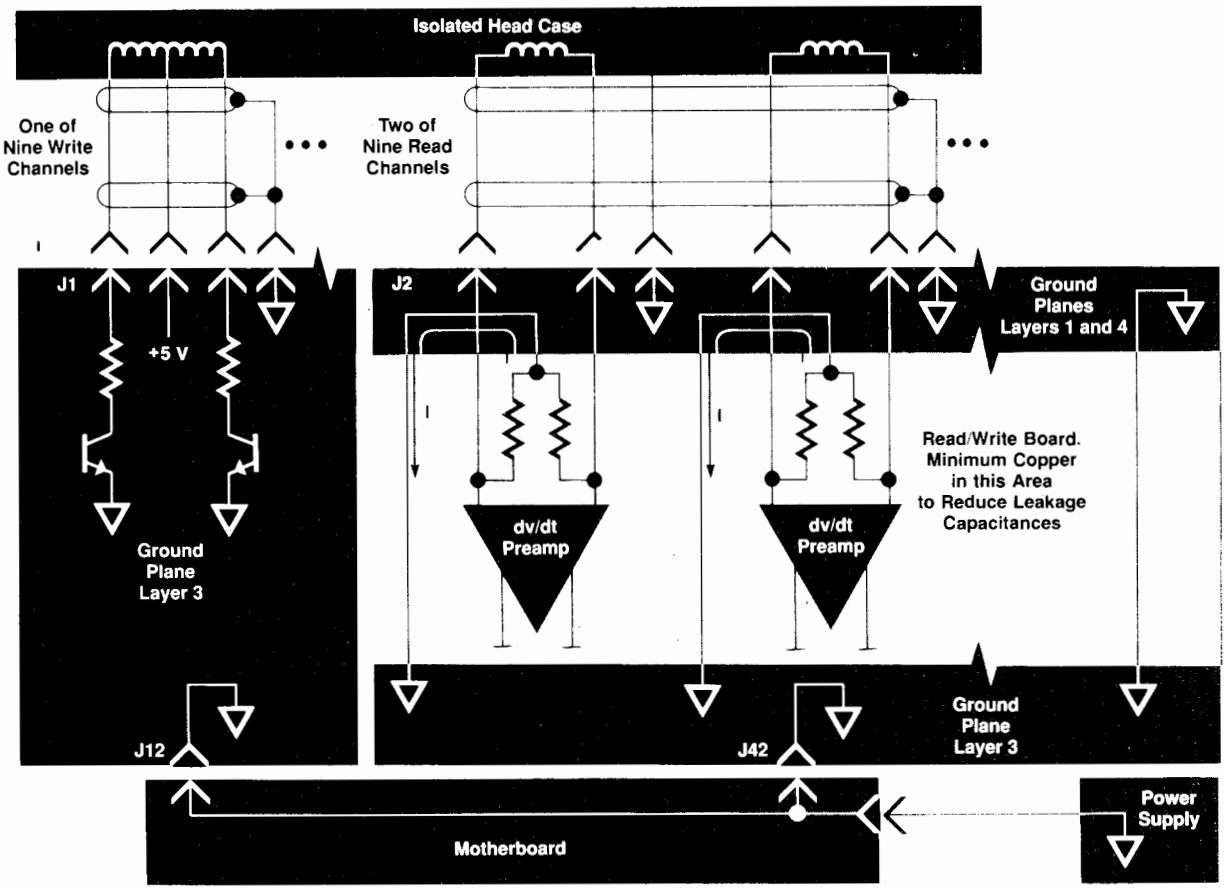

Fig. 5. *The layout of the ground planes for the NE592 front ends is critical for reducing noise and maintaining common mode rejection.*

puts with a common system clock. The bus interface section contains four control registers for full microprocessor controllability. A center-frequency generator provides a reference when there is an absence of data.

The standard cell is implemented using HP's CMOS process. The implementation and testing of parts took only six engineer-months. Our first silicon version was production quality. Because the chip was flexible and usable the first time, we designed it into the HP 7978B as a cost-reduction action before the HP 7980A was introduced. The cost savings achieved in the HP 7978B was enough to pay for the chip's development cost. The gains achieved in the HP 7980A over the original HP 7978A phase-locked loop include a reduction in printed circuit board area by a factor of 10, an improvement in reliability by a factor of 8, a reduction in factory cost by a factor of 5, and an increase in performance by a factor of 2.

Digitally Controlled Write. Each of the nine data signals from the write formatter is turned into two write currents, each driving one half of the write coil for one track. The positive half of the write current is controlled by the signals GCR, PE, and COMP while the negative half is controlled by the signals GCR*, PE*, and COMP*. These six signals are generated for each channel by a PROM which is driven by common address signals comp, bp/g*, and dack. The other two address lines, data-1 and data-2, are channel dependent. data-2 lags data-1 by one bit window time period, allowing the PROM to know the value of the preceding data bit. For data equal to one, GCR is asserted for the full bit window time. PE is asserted for 100 percent of the bit window time in PE mode but for only 16 percent of the bit window time in GCR mode. If the preceding bit was a zero, COMP is asserted for 80 percent of the bit window time in GCR mode or for 90 percent of the bit window time in PE mode. For data equal to zero the control signals GCR* and PE* are asserted instead of the signals GCR and PE. If the preceding bit was a one, COMP* will be asserted.

Each track has two groups of three control signals. These signals control a group of three open-collector drivers. The open-collector drivers are connected to one end of a write coil through current-limiting resistors. The center tap of each write coil is connected to 5V. The half-coil current is then the sum of the three currents generated by each open-collector driver pulling its resistor to ground. This technique allows the write currents to be generated using 5V TTL logic.

To guarantee the write and erase currents will turn on only when commanded to, a POWER GOOD signal is hardwired to a protection circuit. The POWER GOOD signal is a signal from the power supply which will not be valid until voltages are at rated values. The protection circuit turns on an enhancement mode n-channel MOSFET which supplies five volts to the center taps of the nine write coils.

The same type of circuit is used in the erase circuit to turn on an npn transistor which provides a ground for the erase circuit. The dc erase current must ramp to the steady-state current in less than 0.2 ms and stay at this value until turned off. The erase current is controlled by two circuits. The two circuits operate in parallel until the steady-state current level is reached. The ramp circuit is then turned off, leaving the steady-state current circuit on until the erase circuit is turned off.

Hybrid Servo System

The HP 7980A servo system loads and unloads the tape automatically, controls the tape velocity and tension, and performs diagnostic functions. The drive controller uses the servo system in conjunction with the read electronics and formatter to perform accurate control of tape position. The servo moves the motors independently during the tape loading process under the control of a 6809 microprocessor. Sensors monitor the progress of the tape and check for error conditions. Tension is established and the velocity and tension servos are enabled. The tape is under closed-

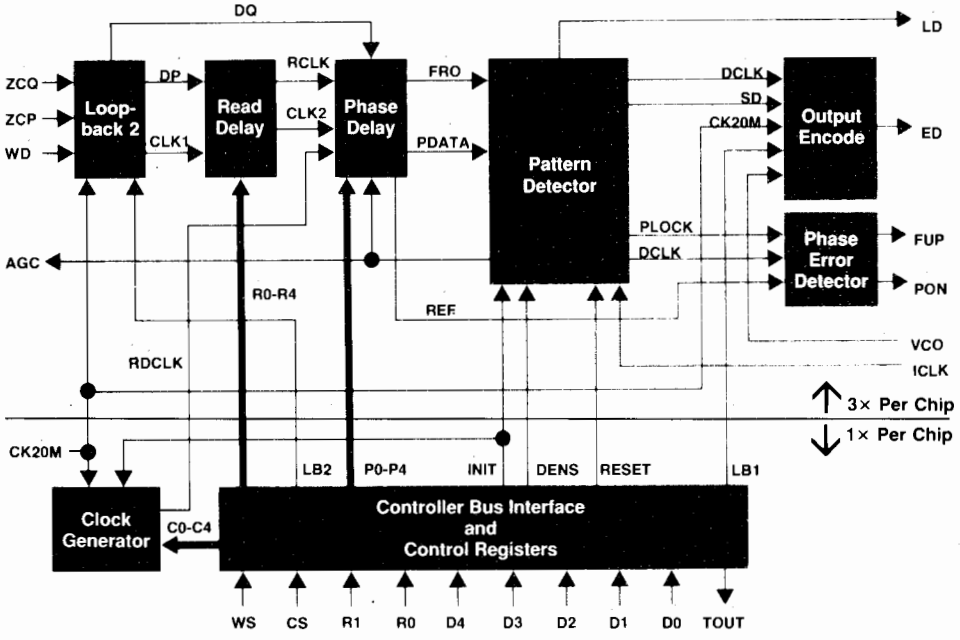

Fig. 6. *Block diagram of standard cell for phase-locked loop chip.*

loop control thereafter. The tape velocity is primarily controlled by the take-up motor, and the tension is controlled only by the supply motor. A block diagram of the servo system is shown in Fig. 7.

Closed-Loop Operation. Tape velocity is controlled by an integral plus proportional control scheme. This yields a zero steady-state velocity error. The long-term tape velocity error is well under one percent. The controller is implemented as a digital-analog hybrid to take advantage of the best features of each type of control. In the HP 7980A, a design requirement for the servo is that the 6809 microprocessor be able to manage all the drive control functions and also control the velocity with minimal involvement. For this reason, the error signal and integral portion of the loop are performed by the processor, and the proportional feedback and multiplication by coefficients are performed by analog circuits. An optical position encoder is used by the processor to measure linear tape velocity. This is done by counting the number of pulses of the encoder every 5 ms. The measured velocity is compared with a velocity command at each sample period and accumulated over time. The resulting value is sent to a 12-bit DAC. The processor has complete control over the velocity of the tape by changing the value of the velocity command. This scheme performs the integral portion of the control with high accuracy. The processor involvement is minimal because only simple fixed-point additions and subtractions are required. The proportional part of the control is done in analog form. The optical encoder drives a tachometer circuit which gives a bipolar voltage proportional to tape velocity. The tachometer circuit does not have to be very accurate since it is only used to generate a proportional feedback term. The velocity control accuracy is determined by the integral term computed by the processor. The integral and proportional terms are summed with appropriate scaling factors by an operational amplifier and the resulting signal is then sent to the motor amplifier.

The output voltage of the velocity controller drives the take-up and supply motors. This reduces buffer arm deflections during velocity ramps. If the velocity and tension servos were completely decoupled, the velocity servo would start a ramp with the take-up motor, and the tension arm would then deflect and start a ramp of the supply motor. This would require large arm deflections. In the HP 7980A the velocity control voltage is scaled and sent to both motors. The buffer arm then only needs to deflect a small amount to correct the tape velocity at the supply motor.

The variable-velocity rewind is an important feature of the HP 7980A tape drive because it allows a reduction of rewind time for a 2400-foot reel from 120 seconds for a constant-velocity drive to 90 seconds. The maximum rewind velocity attainable by a tape drive primarily depends on the maximum voltage available to drive the motors. Each motor generates a back emf proportional to its angular velocity. This back emf counteracts the supply voltage and limits the maximum angular velocity the motor can achieve.

The tape radius of this tape drive can vary over a 2:1 ratio from beginning of the tape to its end. At each end one or the other motor can limit the maximum rewind velocity attainable to about 250 ips. In the middle of the rewind, the tape radius for both motors is roughly equal, and the tape can attain velocities of over 400 ips. In the HP 7980A, the processor maximizes the velocity of the drive during rewind by reading the voltages sent to the motors with an ADC, comparing them against the supply

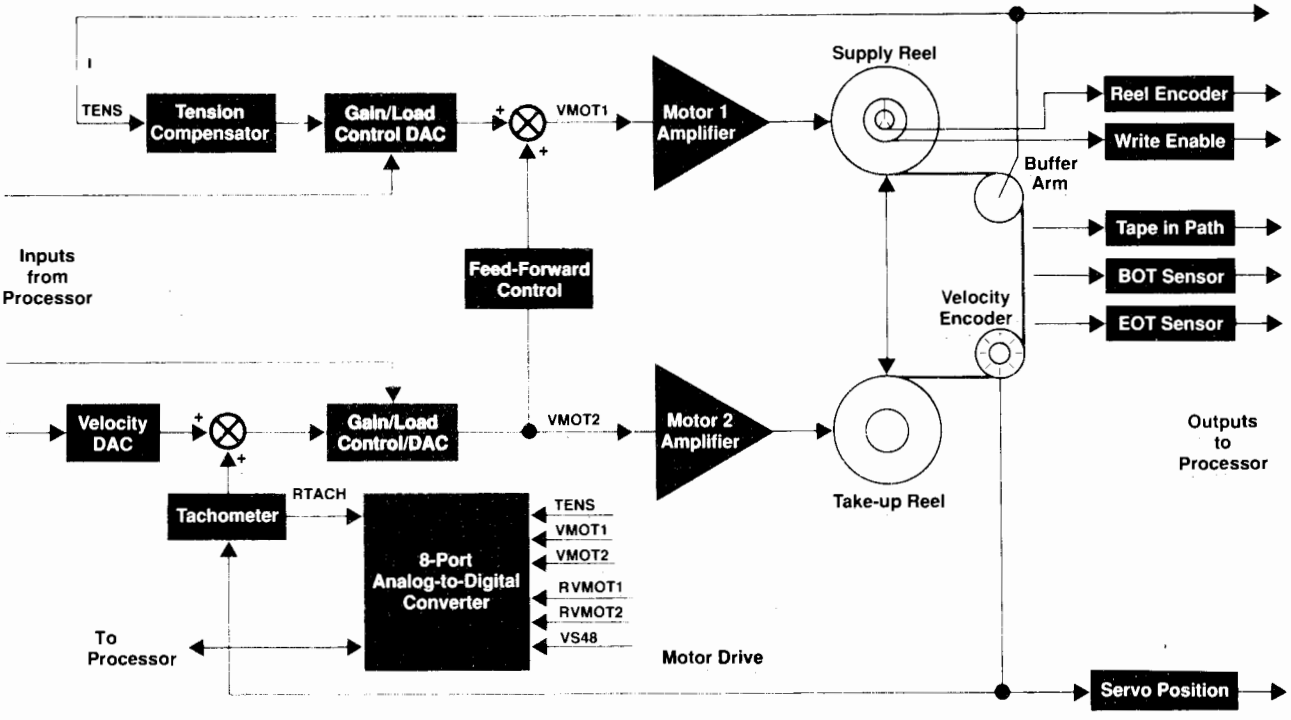

Fig. 7. *Block diagram of servo controller.*

voltage, and adjusting the servo velocity command several times a second to use the available supply voltage most effectively. Both servo loops operate at all times; only the velocity command is varied during the rewind.

The tension loop measures the deflection of the buffer arm and corrects the velocity of the supply motor until the arm returns to its nominal position. This effectively matches the linear tape velocities at both reels as the tape winds from one reel to the other. If both reels were identical, no buffer arm deflection would be required. The buffer arm applies a relatively constant force of 10 ounces to the tape and thus passively controls the tension. The arm force is constant as the arm travels ±1 inch. The velocity and tension loops are approximately decoupled since each motor sees a relatively constant load of 10 ounces.

The tension loop is implemented completely in analog form. The buffer arm uses a linear Hall-effect sensor and a magnet to convert position to a voltage. This voltage is processed by an analog compensator and combined with the velocity control voltage to drive the supply motor. The key feature of the compensator is that it has an integrating term. This always returns the arm to its null point after a ramp. It also reduces arm deflections during ramps and eliminates final velocity-dependent arm deflections. If the integrating term were not present, the high rewind velocities of the HP 7980A would not be attainable.

Open-Loop Operation and Tape Sensors. The autoloading feature of the HP 7980A requires individual control of the two motors until the tape is loaded. The velocity and tension control loops are each followed by a gain/load control stage. In the gain mode, this stage can output a voltage proportional to an 8-bit number. The processor can perform the autoload operations in this mode. When the loops are closed, these stages are switched to the gain mode. In this mode they operate as programmable gain stages. The processor can adjust the velocity and tension loop gains to account for different reel sizes. The gain/load stage is implemented with an 8-bit multiplying DAC. In the gain mode, the voltages generated by the servo loops are fed to the reference inputs of the DAC, and the processor adjusts the loop gain by writing to the DAC. In the load mode, the reference voltage is fixed, and the processor controls the motor drive voltage by writing to the DAC.

Several sensors monitor the progress of the tape during the autoload process. A three-line encoder on the supply hub has several functions. It determines whether the feet on the supply hub have properly engaged the reel, it determines the presence of the reel, it is used to control the velocity of the supply hub during the tape threading operation, and it is used by the processor to determine the reel inertia. The three-line encoder is also used with the velocity encoder during closed-loop operation to determine the supply reel radius instantaneously.

The beginning-of-tape (BOT) and end-of-tape (EOT) signals are determined on half-inch tapes by reflective markers. The markers are detected by the tape drive using two reflective sensor assemblies. Some tapes are almost as reflective as the markers, and this has been a problem for marker detection circuits. The HP 7980A employs a circuit that responds to changes in reflectivity, rather than absolute levels, to detect the markers. This means that the circuit is insensitive to component variations and can handle a wide variety of tapes without adjustments. The circuit is shown in Fig. 8. The sensor consists of an LED and phototransistor pair. The phototransistor receives infrared light generated by the LED which bounces off the tape. As a marker passes the sensor, the phototransistor emits a current pulse. This current is converted to a voltage V1 by amplifier A1. V3 is an attenuated version of V1. V2 is a filtered version of V1. A2 is an amplifier used as a comparator. A sufficiently large pulse at V1 will cause a pulse at V_0 since V2 does not rise as rapidly as V3. The output does not respond to slow variations in tape reflectivity or extraneous light sources, but it does respond to the rapid change across a reflective marker.

A tape-in-path sensor determines when tape has entered the path. The sensor is a phototransistor and LED pair that shines infrared light across the tape entry point near the supply reel. The sensor is designed without adjustments by using a pulsed technique for detection. The detection circuit is similar to the circuit of Fig. 8. In this case the LED is pulsed by the processor for a short time with high current. If there is tape in the path, no output is detected at V_0. Otherwise, a fast change is detected at V_0.

An eight-port ADC is used to perform diagnostics on the analog circuits. It measures the buffer arm position during load and signals the processor to close the servo loops. It measures the motor voltages during rewind to adapt the rewind velocity. It is also used during self-tests to perform a motor-drive loopback, a tachometer loopback, and a 48V supply voltage check.

Tape Positioning Control. Unlike a stop/start drive, streaming tape drives do not have the ability to stop and then restart the tape within the distance of an interblock gap. Each time the tape is stopped, a streaming tape drive must reverse the tape until it is well ahead of the next record to be read. The tape can then be ramped up to speed and the read electronics activated upon reaching the interblock gap where stopping was initiated. While stopping and starting the tape the read head may traverse an unknown number of records. Unfortunately, the 6250 GCR and 1600 PE tape formats do not support a standard mechanism for identifying individual records. Therefore, tape repositioning must be performed based on physical distance along the tape. The HP 7980A Tape Drive uses an optical shaft encoder mounted to the capstan wheel in the tape path. This en-

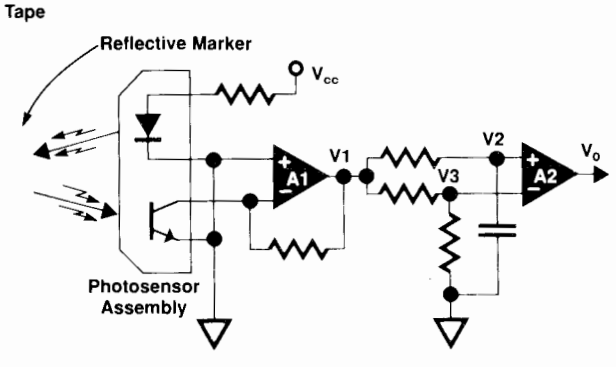

Fig. 8. *Beginning and end-of-tape sensor circuit.*

coder provides two quadrature pulse trains. A quadrature decoder chip (QDC) converts these pulses into a relative tape positioning count with the use of an up/down counter.

Because of the high density and small gap size of the GCR recording format, it is important that relative tape positions supplied by the QDC be as accurate as possible. When a block-to-gap or gap-to-block boundary is sensed by the read circuitry, it is essential that the position obtained by the QDC at that instant be captured and stored away for later use. Although the QDC is a bus-compatible device, time delays from the occurrence of a block boundary to the point at which the microprocessor senses that event and reads the position can introduce unacceptable errors. To avoid the latencies caused by the additional microprocessor cycles, position capture circuitry was designed around the QDC. This circuitry monitors inputs from the read formatter which signal when a block boundary has been crossed. When the event occurs, external hardware extracts the position information from the QDC and stores it in the appropriate location of a 4×12-bit register file. The position is captured within 2.4 μs of the event. This translates into a maximum position error of only 0.0003 inch.

Upon stopping the tape, the last valid block-to-gap position is used to mark the gap that follows the last block read. The tape is stopped, then restarted in reverse. Monitoring the up/down counter, the drive controller waits until the read head is in the target interblock gap. The read electronics is then activated and the tape position at the next gap-to-block boundary is latched. This position will be the same as the block-to-gap position previously latched plus any positioning error encountered in stopping and starting of the tape. The tape is then brought to a stop and restarted again in the forward direction upon receiving a new read command. Again, using the up/down counter to monitor tape position, the drive controller activates the read electronics in the interblock gap before the next record to be read. By recapturing the block-to-gap position in reverse as a gap-to-block position, the drive controller prevents the accumulation of tape positioning error. Each time a position is recaptured, the amount of positioning error is calculated by subtracting the two tape position counts. If this error becomes excessive it is reported to the host, thus indicating a problem with the drive.

Vacuum-Fluorescent Front Panel

We had two basic objectives in designing the HP 7980A's front-panel display. The first was to provide an HP-quality solution, especially since the display is a focal point for the user of the drive. We analyzed a number of factors, ranging from the angle of the display to its color and clarity. The second objective was to provide a convenient means of displaying tape drive status that would be viewable from across the length of an average computer room. Because of the long-distance viewing requirement, special attention was placed upon character size, color. and contrast, and upon the physical placement of annunciators. After a thorough analysis of the options available to us, we converged on a design employing a vacuum-fluorescent display.

Display Operation. In simple terms, the vacuum-fluorescent display (VFD) is a directly heated triode vacuum tube. The VFD consists of an electron-emitting cathode filament, a screened phosphor anode, and a grid (located between the anode and cathode) to control electron flow. Therefore, the VFD is structurally similar to old radio or television vacuum tubes, yet it performs a totally different function. Besides the fact that VFDs are optical displays and not amplifiers, VFDs are often constructed with multiple triode structures included within the same evacuated tube. This feature allows the implementation of cost-effective, complex displays. Examples of these inexpensive yet complex VFDs can be found in all areas of modern consumer electronics.

VFD segments are illuminated when electrons emitted by the heated cathode (filament) are accelerated by the positively biased anode and are allowed by the positively biased grid, or mesh, to collide with the screened phosphor. This causes photons to be emitted from the phosphor at a frequency that depends on the type of phosphor used. This feature allows the design of multicolored displays by screening different phosphor patterns on the same display. Although this multicolored feature is attractive, it is not totally free. Standard available phosphors emit photons at luminous efficiencies that can vary by as much as 50 percent. This causes a brightness balance problem between different phosphors on the same display. Brightness is typically balanced using optical filters, different power supplies, or different duty cycles.

The cathode filament, a thin oxide-coated tungsten wire, emits thermal electrons when heated to around 600°C by a filament power supply. The filament power supply is a major part of the power consumed by a VFD.

The VFD display used in the HP 7980A (Fig. 9) uses an ac filament supply providing 2.8Vrms and 0.47W at 715 Hz, a 30Vdc, 0.6W power supply which provides power for the anode and grid drivers, and a 40-pin IC which provides level shifting (0-5V to 0-30V) and digital control for 18 anodes and seven grids.

Why a Vacuum-Fluorescent Display? There are five reasons for choosing a vacuum-fluorescent display—cost, reliability, versatility, market separation, and human factors. The VFD is very cost-effective compared to other options available. One other display technology, the liquid-crystal dis-

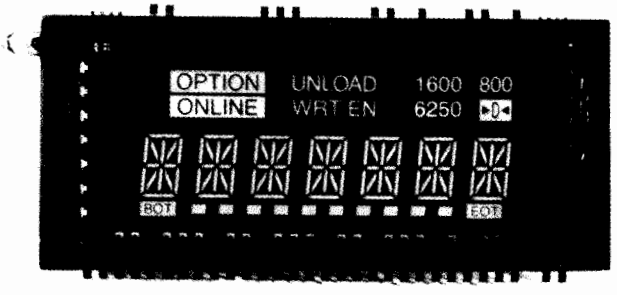

Fig. 9. *Vacuum-fluorescent panel of HP 7980A.*

play, was slightly less expensive, but caused concern regarding low-light viewability and electrostatic discharge sensitivity during assembly.

Reliability is probably the VFD's greatest asset. With a glass-encased body and an evacuated interior, it is impervious to electrostatic discharge damage and can endure harsh environments. Its low power consumption relative to LED displays also allows enhanced reliability.

Since the VFD's light output is multicolored, it can be easily filtered to almost any color desired with standard colored lenses. In the HP 7980A Tape Drive, the blue-green output is filtered to almost white without significantly affecting the amber light output.

Many other tape drives have LED displays and annunciators. By using a more consumer-oriented display (the VFD is standard fare on VCRs), we were able to achieve a more contemporary look.

The contrast of the VFD's bright phosphor with the dark filtered background gives excellent viewability from up to twenty feet while not being too bright at close range.

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