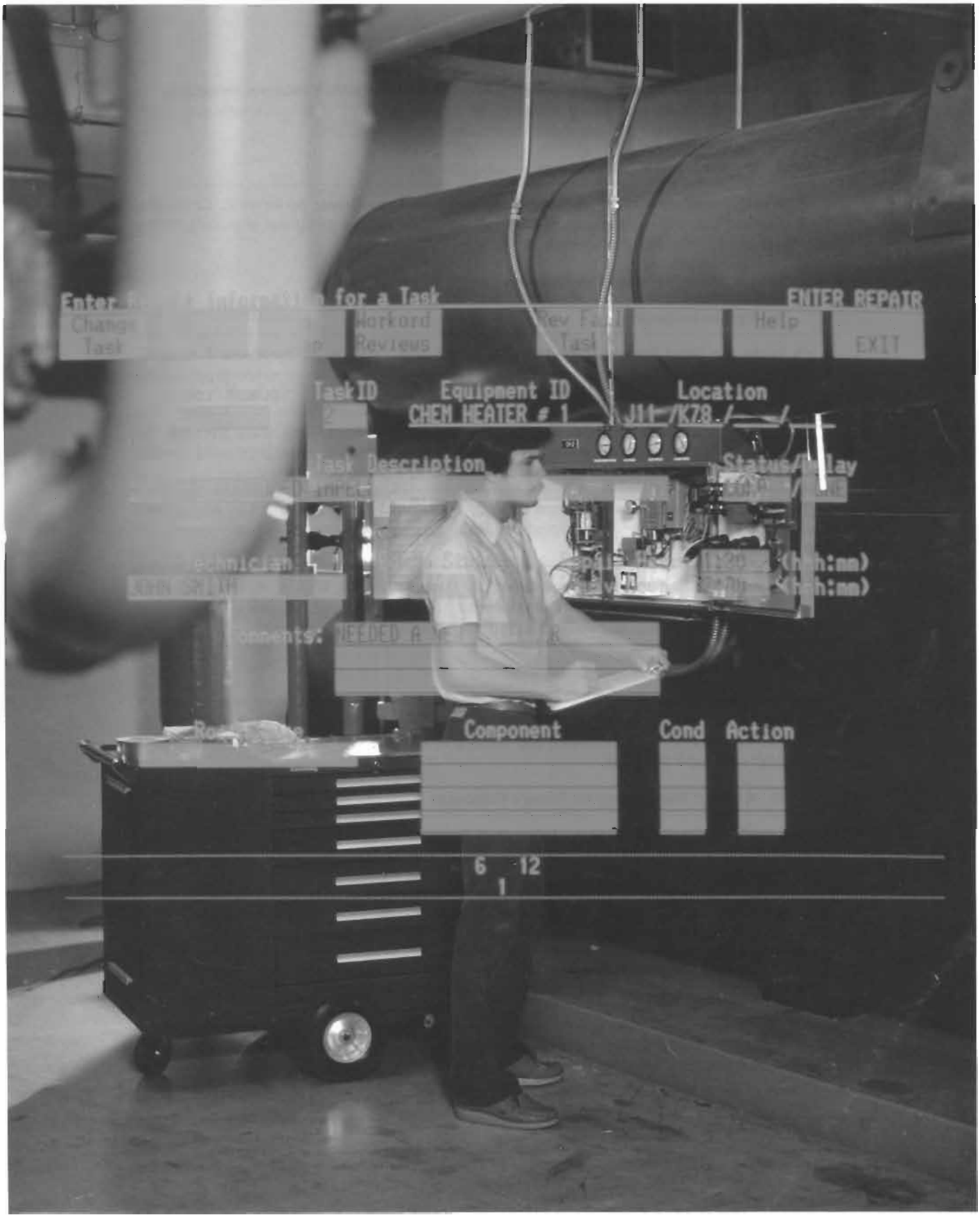
HEWLETT-PACKARD
JOURNAL

MARCH 1985



Low-Cost, Highly Reliable Tape Backup for Winchester Disc Drives

Designed for use on small to midrange computer systems, this new quarter-inch cartridge tape drive packs up to 67 megabytes onto a single cartridge.

by John C. Becker, Donald A. DiTommaso, and Sterling J. Mortensen

AS WINCHESTER DISC DRIVES have dropped in size and price, a matching backup peripheral has been needed that is also smaller in size and lower in price. The HP 9144A, Fig. 1, meets both of these needs. This peripheral can be used with HP disc drives from 5 to 132 Mbytes. It is supported on the HP 3000 family of computers, the HP 1000 A-Series, the HP 9000 Series 200 and 500 Systems, and the HP 150 Personal Computer. It is also available in one box with a Winchester disc drive as the HP 7946A, which also gives one-button full disc image store and restore. The HP 9144A can therefore meet the needs of a wide range of computer users.

The HP 9144A stores data on removable cartridges that contain ¼-inch-wide magnetic recording tape. The cartridges come in two different capacities. The lower-capacity cartridge has 150 feet of tape with a data capacity of 16.7 Mbytes, and the higher-capacity cartridge has 600 feet of tape with a data capacity of 67 Mbytes. The HP 9144A has read after write capability, so that data can be rewritten automatically if there is an error during the write process. There is no time penalty for this read checking. It also has error correction capability, so that entire 256-byte frames can be replaced. The cartridges can be interchanged with the tape drive used in the HP 7908, 7911, 7912, and 7914 Tape/Disc Drives.

Although Winchester disc backup is its primary use, the HP 9144A also meets several other needs, such as data interchange and software distribution. High data interchange reliability from one HP 9144A to another was an important design criterion. This allows data exchange from one system to another. Software distribution can be a problem when the software takes many flexible discs, but with an HP 9144A, it can all be sent out on a single tape cartridge.

With the HP 9144A, the user can back up a 60-Mbyte disc in as little as 30 minutes. A 12K-byte buffer in the drive and optimized system software minimize waiting for data transfers and commands from the host. Operating in streaming mode, the drive provides up to 2-Mbyte/minute backup performance, depending on host software.

To protect the user's data and minimize drive failures, an electromechanical servo control feature is built into the tape drive. This increases both tape and drive motor life by providing gentle acceleration and deceleration as the drive stops and starts.

Internal diagnostics provide quick isolation of failure and ease of repair. This means that the user will experience minimum downtime and lower maintenance costs. A light on the front panel warns if the drive is inoperative and rear-panel diagnostics indicate which replaceable unit has failed.

The HP 9144A fills the same space on a desk as an in-basket. It can also be packaged in a pod configuration or mounted in a standard 19-inch rack.

Disc-Like Format

User data stored on the HP 9144A's cartridge is formatted into blocks that contain 1024 bytes each. Each block contains a header that tells how many bytes are stored in that block, so that partial data blocks can be stored easily. The format allows any block to be accessed separately for reading or writing. Therefore, the tape can be written to and read from just like a disc. This is a distinct advantage because all the operating system commands that can be used on discs can also be used on the tape. The tape can have a directory just like the disc. Files can be stored onto the tape and then retrieved through the directory just as if they were on a disc. Files can be deleted and new ones added anywhere there is free space according to the directory. Alternatively, a file mark command exists so that the drive

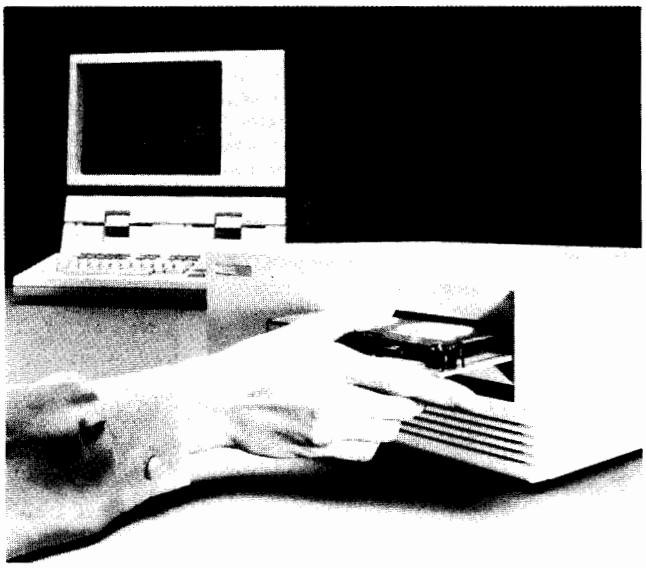


Fig. 1. *The HP 9144A ¼-Inch Cartridge Tape Drive offers convenient, low-cost backup of 67 megabytes on a single cartridge. Read after write capability and exclusive-OR error correction provide improved data reliability.*

can be used like ½-inch tape drives, where different files are found by searching for the appropriate tape mark. Different computer operating utilities will use the cartridge tape in one of these two modes depending on whether the utilities were originally written to work with discs or ½-inch tapes.

There are 16 tracks on the removable cartridge. The drive can write or read one track at a time. These tracks are written in serpentine fashion with the even tracks going from left to right and the odd tracks going from right to left. At the end of one track the head is just moved up to the next track and the motor starts moving the tape in the opposite direction.

The combination of serpentine format and read after write capability requires the magnetic head to have two pairs of gaps. One pair has the read gap on the left side of the write gap so that read after write can be done when the tape is moving from right to left. The other pair has the read gap on the right side of the write gap so that read after write can be done when the tape is moving from left to right.

Data Integrity

Providing superior data integrity was a primary goal for the HP 9144A. Achieving a low error rate on a cartridge tape product requires more fault tolerant design than hard or flexible magnetic media products. Tape, when moving, continuously changes shape as it conforms to the hubs, guides, and head. This can create a higher level of internally generated contamination. A robust design is required to tolerate both particle contamination and other causes of errors such as defects in the tape and externally generated contaminants.

The write and read processes are the two important areas of concern in providing a high level of data integrity. The HP 9144's write process provides assurance that data is written on the tape correctly and the read process incorporates extensive features to ensure data recovery.

Five levels of data protection are implemented in the HP 9144A (see article, page 39). Starting with the media, only certified data cartridges are specified for use on the HP 9144A. Defects that exist on the tape are bypassed by use of a sparing table, which is generated when the tape is certified. A defective portion of the tape will not be used; that block will be replaced by one of a group of extra blocks which have been reserved as spare blocks.

The next step to ensure that data is written correctly is the read after write process. The HP 9144A uses a four-gap wide-write, narrow-read magnetic head. All data written on the magnetic tape is read immediately after the recording process.

Data retrieval is the next level of protection; highly optimized data separation and read algorithms are incorporated in the HP 9144A.

Error detection and error correction provide another level of protection. A CRC (cyclic redundancy check) error detection process is used on every frame and key. Also, 50% data redundancy is recorded to provide error correction. A block of 1024 bytes is completely recoverable if as much as any two adjacent 256-byte frames are completely destroyed.

The last level of protection is media monitoring. The media are monitored by recording the number of passes in the user's log on the tape. After a cartridge has exceeded a maximum number of either insertions or passes, the write-protect light located on the front panel flashes, warning the user to back up the data on that cartridge.

These protection levels provide a very high confidence of correct data recovery.

Reliability

A significant improvement in reliability was a major goal for the HP 9144A. The specific objective established to meet this goal was to improve the reliability by a factor of two over existing comparable products. This would be measured by both in-house and field failure rates.

The approach used to reach this goal was to take specific actions in design, testing, and manufacturing. The steps taken in the design were derating of components, using a higher level of circuit integration, and maintaining a low temperature rise within the enclosure. For example, all components are derated to less than 70% of their specified maximum power. A fan is used to limit the internal temperature rise to less than 5°C. The controller uses two custom VLSI chips and two gate arrays to minimize the component count (see article, page 37).

An extensive test program was implemented, including environmental, error rate, compatibility, and strife testing on 70 units. Strife (stress and life) testing was designed to test beyond specifications to find out what would fail, understand why, and implement improvements.

Process control was implemented in production. Control charts are used to monitor critical parameters such as head alignment. Production audit tests are used to verify error rate performance. Compatibility and strife testing are used as tools for continuously improving the quality of the product.

The results are very encouraging. Based upon the latest environmental and strife testing, strife yields have increased significantly. Building the HP 9144A in production has been extremely smooth, which is indicative of both a solid design and a solid production process.

Acknowledgments

It is difficult to thank all who contributed to this major project. Special thanks to the unnamed people throughout the division from manufacturing, quality assurance, marketing, and finance. Thanks go to lab management for their guidance on this project. Rex James and Rick Spangler as lab managers provided long-term support. Frank Carau and Don Stavely as section managers provided both product and technical support. As project managers, we express our thanks to the engineers who really made the HP 9144A possible. The electrical design team consisted of Doug Gennetten, Larry Paille, Joe Eccher, Tom Oliver, Craig Miller, and Lynn Watson. Walt Auyer, Dave Schmeling, Keith Walden, Dan Dauner, Chuck McConica, and Mark Wanger were members of the mechanical design team. The software team included Gordon Nuttall, Mark Gembarowski, Steve Henry, Frances Cowan, Bob Kaphammer, Perry Wells, and Ken Nielsen. Gene Briles, Mike Niquette, and Peter Way were members of the system integration team. The transfer team members were Kevin Bier, Leo Embry, Lonnie Ford, and Terry Tuttle.

A Design Methodology for Today's Customers

The HP 9144A Tape Drive was designed by Hewlett-Packard engineers to achieve a high level of customer satisfaction. To do this it was necessary to go beyond the standard approach of designing a drive and controller to meet specifications. The marketplace challenged us to go beyond the specifications to provide ample margins to accommodate real-world variances and to provide consistent quality and HP reliability.

Why was such an approach necessary? Let's look at an example. The DC600 Tape Cartridge is a high-technology product providing over 100 megabytes of unformatted storage capacity in a very convenient and low-cost package. Tape of comparable quality, such as ½-in tape, is used mostly in environmentally controlled computer rooms and is typically handled by technicians familiar with high-density computer tape. On the other hand, the ¼-in tape cartridge reaches first-time computer users in a wide range of environments and applications and is most often treated like an audio cassette. Yet, these customers need high capacity and reliability and demand ease of use. To meet these requirements, the media and drive system of the HP 9144A had to achieve four times the track density of state-of-the-art ½-in GCR (group code recording) tape drives.

Clearly, we had to use an innovative design approach and invent the product from the ground up with the customer in mind. We had to design the mechanism, hardware, and software by forming interdisciplinary teams that were highly focused on a problem area and whose goals were to provide reliability and high performance with simple, elegant, and low-cost designs. These teams felt a high level of ownership of a design area and were able to design margin into the product to account for real-world variances and to identify all the key variables that would affect the long-term performance of the system.

In harsh environments, for example, the cartridge sometimes exhibits a sudden burst of high-frequency speed variation that typically causes tape drives considerable problems with data integrity. Our design philosophy challenged us to develop a third-order phase-locked loop that can track this high-frequency variation in tape speed. We integrated the loop with the firmware of our formatter to provide our customers with smooth streaming performance and data integrity.

Another reality of our marketplace is that customers want this streaming tape drive performance in spite of the fact that often the data is gathered and transferred to the tape drive in sequences of short bursts. These short data transfers can wear out the cartridge, cause high stresses on the drive motor, and typically result in poor throughput. To solve this problem, we chose a drive motor with a superior brush design, then surrounded it with a control system that very gently accelerates the tape, and finally, provided software enhancements to help the host system achieve full streaming mode performance even for short data transfers.

Our team approach was especially fruitful in combining software with mechanical design. We use software algorithms to compensate for hysteresis in the head stepping mechanism and even to adjust the placement of data tracks to accommodate thermal bending of the cartridge baseplate.

We also took this methodology outside of HP to our key vendors, who became part of our team, designing margin into their components. In the area of the read/write head we worked together closely and produced a design that is totally insensitive to ±25% off-track alignment. We surrounded this with a mechanism design that minimizes tape wander in the cartridge and a read channel preamp that eases the design constraints on the head and yet achieves full compatibility with HP's current cartridge product line.

Now that we had a product that was designed from the customer's point of view, with margin to accommodate real-world variances, we challenged our team to submit it to a comprehensive test program that was planned to guarantee the quality, reliability, and consistency of every unit we produce. Each designer was responsible for creating a stand-alone test system that would verify the functional performance and margin of the design. Software, mechanism, and electronics designers teamed up to develop functional tests that prove the consistency of the design and demonstrate that all the key variables that affect performance have been identified and brought under statistical control in the *design* phase of the project. These functional tests are now in production; all assemblies receive complete functional tests after automatic component verification. As a result, the current HP 9144A error rate is so solid that we have statistically proven over an order of magnitude of margin on production units over the complete range of environments. All key variables are charted to be in control on a regular basis in production.

Acknowledgments

Such a design approach required the active participation of everyone on the project. Sterling Mortensen architected and managed our programs of structured software design, software QA, and team building. John Becker, who contributed to the testing effort that helped HP to win the Deming Award, designed a program of strife and environmental testing that, under his guidance, was highly effective in identifying system problems and eliminating potential hardware problems.

The final principle of our design methodology is to provide for continuous product improvement. Thus we have put into motion a program of LSI for the controller and cost reductions for the head and drive electronics. John managed a coordinated program between the lab and manufacturing that has resulted in a reduction of controller electronics from three boards to one. These improvements provide equivalent or higher performance and are fully interchangeable.

Donald A. DiTommaso
Project Manager
Greeley Division

Tape/Disc Controller Serves Integrated Peripherals

by Craig L. Miller and Mark L. Gembarowski

THE DESIGN GOAL for the controller of the HP 9144A Tape Drive was to provide a structure permitting one or two mass storage peripherals to operate cohesively for on-line and backup functions. The product's architecture design was a joint venture with HP's Disc Memory Division to provide a common controller for integrated disc and tape peripherals.

The HP 9144A controller provides high performance and flexibility. The controller architecture allows either a fixed disc, a ¼-inch tape, or both to operate in a common environment. A related, combined disc/tape product, the HP 7946A, provides not only read and write capabilities to and from the host but also local data transfers from disc to tape or tape to disc.

The controller functions are segmented into two areas. The functions common to basic mass storage controllers are lumped together onto one controller called the host dependent controller (HDC). Functions that are specific to the tape or disc drive are contained on a device dependent controller (DDC). One HDC can support one or two DDCs (see Fig. 1).

HDC Characteristics

The HDC interfaces between the host computer and the DDC, which provides low-level control of the mass storage mechanism. The HDC provides high-level functions, including:

- Providing the host interface (HP-IB/IEEE 488) and handling the associated protocol
- Operating a microprocessor (6809) for basic control and status reporting
- Providing buffer RAM, enabling data to be read from the device and verified or corrected before being transferred to the host
- DMA capability.

Fig. 2 is a block diagram of the HDC.

The DMA controller is separated into two independent channels, input and output. Each channel has a FIFO buffer which is four locations deep. Addresses for transfers are programmed into the FIFO buffer. Each FIFO buffer location is independent. Each channel can be monitored and new addresses can be programmed into the FIFO buffer during a transfer to allow high performance and uninterrupted transfers. Each channel can support 1-Mbyte/s concurrent transfers.

For example, suppose the host computer wants to perform a selective file backup of the fixed disc onto the ¼-inch tape. The host computer sends commands to the device specifying a file to be transferred from the disc to the tape unit. While that file is being copied locally from the disc to tape, the host can send another command to copy a different file from the disc to tape. Continuing this sequence allows a user to back up the disc drive selectively. The fixed disc could possibly keep the tape streaming in this selective file backup since the buffer RAM (approximately 11K bytes) on the HDC provides data speed matching (see "Making a Start/Stop Tape Stream," later in this article). The tape drive transfers 1K bytes of data every 30 ms, allowing the fixed disc sufficient time to perform most seeks and to read additional data.

If the host computer initiates a backup operation from the disc to tape, the host is free to use the HP-IB for other transactions during the backup operation, since the backup is local to the peripheral. An HP-IB parallel poll will indicate when the backup is complete.

The HDC runs a small operating system serving three users: the host interface firmware, the firmware to control the tape, and the firmware to control the fixed disc in a dual-peripheral configuration. The 6809 microprocessor is time multiplexed between the users. Approximately 30% of every millisecond is devoted to each user, and there is a total of 10% overhead in switching between users.

The interface between the HDC and the DDCs has a fixed definition to provide for independent software and hardware designs. There are two buses with associated strobes or handshake lines. One bus is the command and

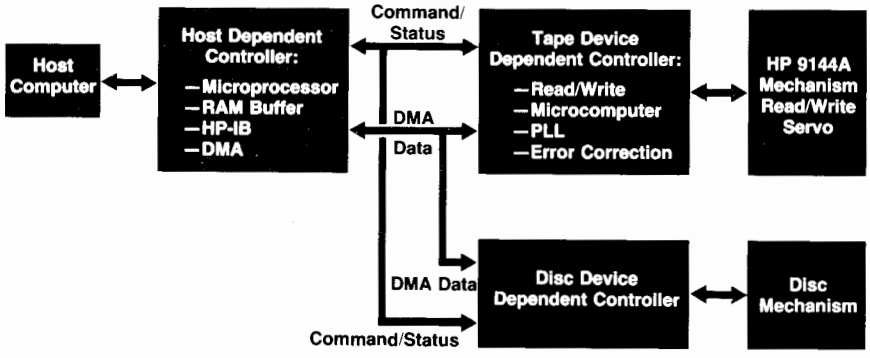


Fig. 1. *The controller for the HP 9144A Tape Drive can interface one or two mass storage peripherals (tape or disc) to a host computer. The controller functions are partitioned into a host dependent controller and one or two device dependent controllers.*

status bus for commands from the HDC to the DDC and DDC status monitoring by the HDC. The other bus is a DMA data bus for data transferred to and from the tape or disc. The separation of these two functions allows monitoring of status and issuing of commands to the tape or disc during data transfers.

DDC Characteristics

Functions that are specific to the tape drive are contained on a device dependent controller (DDC). These functions are reading and decoding data, writing and encoding data, checking and correcting errors, and basic device-specific control.

The DDC for the ¼-inch tape interprets the specific requirements for the tape. There are two basic processes on the DDC: the write process and the read and data recovery process. A 6805 microcomputer oversees these two processes.

The write process, under control of the microcomputer, requests data from the HDC. The data is serialized and the appropriate identification, error detection, error correction, and formatting data are appended to the user data.

The read and data recovery process locks onto the serial data stream and decodes the format to identify the tape position. The read algorithms are tightly coupled to the data recovery circuit for controlling the data separator for optimal performance. The read process also strips away the overhead information and provides the user data to the HDC for later transmission to the host. Error correction is performed in real time by exclusive-OR hardware (see article, page 39).

The microcomputer controls both the read and the write processes. It also communicates with the HDC for commands and status. Physical tape positioning for seek, read, and write operations is controlled by the microcomputer.

The beginning and end of the tape are sensed electronically by the read process algorithms. The beginning-of-tape and end-of-tape positions are written in a special format found nowhere else on the tape. The read algorithms sense these conditions and inform the servo controller to stop the tape motion. For fail-safe protection, the servo automatically stops the tape if the signal is lost. This prevents unspooling of the tape. Previous tape products used LED sensors to sense the beginning and end of the tape. These proved to be less reliable as the product became older or was subjected to heavy use.

The read algorithms associated with the data recovery circuit are very fault tolerant, enabling the read process to recover from many abnormal situations.

Four custom LSI circuits were developed for the HDC and the DDC. The first two are CMOS gate arrays, one having 2000 gates and integrating the DMA controller, real-time clock, and programmable time interrupt on the HDC, and the other having 440 gates and integrating the high-speed precompensation circuit, DMA handshaking, VCO control, and data recovery circuit for the DDC. These two integrations required the development and enhancement of a set of tools initiated by HP's Roseville Division. These tools and thorough simulation allowed the two gate arrays to work exactly as defined the first time.

The tools are based on HP's Testaid-IC logic simulator program. Timing and fault analysis can be performed using this program. The gate array specifications were added to the Testaid-IC library on the HP 1000 Computer System. The timing, loading, and functional descriptions of the library parts were loaded into a data base. Drawings of each library part were created and the design and connectivity were entered using HPDraw on the HP 3000. The drawing file was transferred to the HP 1000, where timing was added to the drawing data base. Functional, performance, and fault analysis were performed on the HP 1000 using Testaid-IC. The files were converted to the gate array format and transferred to the gate array vendor. The tools and analysis were comprehensive enough to provide full functional performance on the first design pass.

The other two LSI circuits are NMOS semicustom state

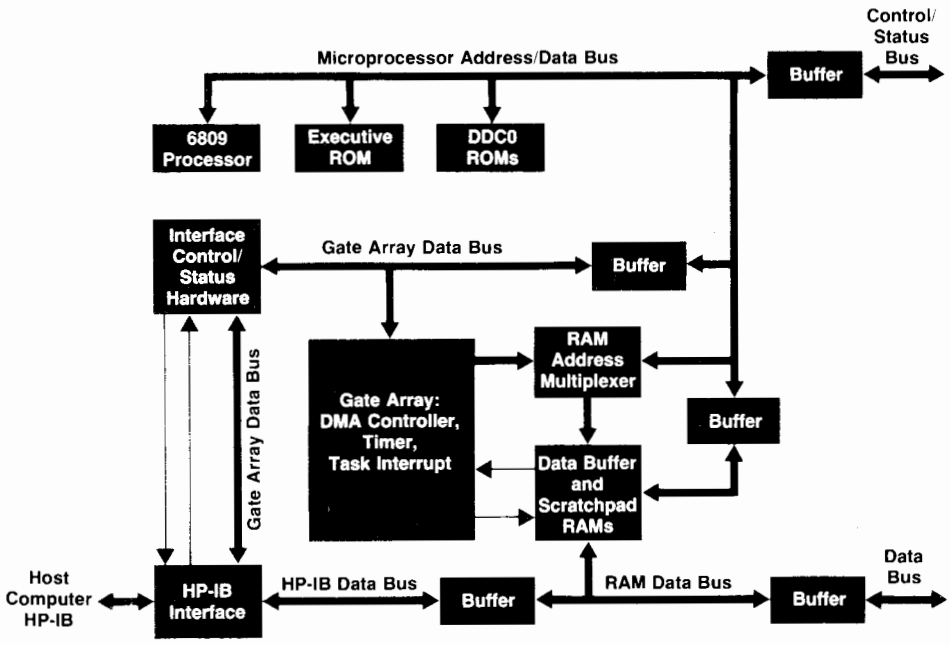


Fig. 2. *Host dependent controller block diagram.*

machines. Advanced tools developed by HP's Greeley Division for a universal state machine (a semicustom part) enabled fast and efficient integration of the read and write state machine algorithms that encode and decode the HP 9144A data format. These state machines also control the read and write functions.

The error rate was improved significantly by integrating the data recovery circuits in a gate array. The integration allows tight control of timing and closely matched delays in portions of the circuit.

Making a Start/Stop Tape Stream

One of the key performance improvements of the HP 9144A over the tape drives in the HP 7908, 7912, and 7914 is the addition of streaming mode. Streaming is a mode of operation in which the tape continues to write or read data without repositioning. The HP 7908/12/14 Tape Drives would stream only for the short amount of time that the host computer could buffer data. On the single-controller versions of these products, the tape would stream only for an image copy of the disc.

The HP 9144A has a significant performance advantage over its predecessors because streaming is not dependent on host buffer size, and streaming can be maintained even on selective file store and restore operations. The HP 9144A saves over one second per host transfer because it has streaming built-in.

How is this improvement realized? In normal start/stop operation, the drives (HP 9144A and HP 7908/12/14) reposition the tape upon completion of the execution phase of the transfer. (In execution phase, the data is sent to or from the host). Once the repositioning is completed, a report is sent to the host. Repositioning moves the tape back far enough so that if the host sends a command to read or write the next sequential block on the tape, the drive can accelerate and read or write the target block at the proper speed of 60 inches per second.

We make the tape drive stream rather than operate in start/stop mode by eliminating the repositioning at the completion of reading or writing the data. The stream mode of writing is called "immediate reporting." This name evolved from the fact that the report byte is sent to the host computer immediately after the last byte of data has been transferred to the tape drive controller's RAM buffer, rather than after it is all written to the tape (start/stop mode). The host, because it has seen the report byte, can queue another write command to the tape drive (provided it is for a sequential address) and the tape drive will stream as long as the command is sent before the RAM buffer is empty. The only change that is necessary in the host driver is the addition of the set option command to enable the immediate reporting mode.

Streaming while reading data for the host presents a different problem. The tape drive is the source of execution data for the host. Normally, the controller repositions the tape as soon as all the data has been sent to the host, and then sends the report byte. In the streaming mode, which is called "read ahead," the report byte is sent to the host as soon as the data transfer is complete, and the drive continues to read data, buffering it in the RAM on the tape drive controller. If the host sends another read command to the tape drive for the next sequential address, the tape drive will not have to reposition to get data it already has in RAM, and hence it will stream. This streaming will continue as long as another sequential read command is sent before the RAM buffer is filled with read ahead data. Read ahead mode is enabled with exactly the same set options command and parameter byte that are used to enable immediate reporting.

Cartridge Tape Data Integrity Ensured at Five Levels

by K. Douglas Gennetten

THE NEW HP 9144A ¼-INCH CARTRIDGE Tape Drive provides a convenient, low-cost, high-reliability alternative to flexible discs and ½-inch tapes for backing up valuable data. The remarkable data reliability of the HP 9144A is ensured by the melding of several important data protection techniques. Extensive testing has proved that the typical HP 9144A's data error rate is more than ten times better than the specified rate of less than 1 error in 10^{10} bits. This performance is achieved through careful attention to design margin in many areas of the product.

Read After Write

The HP 9144A provides the first level of data integrity through precise flux-change placement on the media followed by immediate verification of written data.

Encoded data is first preconditioned to compensate for peak shift or spreading, which occurs when two flux changes are placed in close proximity. Each data edge is phase shifted by an amount determined by the surrounding data pattern. Two flux changes placed close together will tend to repel and shift apart in opposite directions. Precompensation of these two edges improves this condition by

writing the edges closer than nominal by a controlled amount. Upon relaxation, the edges return to their proper positions. The write circuit precisely records the flux changes into the media, removing any previous data.

The final written position of these flux changes is tightly controlled to ensure adequate performance margin in the data retrieval process. The read circuits are carefully designed to introduce no significant phase shift onto the read data. This is done using high-order phase-linear filters.

The read after write capability enables the drive to detect and automatically correct or spare out errors caused by media defects or foreign particles. This powerful advantage, typically found only in larger, more expensive tape storage systems, guarantees that the recorded data is initially defect-free.

Certified Cartridge

The second level of data integrity is provided by the HP DC600 High-Density Data Cartridge. This cartridge contains magnetic media formulated from high-coercivity materials which are applied using a special process to reduce error-producing dropouts. These characteristics permit reliable, high-density, minimal-defect recording.

Cartridges used on the HP 9144A are preformatted and certified at the factory. This provides additional protection and allows immediate use of new cartridges. No time-consuming certification or formatting is required.

The HP 9144A Tape Drive uses a block-oriented format written over 16 tracks in a serpentine block-serial fashion. For example, all the blocks on track 0 are written in the forward direction first; then the head steps to track 1 where all the blocks are written in the reverse direction. This formatting method allows random access as well as streaming operation. The drive uses preformatted tapes with storage capacities of 16 megabytes (150 ft) and 67 megabytes (600 ft). Fig. 1 shows the tape format.

Each 1024-byte block is written between interblock preformatted keys placed vertically across the entire width of the tape. The blocks contain six 256-byte frames: four for user data and two for error correction. Even tracks are written from the beginning of the tape (BOT) to the end of the tape (EOT). Odd tracks are written from EOT to BOT.

Keys contain the physical block number, which is also reproduced in each frame header along with other information describing the block. All frames and keys end with a 16-bit cyclic redundancy check (CRC) character, which provides very reliable error detection, and a postamble.

The tape format contains special prerecorded BOT and EOT patterns which allow solid-state beginning-of-tape and end-of-tape detection without the use of conventional optical sensors, which are more costly and less reliable.

Data Separation and Clock Recovery

The third level of data integrity assurance takes the form of accurate data retrieval. Phase-linear signal filtering followed by optimized data separation provides data recovery margin well above that found in other high-performance tape systems. Rigorous design and optimization methods (described below) have provided the HP 9144A with enhanced read margin over a wide spectrum of cartridge conditions. The data retrieval process is exceptionally tolerant to large levels of phase error caused by peak shift and noise as well as extremely rapid and large speed variations, both being common conditions in high-density, belt-driven cartridge tapes.

The user data to be recorded on the magnetic tape is first intermeshed with a clock in a form of modified frequency modulation (MFM) encoding. MFM data encoding, when combined with optimized, low-noise data recovery, enables higher bit densities and improved speed tracking compared with other commonly used tape codes. MFM also has the advantage of being very easy to implement. For each 1 a flux transition is written at the center of the bit cell and for each 00 pair a flux transition is written between the bit cells (see Fig. 2). Before being recorded onto the tape, each encoded transition is first precompensated (phase shifted) to counter the expected peak shift that occurs when flux reversals are placed side by side at high densities.

Data retrieval requires reliable separation of the MFM-en-

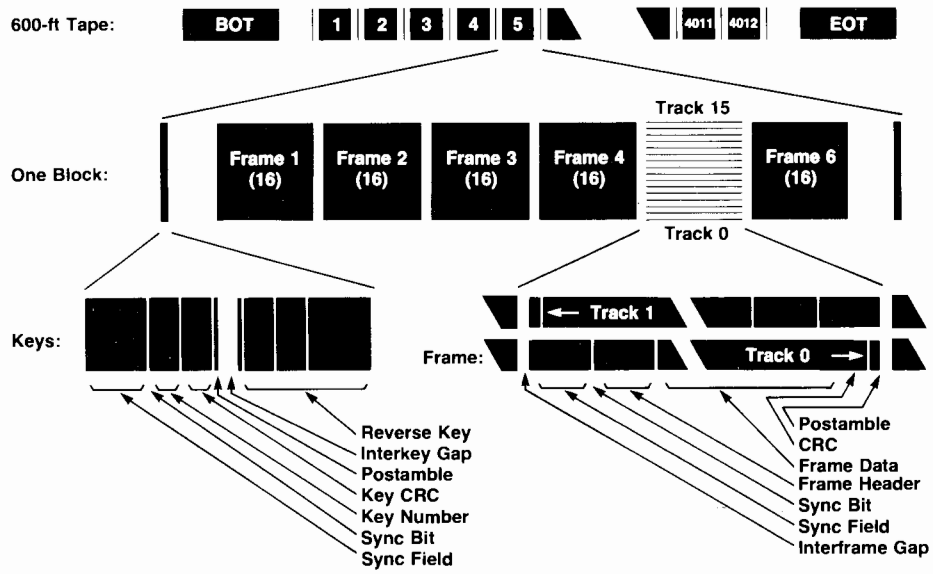


Fig. 1. *DC600 tape format. All blocks on track 0 are written in the forward direction first. Then the head steps to track 1 and writes data in the reverse direction, and so on.*

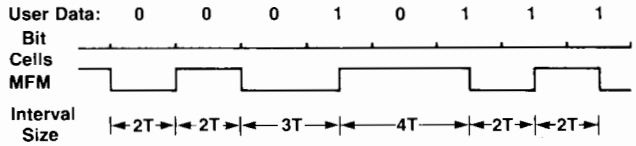


Fig. 2. *MFM encoding example.*

coded data and clock. This objective presents unusually difficult challenges when the data is stored on cartridge tape at very high flux densities. The encoded data read back from the tape is degraded by two major sources of distortion: tape speed variation and phase shifted data.

Tape speed variation in the DC600 cartridge is dominated by several large components at 30 Hz, 100 Hz, and 6000 Hz (using 60 inches per second tape speed), which are beyond the control bandwidth of the capstan servo system and, in fact, are not seen by the capstan servo encoder. Of these, the 6-kHz component is the most severe. When all three components are overlapped, they can add up to speed variations of over 15% of the normal read/write speed. Speed variations evoke frequency modulation of the data signal, which requires accurate demodulation during data separation.

Phase shift is caused by several sources. The most pronounced include imperfectly compensated peak shift, phase nonlinearity of the read head, and electrical noise. Phase shift evokes phase modulation of the data signal, which must be filtered during data separation. The HP 9144A read amplifier and filter electronics have a high degree of phase linearity and do not significantly add to the total phase shift.

The tracking of speed variations and the filtering of phase shifted data are done in the data separator by a phase-and-frequency-sensitive closed-loop servo system termed the phase-controlled loop, or PCL (Fig. 3). Higher and faster speed variations require quicker response by the PCL while higher phase shift magnitudes are best handled by a slower response. The resulting conflict requires a careful compromise and is handled particularly well by the PCL, which is an optimized third-order system (second-order systems are most common). The higher-order loop, when accurately optimized, is better able to make such compromises by minimizing the average and instantaneous real-time error (RTE), thus providing the necessary margin for reliable data recovery during the extreme circumstances commonly found in inexpensive tape cartridges.

Data Separator

The HP 9144A data separator (Fig. 3) is composed of the phase-controlled loop,* an MFM decoder, gap and lock detectors, and a synchronous state machine. The state machine monitors gap, lock, and data status of the separator and controls the PCL modes.

Frequency-lock mode. This mode is invoked during sync field frequency acquisition, which occurs at the beginning of every data area, and during gaps, when the loop is frequency-locked to a crystal-based clock. The frequency-lock mode inserts a frequency divider (÷2) in the PCL feedback path. This divider causes the VCO to acquire lock at twice the incoming data rate; this is necessary for providing the two-windows-per-bit needed for MFM. The frequency-lock mode also disables the pulse gate function of the phase/frequency detector, thus allowing the frequency of VAR (VCO/2) edges to be compared with the frequency of the REF (incoming data) edges.

Phase-control mode. This mode is used during all data tracking and decoding. It is invoked after the frequency-lock mode has achieved a stable locked condition in the loop, but before the data actually begins. The phase-control mode disables the VCO/2 divider, making all VCO edges available to the phase/frequency detector for phase comparison. The pulse gate function is enabled, blocking all extra VCO edges and removing the loop's frequency-discrimination capability. The phase detector attempts to match each REF edge with one and only one VAR edge. From one to three extra VAR edges occur between each REF edge. The phase/frequency detector matches each REF edge with the one VAR edge that is within one half window before or after the REF edge. Once a valid match is made, the phase/frequency detector sends a pulse to the loop filter

*The more common term "phase-locked loop" is avoided here because the PCL is never actually phase-locked as in a frequency synthesizer or FM receiver; it is frequency-locked but exhibits large, rapidly changing phase error.

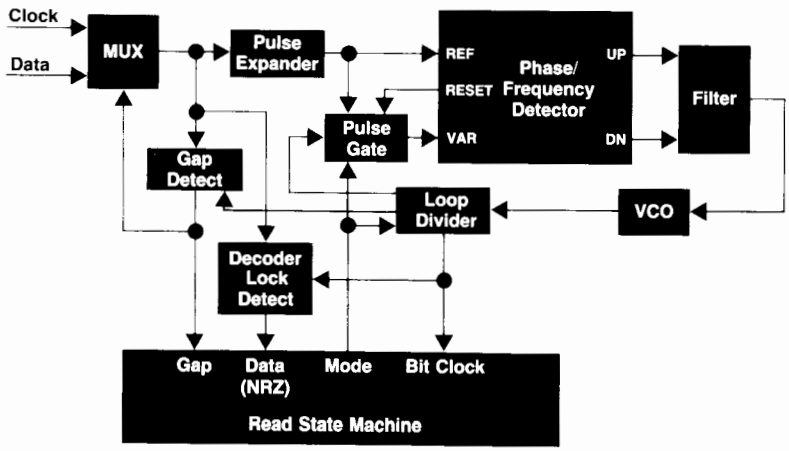


Fig. 3. *Data separator block diagram.*

that is proportional to the phase error and of the appropriate sign. The loop filter then processes this signal and sends the filtered response to the VCO, which begins to nullify the detected phase error.

The lock detector is nothing more than the data decoder combined with a lock-detect algorithm in the state machine. When locked and in a sync field, the data decoder will have a stable output. Any cycle slip or other lock failure will show up as an unstable decoder output and is easily recognized.

The gap detector is a resettable counter that increments one count for each VCO clock and is reset by each data edge. When the count is at or above five, the circuit alerts the state machine that a gap or dropout has been detected. With the format used, it is important that gap detection be rapid and reliable. This circuit meets that need by using a tracking time base rather than an external crystal or one-shot timer. A gap is detected based on the count of bit times, rather than a fixed time period.

Propagation delays in a design such as this can easily accumulate and produce asymmetry in the form of large steady-state phase error (i.e., reduced RTE margin). This design incorporates delay equalization, which balances the data path from the data source to the phase/frequency detector with the data path from the source to the MFM decoder. The result is improved operating margin and enhanced data integrity.

PCL Optimization

Optimization of the PCL's tracking dynamics is of paramount importance. Two common optimization procedures for data recovery systems are 1) trial and error adjustment of the loop filter parameters while observing the error rate performance and tracking ability under typical data conditions, and 2) reduced-window accelerated testing in combination with the first procedure. Reduced-window testing artificially reduces the RTE margin by an adjustable amount during tracking of normal data. Another common testing method is subjecting the system to artificially generated data patterns from a pattern generator modulated by a variable-frequency source. This last method is of little value, since it simulates speed variation without any superimposed phase modulation. Under such conditions a loop will perform much better than in actual use where pattern-dependent peak shift and random noise induce phase modulation of the data, which greatly reduces the frequency demodulation (speed tracking) ability of the system. These optimization procedures do not provide best-compromise performance, which is necessary for ensuring the best overall error rate. These inadequate methods all incorrectly assume a direct link between available tracking and decoding window margin (RTE margin) and error rate. A system optimized to provide the best compromise provides the best possible performance without going to a higher-order response. It can therefore be termed a best-fit optimized system. The HP 9144A PCL is this type of system.

A best-fit optimized PCL will provide an absolute minimum error rate when subjected to the entire range of expected conditions. This loop, however, will not exhibit the maximum possible average RTE margin and will not have the maximum possible instantaneous RTE margin during most typical conditions. This is not undesirable; although the margin is reduced during noncritical conditions, it is still reliably maintained well above necessary levels. The reserve capability needed for worst-case conditions (relatively infrequent surges in speed and/or phase shift) causes minor overshoot during less strenuous typical conditions, resulting in reduced average and instantaneous RTE margin. Higher-order loops are more effective in allowing such trade-offs, resulting in improved error rates. A loop optimized to typical conditions using one of the common procedures noted above will not perform as well in any data recovery environment (especially cartridge tape drives) exposed to transient noise sources, head and media imperfections, and speed variations.

Best-fit PCL optimization requires an accurate evaluation of the data modulation during readback. The most critical element of this process is the careful capture and analysis of transient worst-case conditions during all operating environments. This information is used in the first phase of the optimization by applying theoretical analysis and de-

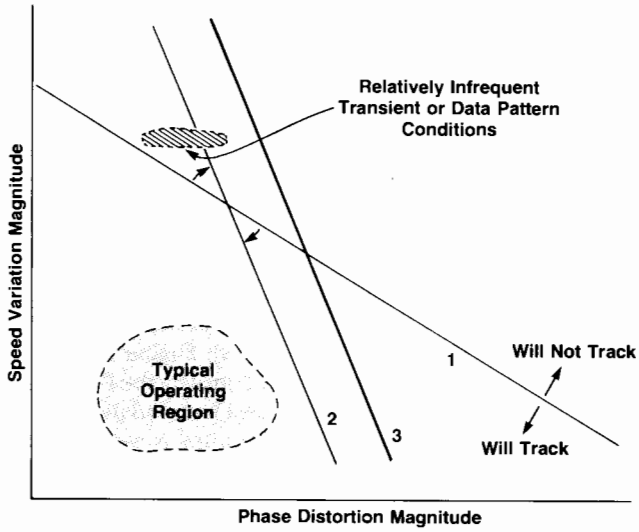


Fig. 4. *This diagram illustrates the three possible phase-controlled loop (PCL) operating points. The two sources of data modulation are phase modulation (abscissa), and frequency modulation (ordinate). Increased levels of phase modulation (noise and peak shift) reduce the amount of tolerable frequency modulation (speed variation). This is shown by the PCL operation-limits line. Any modulation falling to the right of the line or above it causes tracking failure. Line 1 represents a typical set point: relatively large margin (distance from modulation area to limits line) exists for typical operating conditions, and failure occurs during transient conditions of large speed variation. In general, increasing the PCL's bandwidth will rotate the line clockwise (line 2). This increases the margin available for transients (but not enough in this case) while reducing the rnargin for typical conditions. By using a third-order loop (rather than second) and optimizing both bandwidth and phase margin (damping) one can achieve limits-line translation with little or no rotation, thereby improving overall margin (line 3). The margin provided for typical modulation is set larger than that provided for rare events of large modulation. This is essentially a "proration" of margin, which provides the best overall error rate.*

sign techniques to arrive at important parameter values such as bandwidth and stability factors (see Fig. 4). These transient conditions are then simulated by using a special signal source which overlays controlled phase and frequency modulation onto a predetermined data pattern. These simulated conditions are used in the second phase of optimization by observing the instantaneous RTE margin during minor parameter adjustments.

During the HP 9144A development, a PCL test system was designed to aid the best-fit optimization process. This test system provides two separate functions: 1) modulated data simulation—combining variable data patterns with controlled simultaneous frequency and phase modulation—and 2) data capture and analysis—high-resolution data gathering and automated analysis of tracking performance and RTE margin. The modulated data generator allows simulated phase modulation from random noise (asynchronous) and from pattern-dependent peak shift (synchronous) to be superimposed onto frequency modulation, thereby providing a realistic, controllable, comprehensive test data source.

Other noteworthy contributions to data integrity are included in the HP 9144A's data separation functions. No adjustments of the circuitry are possible or necessary during the production process and low-tolerance components can be used. Both factors contribute to the low cost and ease of manufacture of the product. All of the timing-critical signal paths are carefully balanced and integrated into a single LSI chip designed for the HP 9144A, providing significantly improved margin and reliability and lower cost.

The phase/frequency detector designed into the HP 9144A's PCL is an improved design that eliminates synchronization boundary problems commonly found in classical sequential phase detectors. When switching from one signal (clock) to the other (data), the phase of the new data source is unknown and can often cause a glitch in the phase synchronization process, which may cause a transient error condition. To avoid this, the asynchronous state machine was carefully analyzed to identify and resolve any possible state transitions that could cause race conditions or hung states.

Error Correction

While the DC600 cartridge is capable of storing data without significant degradation for several years, data loss caused by dust particles, stray magnetic fields, and extremely long storage intervals is possible. The HP 9144A protects the user from such losses through the fourth level of data integrity assurance: post-retrieval error correction. Large portions of the recorded data—up to 512 contiguous bytes—can be destroyed without inducing an unrecoverable data error. This feat is made possible by the use of redundant data embedded within the user's data. The prevailing cause of transient errors in a cartridge tape drive is foreign particles, which lift the tape off the head surface, causing loss of a large number of contiguous bits. The HP 9144A's exclusive-OR error correction is especially suited to correcting such errors.

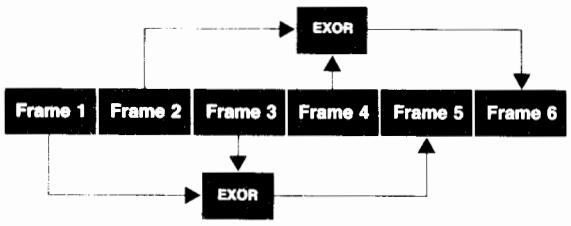


Fig. 5. *Exclusive-OR frame generation during data recording.*

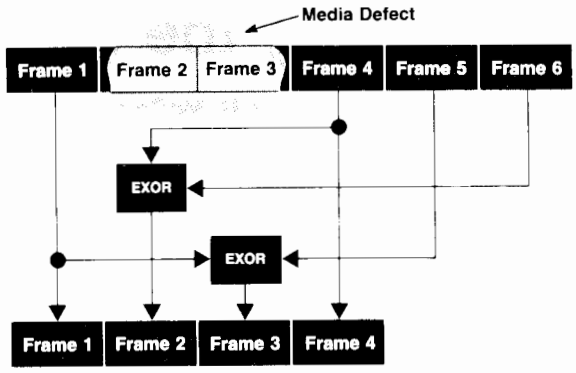


Fig. 6. *Exclusive-OR error correction of defective media. Data can be recovered when up to two complete adjacent frames are in error. Correction is done on the fly; there is no need to reposition the tape and retry. Retry algorithms are used only as a last attempt to recover data.*

Error correction also serves to extend motor and cartridge reliability by minimizing the need for tape repositioning. Without error correction, each error-causing dust particle or media defect would initiate a reposition and retry operation over the data area, reducing motor and cartridge life. Starts and stops (two are required for each repositioning) are the primary cause of motor wear.

User data is written onto the tape in the form of 1024-byte blocks. Each block is segmented into six 256-byte frames. The first four frames contain the user data while the last two frames contain redundant data (see Fig. 5). The redundant frames are generated concurrently with the write process by executing a bit-serial exclusive-OR operation on the previous frames: frame 5 is frame 1 combined with frame 3, and frame 6 is frame 2 combined with frame 4.

Defective data areas of up to two consecutive frames (512 bytes) can be successfully corrected by virtue of the previously recorded redundancy. Fig. 6 illustrates the process for correcting a defect that overlaps into frames 2 and 3. Frame 2 is reconstructed by performing an exclusive-OR operation on frames 4 and 6. Similarly, frame 3 is reconstructed from 1 and 5.

In general, defects are correctable that affect up to one odd-numbered frame and up to one even-numbered frame. For example, a block is recoverable if defective in frames 1 and 6 if the remaining frames are error-free.

Media Monitor

The fifth and final level of protection against data loss is furnished by the automated media monitor. A built-in use log automatically alerts the user of worn media by flashing a light when it is time to replace a used tape. This allows replacement of the media to avoid losing data, yet enables full use of the expected lifetime of the cartridge.

Controlling the Head/Tape Interface

by Walter L. Auyer, Charles H. McConica, David J. Schmeling, and Mark E. Wanger

ONE OF THE MOST CRITICAL AREAS in the HP 9144A, as in most magnetic storage devices, is the head-to-media (tape) interface. A considerable amount of engineering effort was spent both in examining and in the subsequent control of this interface to ensure data integrity as well as unit-to-unit interchangeability.

For optimum performance, the tape must be in intimate contact with the read/write head and accurately aligned to it. The most important alignment parameters to control are those that influence azimuth angle, tape flying height, and off-track error. The azimuth angle (head-gap-to-tape-path orthogonality) affects phase distortion and signal amplitude; both are important in data recovery. The tape flying height (distance between the tape and the head) is a function of tape tension, tape wrap angle, head penetration, and head geometry; this also affects phase distortion and signal amplitude. Off-track error (head gap position relative to the written track) can introduce erroneous data sensing (from adjacent tracks or other residual data), resulting in unwanted noise, which causes phase distortion. In practice, off-track error is more a function of the step motor positioning system than the head alignment process.

Control of the head/tape interface involves four major areas:

- Head mounting
- The head actuation system
- Head design
- Cartridge referencing.

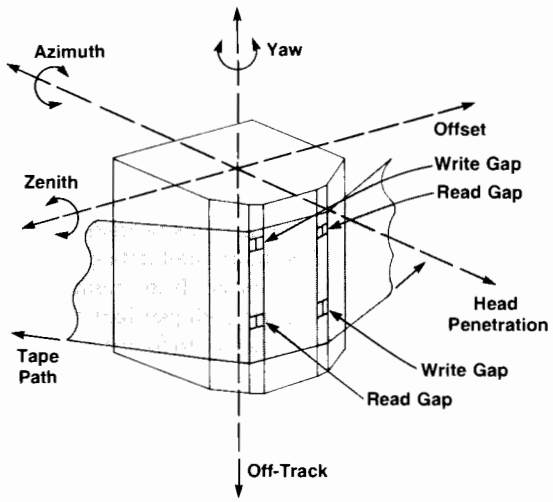


Fig. 1. *HP 9144A read/write head, showing the six degrees of head mounting freedom and the read and write gaps for the two directions of tape travel.*

Head Mounting

In the head mounting process the read/write head is aligned and mounted in the drive. The six degrees of freedom (three angles and three displacements) that affect signal amplitude and phase distortion must each be addressed (see Fig. 1). There are two schools of thought regarding head mounting precision. One favors creating a precision interchangeable mechanical assembly, including the head. The other favors mounting the head relative to the drive volume, reducing sensitivity to manufacturing tolerances, but sacrificing interchangeability. The HP 9144A design team, after carefully considering both options, chose the second because 1) the head has a lifetime ceramic wear coating which virtually eliminates the need for field replacement, and 2) the mechanical parts require less precision and therefore cost less. Since the mechanical parts do not require a high degree of precision, the design team was

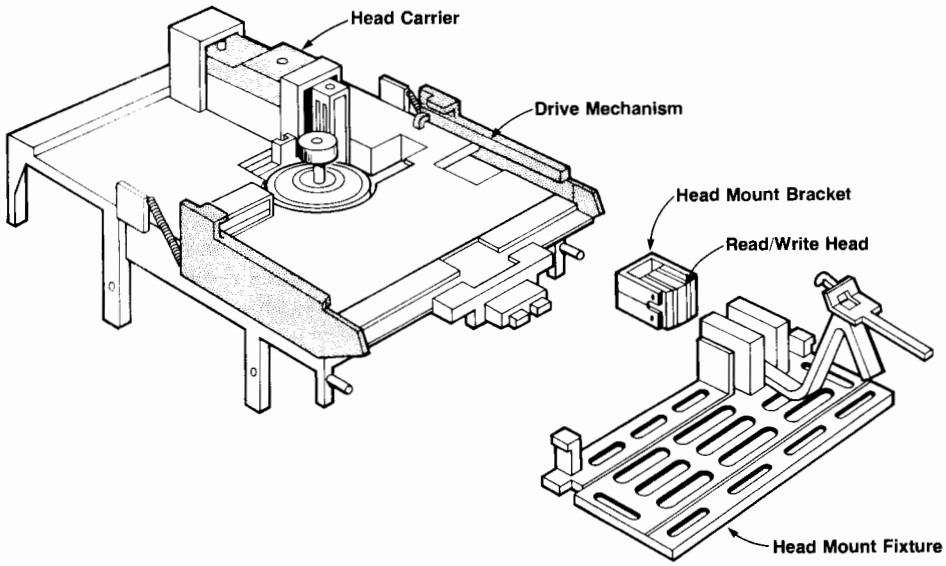


Fig. 2. *Preliminary head mount fixture.*

able to concentrate its effort on the head mounting tools and procedures to make the process fast and precise.

The head mounting process involves two steps: preliminary head mount and azimuth adjustment. The head is first aligned and clamped to a precision fixture, which simulates a data cartridge (see Fig. 2). The fixture is then inserted into the drive, which clamps and references it to the drive mechanism. This establishes five of the six degrees of freedom (all but azimuth). The head is then tacked with adhesive to a bracket, which in turn is held to the drive by a small, clothespin-like clamping fixture. The preliminary head mount fixture is then removed and the drive is ready for azimuth adjustment. The small clamping fixture holds the head and bracket assembly tightly against the head carrier, yet allows rotation to adjust the azimuth angle.

Azimuth adjustment for any type of magnetic storage device can be tedious and costly, calling for a high degree of operator skill and a large investment in equipment. The HP 9144A design team made a significant contribution in this area by designing a process that is fast, inexpensive, and requires no special operator skills. The azimuth adjustment process takes advantage of the head design and the media format. The head has two pairs of gaps (total of 4) that allow bidirectional read/write operations (see Fig. 1). The object of the azimuth adjustment is to set the in-line head gaps perpendicular to the direction of tape travel.

The data cartridges are preformatted with keys written across the width of the tape and spaced 1.7 inches apart, which functionally indicate the physical address of the data. By reading the keys with one vertical pair of in-line gaps (one read gap and one write gap) the time delay between the arrival of a key at each gap can be measured. An azimuth adjustment test station was designed using two read/write boards and a servo control board from the HP 9144A and an HP 9000 Model 216 Computer to control the process. A tape is inserted into the drive and run back and forth.

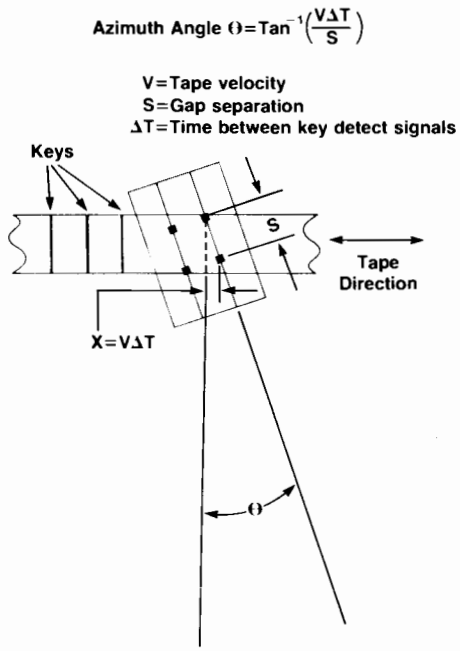


Fig. 3. *Azimuth angle calculation.*

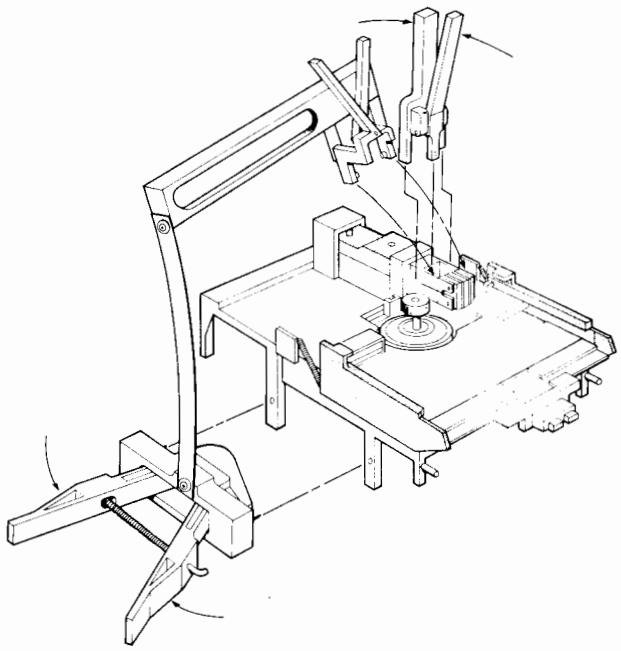


Fig. 4. *Azimuth adjustment fixture.*

As the keys cross the head, the time delay between the in-line gaps is measured and stored. A simple algorithm is used to calculate the azimuth angle from the time delay, the tape velocity, and the in-line gap separation distance (see Fig. 3).

Initially, a rotation fixture is clamped on the head (see Fig. 4). As described above, the data from a test cartridge is used to compute the existing azimuth angle. Computer-controlled corrections direct the head actuation system to step the head up or down an appropriate number of steps, thus rotating the head relative to the tape path. The final azimuth correction is set by factoring in the statistical distribution of all the azimuth readings for both pairs of in-line gaps for both directions of tape travel. Finally, a correction is made to compensate for the azimuth of the test cartridge. When the head azimuth angle is adjusted to the required specifications, the head is tacked in place with a fast-curing adhesive and all the fixtures are removed. The head is now precisely mounted relative to the drive.

Next, the head is checked for magnetic and electrical parameters. If it meets the specifications, the head and bracket are bonded to the head carrier using a high-strength adhesive.

The results of this head mounting process have been impressive. The whole mounting procedure, which took one hour during the early project stages, can be completed by production personnel in only six minutes. The azimuth angle specification is ±6 minutes, but the process is yielding a majority of heads mounted in a ±2-minute range. No part of the process requires operator judgment in setting or aligning the head. Azimuth angle, zenith angle, head penetration, and yaw are measured on each drive and recorded automatically in a data base. Control charts are used to monitor the process and maintain its consistency.

Head Actuation System

The function of the head actuation system is to place the read and write gaps accurately and repeatably on the tracks on the tape and perform such functions as edge finding and unlocking the cartridge. The off-track error is directly related to the accuracy that can be maintained in the working range of the head actuation system. A four-phase dc step motor and a lead screw result in a travel of 0.02 mm per step. The working range is 8 mm (400 steps), although the overall range is greater to allow for unlocking the cartridge. The positional accuracy over the working range is within ±1 step (±0.25%). Hysteresis in the system is compensated by using an antibacklash spring in conjunction with a routine in the servo electronics that causes the head to approach all targets from the same direction.

Head Design

The mechanical design of the head addresses two aspects of the head/tape interface, one being off-track alignment and the other being head/tape contact or tribology. Both issues are important for achieving a reliable signal from the media.

Tracks are placed on the media with an open-loop positioning system. After an initial referencing to the tape edge, any error in positioning the head or vertical tape movement within the cartridge (tape wander) leads to track misalignment and possible loss of data. The design of the head gap geometries is aimed at providing a margin for positioning error. Current head technology precludes having a trim erase geometry* with read after write capability, so a wide-write, narrow-read design is specified. The 0.013-in write gaps are 0.004 in wider than the 0.009-in read gaps. The result is that the read gap positioning can vary ±0.002 in without any signal degradation. The width of the write gaps is limited by the track density requirements and subsequent data overlap.

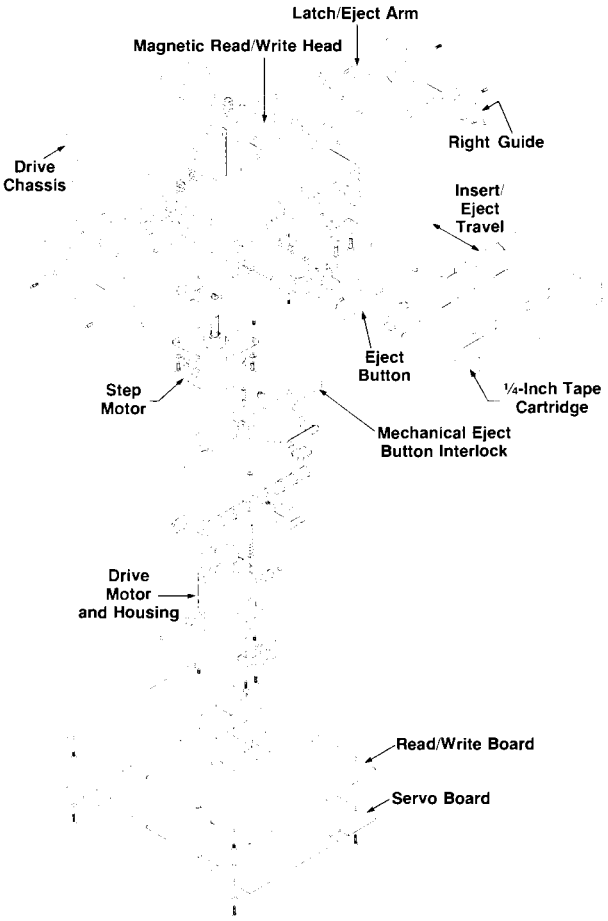


Fig. 5. *Exploded view of the HP 9144A.*

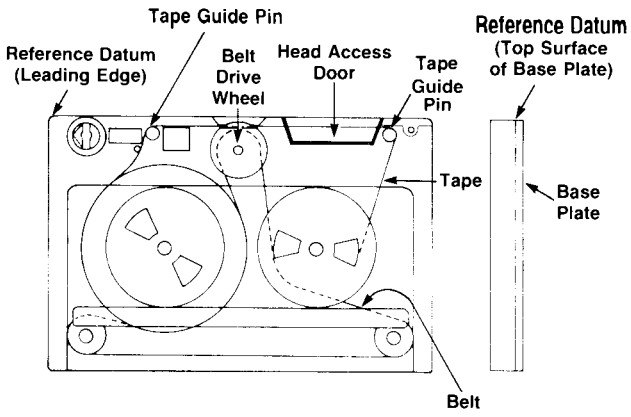


Fig. 6. *DC600 Tape Cartridge.*

The design goal for the head in relation to the head/tape interface was to supply an extremely reliable data signal over the range of cartridge variations while not requiring an extremely accurate head mounting process. Head contour design must consider variations in tape tension and wrap angle, which directly affect tape flying height. The gap configuration compounds the problem since there are four gaps, which must be held in intimate contact with the tape, which is traveling at 90 inches per second. To provide some perspective, the Van der Waal equation for signal loss from spacing (flying height) is 55 d/λ dB. At 10,000 flux reversals per inch, λ = 100 μin and a flying height of 5.5 μin (about the surface roughness of the media) results in a 3-dB loss. The final design uses a double-bump configuration with a consistent curvature on each bump. The curvature allows for variations in wrap angle while still maintaining good head/tape spacing.

We chose to use a ceramic wear layer to enhance head life. The trade-off was difficulty in working with materials of different hardness in the machining and profiling process. To get the necessary profile required working closely with the head vendor on the design and the manufacturing process.

The result of careful design and extensive testing is a head that gives a very reliable signal that is insensitive to variations in cartridges, tape tension, and tape wrap angle.

Cartridge Referencing

Equally important in controlling the head/tape interface is the relative position of the tape cartridge (and thus the

*In a trim erase geometry, two erase heads, one on each side of the data track, trim the track to its proper size after the data is written by the write head. This geometry is common in flexible disc drives.

tape itself) to the HP 9144A tape drive mechanism. Esthetic considerations (insertion and ejection forces and travel, "feel," appearance, etc.) of the mechanism also were challenging aspects of the design.

The drive mechanism, primarily a mix of motors, plastic hardware and die castings (see Fig. 5), accepts and captures an inserted cartridge, positions it relative to the read/write head, stabilizes it during dynamic drive functions (tape movement relative to the head and vice versa), and upon request, unlocks the cartridge for the user to eject.

ANSI Specification X3.55-1977 defines the parameters for the ¼-inch tape and 0.67 × 4.00 × 6.00-in tape cartridge used in the HP 9144A. The defined cartridge reference datums (cartridge position planes) are the forward (or leading) edge and the top surface of the 0.10-in-thick aluminum baseplate (see Fig. 6). Internally, the tape guide pins are positioned relative to these datums, thus establishing the tape path relative to the cartridge base plate.

The user inserts the cartridge until it firmly snaps into place. Insertion resistance forces (friction, motor capstan reaction, latch/eject arm reaction) build to approximately 3 lb. To smooth and minimize this resistance, the guides are made of Teflon™-filled plastic (not glass-filled—glass causes friction) and incorporate guide rollers for aft cartridge stabilization. During the last millimeter of insertion travel, the dual-purpose latch/eject arms are released. This results in 3.5 lb upward and forward forces applied to the cartridge, pulling the cartridge reference datums audibly, firmly, positively, and repeatably against their corresponding mechanism references. A stable head/tape interface is thus established.

Another feature of the mechanism is a mechanical eject button interlock, which prohibits the user from inadvertently ejecting the cartridge while the head is in an active, or up, position. This interlock decouples the eject button from the head/tape interface, thus preventing accidental bumping of the eject button from disturbing any read/write operations that may be in progress. Cartridge ejection must be preceded by a request for unload (a pushbutton on the front panel) which initiates a down-load sequence, subsequent head stepping down, and release of the mechanical eject button interlock.

Software Methodology Preserves Consistency and Creativity

by Mark L. Gembarowski

THE PROJECT TEAM that developed the HP 9144A Tape Drive also developed a software methodology that is now the way in which all programming is done at HP's Greeley Division. The methodology provides designers with a consistent, common approach to software design without limiting their creativity and coding style. This software methodology addresses two major questions:

- What can we do about schedule?
- How "good" is the code?

The software methodology does not generate code until the final step of the design. Yet, we can maintain or even beat schedule because the code generated is very easy to debug, extremely flexible (features can be easily added), and extendable. Many of the subroutines written for the HP 9144A are being used on new products under development because of the modularity of the code that the design methodology produces.

The software design methodology embodies a number of design ideas seen in the current literature.[1-3] They include structure charts (hierarchy charts), structured programming, top-down design, structured walkthroughs, and structured analysis. We took the best attributes of these methods and combined them into a methodology that gives the designer a series of design steps that offer additional insight into the design at each subsequent phase. The methodology generates design documentation as a product of each design step, and provides management with a series of design checkpoints for measuring progress.

Four Phases

The specific steps of the software design methodology are the definition phase, the hierarchy phase, the input-process-output phase, and the coding phase.

Definition Phase. The output of this phase is a document that details what the code must do, what hardware environment it resides in and must interface to, and a list of reference documents. This design step may include system architecture design, some structured analysis, and some testing of existing products one is trying to improve.

Hierarchy Phase. Once you know what you need to do (definition phase), you need to know how to do it. A hierarchy is a graphical representation of how the code accomplishes all of the functions listed in the definition. It shows individual modules (subroutines) and the interface between the modules. An initial hierarchy is created and then refined to improve the functionality of individual modules while reducing the interdependence between modules. This design step uses the methods of hierarchical decomposition found in much of the current software design literature. Fig. 1 shows a sample hierarchy chart.

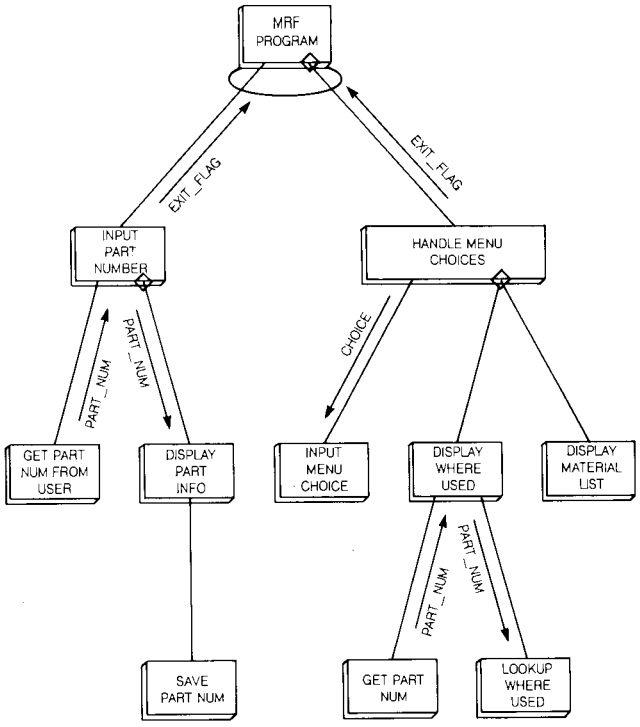


Fig. 1. *A portion of a hierarchy chart. Such charts tell how the code accomplishes the functions required. Each box with a name in it is a code module (subroutine). The arrows on the lines connecting the modules indicate parameters passed between modules. The elongated circle below the top box indicates that the subordinate calls are repeated. The diamond symbols indicate conditional calls or a selection from a group of choices.*

Input-Process-Output (IPO) Phase. Now that we have seen *how* we will do each function, we again develop *what* we will do, but this time the focus is on the individual modules rather than on the entire task to be accomplished. For each module in the hierarchy, we write a document (typically one-half page in length—it serves as an ideal header for the code) that shows the inputs to the module and their type (Boolean, real, integer, etc.), the process within the module (using inputs, subordinate module calls, and how the outputs are created), and the outputs and their type. For complicated algorithms, we expand the IPO to include a structured English algorithm to help the code writer understand exactly what the module must do. We use constructs such as IF-THEN-ELSE, REPEAT-UNTIL, WHILE-DO, and CASE and indentation to show the structure of the complicated algorithm. Once the input-process-output phase is completed, the code for any module can be written by any member of the team.

Coding Phase. Notice that no code has been generated before the design is finished. There are no constraints regarding what language the designers write in. They may be limited by design tools, but not by the methodology. When the coding begins, typically certain functions will need to be done first, most likely to help show functionality for a checkpoint meeting. Since the design is finished, portions of the coding can be set aside and done later, or new project members can do it when they join the team.

References

1. G.J. Myers, *Reliable Software through Composite Design*, Van Nostrand Reinhold, 1979.
2. G.J. Myers, *Composite/Structured Design*, Van Nostrand Reinhold, 1978.
3. E. Yourdon and L.L. Constantine, *Structured Design*, Prentice-Hall, 1979.

HEWLETT-PACKARD JOURNAL

HEWLETT PACKARD

5953-8533