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PRODUCT INFORMATION

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I

I PRODUCT INFORMATION

[1] PRODUCT DESCRIPTION

The HP 7978A is a streaming tape drive designed to provide low-cost, high-speed backup and data interchange. This drive supports 6250 CPI Group-coded Recording (GCR) and 1600 CPI Phase-Encoded Recording (PE). Nominal read/write tape speed is 75 ips and the rewind speed is 250 ips. Interface to the the Host is through the Hewlett-Packard Interface Bus (HP-IB).

Being a streaming tape drive, the 7978A requires a relatively long period of time to stop, reposition, and restart the tape. Throughput, however, is maintained at a maximum if the tape is kept moving. Therefore, whenever the command queue is empty, and the tape is moving, an attempt is made to maintain streaming.

A STREAMING DATA TRANSFER IS MAINTAINED by multi-block buffering of data and an implementation of command queueing called Immediate Response.

Immediate Response interchanges the execution phase of a command sequence with its report phase. This prevents the Host from waiting on the drive to complete a request, thus the Host is free to prepare the next request.

Immediate reported commands are placed in a command queue for execution. Data associated with write record commands is stored in a data buffer. These queued commands are executed by a Device program, which runs concurrently with the Channel program.

> The Channel Program is responsible for processing of all user interactions with the drive. User interactions include requests from the Host via the HP-IB interface and requests from the operator via the Front Panel. The Device Program is responsible for executing commands sent by the Channel Program.
>
> These programs will be discussed at length in Section V.

Immediate reports are possible on three different commands: write record, write file mark, and write gap. All other commands will not be immediate reported, and cannot receive their report until all outstanding immediate reported commands have completed.

An immediate report will not be given under certain circumstances. If the Host does not enable immediate response mode no immediate reporting will be done. If the command queue is full (twenty commands pending execution) an immediate report is not given until there is room in the queue for another command. If the tape is beyond the End-Of-Tape marker immediate reports will not be given. Lastly, if a write file mark command is received, and the last command was also a write file command, then no immediate report will be given.

Two types of errors can occur on an immediate reported command: soft errors (retries needed to successfully complete the write) and hard errors (the write failed after all possible retries were exhausted). When a soft error occurs, the drive will send back a transparent status message to the Host on the report phase of the next command. If a hard error occurs, the drive will send a failure message to the Host on the report phase of the next command. A back reference count in the status message will indicate which command actually had the error.

On the HP 7978A, the write record setup request has been enhanced to allow the Host to specify the record size. The tape drive then responds back to the Host as soon as it has the requested amount of room available

in its data buffer. This feature allows the Host to more fully utilize the drive's buffer to improve performance.

A technique called "write holdoff" is used to prevent apparent thrashing. If the tape is not moving, the drive will hold off executing immediate reported writes until there is 16K bytes of data in the buffer, five seconds elapse, or a command is received from the Host which cannot be immediately reported. The effect of write holdoffs is most apparent when the Host is sending small records, at a slow rate. The drive will not start up the tape until it has enough records or data to make it worthwhile. This decreases the number of tape repositions needed, and minimizes wear and tear on the tape transport.

When a write is completed, and another request is not available, the drive extends the interblock gap up to one inch before repositioning. This is done to help maintain streaming, hoping that another request will be received before the one-inch gap limit is reached. If a reposition is necessary, then a nominal size gap will be used between the last block and the next.

The performance of read operations is improved by "readahead". This technique enables the drive to maintain streaming when no Host request is available. Without readaheads the drive would have to reposition after a read if a Host request is not received before the next block is detected. With readaheads the drive can continue reading until it fills its buffer. Following read requests from the Host can be filled immediately from the readaheads in the buffer. When all of the readaheads in the buffer are exhausted, the device will initiate another read from tape, and the process repeats. Readahead report information is actually stored in a separate readahead queue. This queue allows file marks as well as data records to be read ahead. Thus the drive can stream across file boundries.

Readaheads may terminate before the buffer is full under certain conditions. If the readahead report queue becomes full (20 blocks read) then readaheads will stop. If an error occurs such that a retry would be needed then readaheads will also stop. Finally, if two consecutive file marks are encountered readaheads stop.

All internal data paths have some form of data integrity checking such as parity or cyclic redundancy checks. In addition, the HP 7978A has its own optimal retry algorithm. Any data written onto the tape is verified by an automatic read-after-write.

RELIABILITY is designed into the HP 7978A by use of HP-designed Large Scale Integration circuity and a simplified hardware design. These two factors, coupled with an extensive array of built-in diagnostics significantly reduce downtime.

DIAGNOSTICS are immediately entered when power is applied. This power-on testing confirms the integrity of all subsystems and of the tape drive as a unit. The operator is informed of the drive status at all times by lighted messages and numbers appearing in a two-digit alphanumeric display.

Some of the built-in diagnostics are useful to an operator and may be called individually from the Front Panel keyboard or through the HP-IB interface by the Host. A large portion of the diagnostics is meant for service use, and give the HP-trained service person a comprehensive set of tools to diagnose a problem and locate the problem to a specific Field Replaceable Unit.

Diagnostic results are displayed on the Front Panel of the drive or reported to the Host computer through the interface. Results may be interpreted, displayed, and logged by the Host or by external service equipment. With the exception of downloaded service routines, all tests and diagnostics may be run with the drive either online under direction of the Host or offline by the operator using the Front Panel.

When diagnostics are run, the HP 7978A logs any failures and the time (relative to power-on intialization) that the failure occurred. This log holds information on the last 10 diagnostic test failures.

The operating and diagnostic firmware in the HP 7978A resides in Electrically Eraseable Programmable Read Only Memory. This firmware may be updated either by reading a firmware update tape while offline or by downloading the update from the Host.

The tape path is gentle and all components are designed for long life. All wear surfaces (tape cleaner, edge guides, and tape head) are ceramic and the fixed guides are made of stainless steel. Pressure exerted by the edge guides on the edge of the tape is low and the fixed guides maintain a large radius. Bearings are derated and well lubricated. Rather than having sharp blades to scrape the oxide surface of the tape, the tape cleaner consists of a series of 90-degree vertical traps which capture tape debris.

To distinguish tape media problems from tape drive problems, there is a Front Panel indication when there has been an excessive number of recoverable (soft) errors on a section of tape. If the soft error rate is exeeded on the tape, the soft error warning remains on the display to alert the operator to the possibilities that the tape path might be dirty or the tape is faulty. The HP 7978A keeps a log of the last 20 soft errors along with the time the current tape was loaded, the number of hard errors, and the number of reportable commands since the tape was loaded.

The amount of tape which passes over the head is monitored and the cumulative total is updated in non-volatile memory every 20,000 feet.

The two tape guides and the head are mounted on the head plate, which has a precision flat surface and locates these components accurately with respect to one another. The head plate has a skew adjustment apparatus and skew is set at the factory to a middle of the tolerance range making all head assembly replacements interchangeable. There is no field adjustment of skew.

The tape path is designed to exceed 8000 hours of continuous operation.

The tape is moved directly by motors on the supply and takeup reels. No capstan is used and there is only one mechanical arm to buffer tape motion. The number of parts in the drive is minimized, especially those which touch the tape.

[2] ORDERING OPTIONS

HP 7978A Standard Product
- 6250/1600 cpi magnetic tape drive
- upright cabinet
- power configuration and power cord option taken from country code on the order.

Option 132
- 6250/1600 cpi magnetic tape drive
- installation hardware to mount the tape drive into an existing HP 7978A cabinet.

[3] SPECIFICATIONS

PERFORMANCE

TRANSFER RATE

Channel Burst Rate	1 Mbyte/second, nominal
6250 GCR Burst Recording Transfer	461 Kbytes/second, nominal
1600 PE Burst Recording Transfer	120 Kbytes/second, nominal

DATA CAPACITY (2400 ft tape)

6250 GCR	140 to 150 Mbytes (typical)
1600 PE	40-41 MBytes (typical)

MAGNETIC TAPE

Width	12.7 mm (0.5 inch)
Thickness	0.38 mm (1.5 mils) Use of 1 mil tape not supported
Reel Size	178 mm (7.0 in.) 216 mm (8.5 in.) 267 mm (10.5 in.)

READ HARD ERROR RATE

6250 GCR	$<=10^{-11}$ bytes
1600 PE	$<=10^{-10}$ bytes

SPEEDS

Read/Write/Search Speed	75.0 ips, 6250 GCR 73.7 ips, 1600 PE
Rewind Speed	250 ips

REPOSITION TIME

6250 GCR	738 ms
1600 PE	712 ms

TENSION AND BRAKING

Tape Tension	283.5 gmf (10 oz) nominal
Reel Motor Braking	Active for normal tape

	operations; passive in power failure.
INTERFACE	IEEE 488-1978 (HP-IB)
MAGNETIC HEAD ASSEMBLY	Nine-track, long-life ceramic coating; factory preset for skew and azimuth. No adjustment required.
BOT/EOT SENSING	Reflective; LED/phototransistor

PHYSICAL CHARACTERISTICS

Standard Option (tape drive with cabinet)

	In shipping container (incl. pallet and carton)	No shipping container
Height	1725 mm (68 in.)	1600 mm (63 in.)
Width	925 mm (36 in.) (viewed from pallet front)	600 mm (24 in.) (viewed from drive front)
Depth	775 mm (31 in.) (pallet front to pallet rear)	780 mm (31 in.) (drive front to drive rear)
Weight	214 kg (472 lbs)	190 kg (419 lbs)* *(excludes accessory pack)

Option 132 (tape drive less cabinet, with mounting hardware)

	In shipping container (incl. pallet and carton)	Drive Module Only
Height	895 mm (35 in.)	635 mm (25 in.)
Width	785 mm (31 in.) (viewed from pallet front)	484 mm (19 in.) (viewed from drive front)

Depth	635 mm (25 in.) (pallet front to pallet rear)	685 mm (27 in.) (drive front to drive rear)
Net Weight	84 kg (185 lbs)	64 kg (141 lbs) (excludes mounting hardware)

Drive Module On Pallet (with accessory pack and lower padding)

Weight	81 kg (179 lbs)
Height	820 mm (32 in.)
Width	785 mm (31 in.)
Depth	635 mm (25 in.)

OPERATING ENVIRONMENT

TEMPERATURE

Operating Temperature	Range is media limited: 15 to 32 C (60 to 90 F)
Storage Temperature	-40 to 75 C (-40 to 167 F)
Shipment Temperature	-40 to 75 C (-40 to 167 F)
Rate of Change	20 C (36 F) / hour (non-condensing)

RELATIVE HUMIDITY (Non-Condensing)

Operating	media limited to 20% to 80% at <22 C (78 F) maximum wetbulb temperature
Standby	media limited to 20% to 80% at <22 C (78 F) maximum wetbulb temperature
Storage or Shipment	90% at 65 C (149 F)

ALTITUDE (Above Sea Level)

Operating	3.0 km (10,000 ft)
Non-Operating	15.3 km (50,000 ft)

SHOCK AND VIBRATION

Non-Operating Shock	2-inch edge drop
Non-Operating Vibration	0.5 G for 5 to 55Hz

POWER

LINE VOLTAGE	Factory configured to 90 to 125 VAC or 198 to 250 VAC
LINE FREQUENCY	48-66 Hz

POWER CONSUMPTION (Watts)	90-125 VAC	198-250 VAC
Standby (tape not loaded)	162	147
Standby (tape loaded)	229	186
Operating (any motion)	367	397

HEAT DISSIPATION	2,074 Btu/Hr

LINE CURRENT (Amperes-max.average)	90-125 VAC	198-250 VAC
Standby (tape not loaded)	2.4	1.0
Standby (tape loaded)	3.5	1.3
Operating (any motion)	7.1	3.3

REGULATORY AGENCY COMPLIANCE

Agency	Standard
SAFETY	
Underwriters Laboratories	UL 114,478 (UL listed)
Canadian Standards Association	C22.2 No. 154-M1983 (CSA certified)
International Electrotechnical Commission	IEC 380,435 (complies)
EMISSIONS	
Federal Communication Commission	FCC-A
FTZ	VDE-B

AUDIBLE NOISE 60 dBA Sound Power

APPLICABLE STANDARDS

ANSI X3.39-1973	Recorded Magnetic Tape for Information Interchange (1600 cpi, PE)
ANSI X3.54-1976	Recorded Magnetic Tape for Information Interchange (6250 cpi, Group-coded Recording)
ANSI X3.40-1976	Unrecorded Magnetic Tape for Information Interchange (9-track 200 and 800 cpi, NRZI, 1600 cpi, PE)
ECMA-36	Data Interchange on 9-track Phase-encoded Magnetic Tape at 63 bits/mm (1600 cpi)
ECMA-62	Data Interchange on 12.7 mm 9-Track Magnetic Tape

[4] ACCESSORIES

1	-	Reel of Magnetic Tape (2400 ft)	9164-0158
1	-	Empty Reel	1490-0738
1 pkg	-	Foam-tipped Swabs	9300-0468
1 can	-	Head Cleaner	8500-1251

[5] SERVICE KITS

Inventory Parts Package (IPP) 07978-67197

Contents:

07978-66506	HP-IB Assembly
07978-66512	Preamplifier Assembly
07978-67901	Speed Encoder Assembly
07978-67908	Front Panel Assembly
07978-67905	Tape Buffer Assembly
07978-69501	Servo Controller Assembly
07978-69502	Motor Drive
07978-69504	Master Controller Assembly
07978-69505	Formatter Assembly
07978-69507	Write Assembly
07978-69508	Read Assembly
07978-69509	Phase Lock Loop Assembly
0957-0001	Power Supply

[6] CONSUMABLES

- Magnetic Tape, 2400 ft (box of 10)	92150F
- Magnetic Head Cleaner Kit	92193H
(contains all of the items below)	
Tape Head Cleaner, 4 oz bottle	8500-1914
Tape Head Cleaner, 4 oz can	8500-1251
Foam tipped swabs	9300-0468
Lint-free paper cloth	9310-4028

SITE PREPARATION AND REQUIREMENTS

SECTION

II

II SITE PREPARATION AND REQUIREMENTS

[1] SITE PREPARATION

The following paragraphs discuss the requirements for proper operation of the tape drive. For detailed site environmental information, refer to the publication entitled *Site Environmental Requirements for Tape Drives* HP #5955-3456.

[2] ENVIRONMENTAL REQUIREMENTS

The tape drive is designed to operate with an ambient air temperature range of 15° to 32°C (60 to 90°F) with a rate of temperature change not to exceed 20°C (36°F) per hour. See [4] COOLING REQUIREMENTS for recommended operating range.

NOTE

The environmental specifications listed here apply when the tape drive is not connected to a Hewlett-Packard system. When this device is connected to HP systems, the more stringent environmental specifications listed for any single HP device within the HP system are applicable and supersede these specifications.

[3] PRIMARY POWER AND EXTERNAL GROUND REQUIREMENTS

The female power outlet to be used to supply AC power to the disc drive must be checked by a certified electrician to ensure that the proper voltage is available for the tape drive. The permitted voltage range(s) depending on configuration, are 90 to 125 VAC (115 VAC nominal) and 198 to 250 VAC (230 VAC nominal). The earth (safety) ground in the power outlet must also be checked.

Be aware that the electrical load imposed by the tape drive may reduce the available voltage below the non-load value. If the line voltage is not within the correct range, check for proper wiring.

[4] COOLING REQUIREMENTS

A minimum of 70-80 mm (3 in.) is required behind the rear door to allow air circulation. Maintain a clearance of at least 1 metre (approximately 39 in.) in front of the unit to provide adequate space for opening the front door (490 mm / 19.3 in.) and for pulling the cabinet out during servicing.

The area does not have to be air-conditioned but an operating room temperature between 18°C to 24°C (65°F to 75°F, non-condensing) is recommended.

[5] LOCATION REQUIREMENTS

Position the drive away from sources of particulate contamination such as frequently-used doors and walkways, stacks of supplies that collect dust, and smoke-filled rooms.

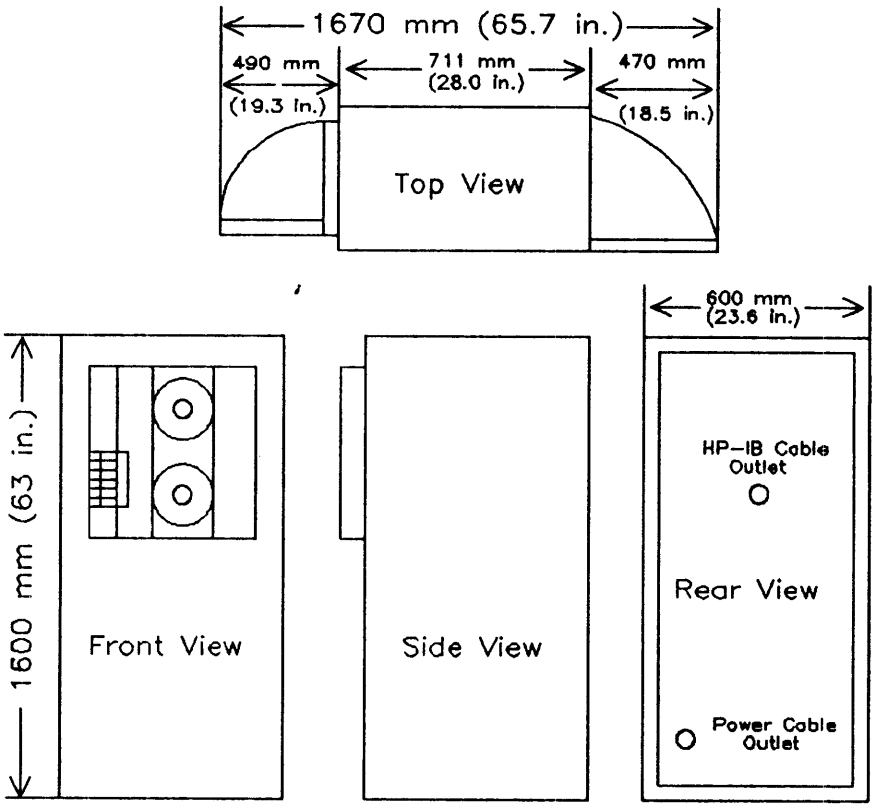

Figure (2) 5-1 HP 7978A Cabinet Dimensions

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INSTALLATION AND CONFIGURATION

SECTION III

III INSTALLATION AND CONFIGURATION

[1] INSTALLATION OF STANDARD UNIT

1.1 UNPACKING AND POSITIONING THE STANDARD UNIT

BEFORE UNPACKING THE TAPE DRIVE

Inspect the shipping container before unpacking the unit. If the shipping carton is damaged, refer to CLAIMS PROCEDURE at the end of this Subsection.

If no damage is seen on the carton, remove the carton (Steps a to c in the upacking procedures) and inspect the tape drive unit. If there is no damage, continue unpacking and move the tape drive to its operating site (Steps d through l).

UNPACKING THE TAPE DRIVE

This procedure requires a sharp knife or scissors for cutting the plastic banding material and the cardboard carton, an adjustable wrench for raising the levelers and removing the wheel stops on the pallet, and at least two people to unload the unit.

WARNING

Protective glasses should be worn while cutting the strapping bands around the drive cabinet. These straps are under tension. When cut, they may spring back and cause serious eye injury or other injuries.

SEE UNPACKING INSERT FOR PHOTOS

a) Cut the strapping bands surrounding the carton.

b) Cut the shipping carton along one of the vertical edges and across one adjoining upper horizontal edge.

c) Fold back the edge that has been cut and remove the carton from the opposite side.

d) Cut the strapping bands surrounding the tape drive cabinet.

e) Remove the cushion, ramp piece, and plastic bag from the top of the unit. The cushion and ramp piece will be used in Steps g and h to form a ramp for rolling the tape drive down to the floor.

f) One end of the pallet has steel pins sticking up through the corners. Use the wrench to remove the wheel stop from that end of the pallet.

g) Build the ramp by placing the cushion behind the pallet so that the pins protrude through the holes in the deck of the cushion.

h) Place the ramp piece at the lower end of the cushion. Make sure the pins on the lower end of the cushion protrude through the holes in the ramp piece.

WARNING

Ensure that the tape drive casting is properly secured before moving the unit. Severe injuries could result if the casting swings open while the cabinet is being pushed, especially on inclines.

The access panel for the screw that secures the casting is directly below the front panel buttons. Grasp the edges of this portion of the panel and pull. The panel is a snap fit and should come off easily. Use a screwdriver to verify that

the casting release screw is tight. Replace the access panel.

WARNING

The tape drive is heavy and difficult to move. Use considerable care during unloading. Use a minimum of two people; one pushing and one guiding it down the ramp.

SEE UNPACKING INSERT FOR PHOTOS

WARNING

The leveler feet must be raised when the drive is rolled down the ramp. If not, they could catch on the ramp and cause the unit to tip over.

i) Check that the leveler feet are raised at least 1/2" above the pallet. Use the wrench to adjust them if necessary.

j) Carefully roll the unit down the ramp.

k) Before placing the drive into its operating site, lower the rear levelers until they are .3 -.6 cm (1/8 - 1/4 in.) above the floor.

CAUTION

Do not push the drive unit when the levelers are touching the floor. The levelers may bend or break.

l) Push the drive to the location where initial installation and checkout will be performed. If the front casting will be swung out during checkout, extend the stablizer arms and lower the leveler feet to provide stability.

m) After initial installation and checkout, raise the leveler feet enough to clear the floor, retract the stablizer arms, and roll the drive into final

position. Lower the leveler feet to just touch the floor.

CLAIMS PROCEDURE

Factory warranty does not cover shipping damages caused by negligent handling. If the tape drive appears to have been damaged in shipment, notify the claim office of the carrier.

Problems determined to be factory packaging should be reported, in detail, to the factory in order to submit a warranty claim.

In all cases the unit will be repaired or replaced. Billing of the charges depend on whether the damage was caused by the carrier or caused by factory packaging. The determination of what caused the damage will be made by the Field Service Representative.

If the carrier refuses payment of damages, replacement/repair costs should be entered into the Field Engineering Support account (F.E.S.).

Be sure to include the model number and full serial number in any correspondence with Hewlett-Packard concerning the tape drive. The tape drive model number and serial number are on an identification label inside the front access panel, directly beneath the front panel buttons.

Check that all standard equipment is included with the drive unit. If any items are incorrect or missing, please contact the factory Order Processing Center with the following information:

1. Original order number or unit serial number
2. Receiving address.

1.2 CONFIGURATION OF STANDARD DRIVE UNIT

VOLTAGE SELECTION AND FUSING

The tape drive power supply is configured according to the area to which it will be shipped. Checkout procedures involve verifying that the drive was configured correctly.

The drive should have two sets of fuses; one set for 110 V operation and one set for 220 V operation.

The two sets of fuses are as follows:

OPERATION	FUSES		HP PART NUMBER
110 volt	Logic Power Supply	5 A 250 V	2110-0010
	Motor Drive	8 A 250 V	2110-0342

220 volt	Logic Power Supply	2.5 A	250 V	2110-0083
	Motor Drive	4 A	250 V	2110-0055

Check that the power cord from the Power Module has the proper connector for the country.

Verify that the part number for AC board is correct. The AC board is mounted on the outside of the Power Module enclosure. To gain access to the Power Module, refer to Section VI, Subsection 2.7 for instructions on removal of the rear panel. Only the first two steps are needed to be able to see the back of the Power Module.

For 110-volt operation, the number of the AC board should be 66511. For 220-volt operation, the number of the board should be 66521.

CABLING

HP-IB cabling requires that the total cable lengths in a configuration, both internal and external, must not exceed the total cable lengths supported by the devices in that configuration. (Cable lengths are given here in metres.)

The maximum allowed length of the HP-IB cable which connects devices to a General I/O Channel (GIC) is 7 metres plus 1 metre for each device. Two metres are used internally in the System Processor Unit (SPU) and must be subtracted from the total cable allowed. The result is that there are 5 external metres supported plus 1 metre for each device.

The HP 7978A Tape Drive accepts the HP-IB cable directly into its HP-IB transceivers and therefore has an internal cable length of 0 metres. The tape drive supports 1 metre of external cable length.

The following example shows how both the internal and external cable length ("loads") of a simple system are used to calculate the maximum amount of cable allowed between the GIC and the tape drive. The example assumes a HP3000 Series 64 computer using a GIC supporting 7 metres of cable with 2 metres of cable internally (from the SPU to the outside of the cabinet).

HP 7978 Cable length Supported	+ 1 m
GIC Cable length Supported	+ 7 m
HP7978A Internal Cable (inside cabinet)	0 m
GIC Internal Cable (inside cabinet)	- 2 m
Cable available	+ 6 m

When all supported external cable lengths (pluses in this case) are added to all existing internal cable lengths (minuses in this case), the optimum result should be zero. If there is a difference, it must be on the side of having more cable supported than actually used. If the amount of supported cable length (total of internal and external) is exceeded, spurious and hard-to-find errors will most probably be introduced into the system.

A GIC supports from 1 to 8 HP-IB peripherals. Depending on the type of peripheral and its time of use, connecting other peripherals to the GIC that supports this drive might degrade the performance of the drive to an unacceptable level.

To add some flexibility in installation, the cable length supported by the HP 7978A may be increased by using the resistor packs on the HP-IB board.

NOTE

Short HP-IB cables should not be linked together to make a longer cable. Use a single cable of the correct length.

The following is a table of HP-IB cables which could be used with a tape drive. The 31389-series cables have been improved to meet the new FCC rules which took effect October 1, 1983. The 31389-series and 10833-series are identical and both numbers are listed here.

LENGTH	ORDER NUMBER
1.6 ft (0.5 m)	10833D
3.3 ft (1.0 m)	31389A or 10833A
6.6 ft (2.0 m)	31389B or 10833B
13.2 ft (4.0 m)	31389C or 10833C

CHECKOUT OF STANDARD DRIVE UNIT

NOTE

If a review of the operational controls and indicators is necessary, refer to DESCRIPTION OF CONTROLS AND INDICATORS at the end of this subsection.

POWER-ON PROCEDURE

Plug the tape drive into the appropriate power receptacle.

The power switch is a rocker switch located on the back panel of the drive electronics. To apply power, open the back door of the tape drive and rock the switch to the left (towards the '1').

When you turn power ON, the drive immediately executes a power-on test sequence. The tape drive checks is own operating system, the digital data path, control functions, and partially checks its BOT/EOT sensing capability. No checks which involve tape movement are made at this time.

As each internal test is called, its number is shown in the display on the front panel. Many tests, however, pass by too quickly to see the number.

The most noticeable test is when the drive exercises the front panel. Each light, starting from the top, will be lit and then extinquished in order. The display will cycle through the digits from **00** to **99** and the letters from **AA** to **FF**.

Even though the HP 7978A extensively checks itself during power-on, the complete sequence should take no more than one minute.

If all subsystems pass, the STATUS light comes on green. The BUSY light goes out and the OFFLINE light comes on.

If any of the power-on tests fail the STATUS light comes on red. Also, the code **F0** appears in the display. **F0** is the failure code for the power-on selftest and is explained, with other diagnostic messages, in Section V, Subsection 2.1, DIAGNOSTIC PROGRAMS, and Section VIII Subsection 1.1, DIAGNOSTIC ERROR CODES.

After showing a failure code, the drive would place itself in a halt state, preventing any further actions until the cause of the failure is found and corrected.

NOTE

To prolong the life of the tape drive, the power should remain on continuously.

Setting the HP-IB Address ---

The HP-IB address is set using the buttons on the front panel.

Go offline-
If not offline, press the OFFLINE/RESET button to place the drive offline. The OFFLINE light should be lit.

Set display to addressing-
If the ADDRESS light is not illuminated, press the TEST/ADDRESS button to toggle the ADDRESS light on.

Select addressing mode-
Press the ENTER button to select the addressing mode.

Select address-
Each press of the TEST/ADDRESS button increments the number shown in the display. Holding the button down causes the display to increment about twice per second. Release the button when the desired address is shown.

Enter address into drive-
Press the ENTER button within 5 seconds after the address you want is shown in the display. The tape drive initializes to that address.

If neither the ENTER button nor the TEST/ADDRESS button is pressed within 5 seconds, the drive aborts the addressing mode. The ADDRESS light goes out and the display goes blank. The addressing mode may also be aborted by pressing the OFFLINE/RESET button.

Mounting and Threading the Tape ---

Open the tape path door.

Release the hub locking lever on the supply hub by catching your thumb or fingers under its lip and pulling away from the hub.

Grasp the reel of tape by hooking your thumb into the hub hole and place your fingers lightly on the outside rim. Let approximately three feet of tape dangle from the right side of the reel to give you an ample amount to lay in the tape path.

CAUTION

Do not hold the reel by the rims. Pressure on the outside edges of the tape may cause the tape to wrinkle and its edges could be damaged. Edge damage may result in hard errors that prevent reading data on the tape.

Place the reel over the hub using both hands. Press near the center of the tape reel and push the reel flat against the tape drive casting.

Hold the reel in place and lock it onto the drive hub by rotating the hub locking lever forward and down until the lever is flat with the reel hub. Ensure that the tape is flat against the casting.

CAUTION

If the tape is not squarely mounted on the drive, it may wobble during tape operations and damage the edges of the tape. Edge damage may cause hard errors that prevent accessing data on the tape.

Thread the tape along the path of the blue line on the casting. See Figure (3) 1-1.

Place the end of the tape on the top of the takeup reel in a position where you can stick a finger between the spokes of the takeup reel and press the end of the tape to the hub. Slowly rotate the supply reel clockwise with one hand (to keep tension off) as you rotate the takeup reel (also clockwise) with the other hand, keeping the end of the tape on the hub with your finger.

After a full clockwise turn of the takeup reel, the tape coming on to the reel should overlap the tape held down by your finger. Rotate the takeup reel a little more until the tape is capable of holding itself onto the reel. Withdraw your finger and, using both hands, feed tape onto the takeup reel for 2-3 more turns. Keep a small amount of tension on the tape as you rotate the takeup reel to ensure that the tape is forming a good hold on the hub.

After the tape is started on the takeup reel, check the tape where it passes over the tape guides. The tape should be centered on each guide and not riding up on the edges of the guides. If the tape is not centered on a guide, the edge may wrinkle and be damaged as the tape passes along the path.

CAUTION

Edge damage may cause hard errors and prevent accessing data on a tape.

Turn the top or bottom reels gently to take all the slack from the tape.

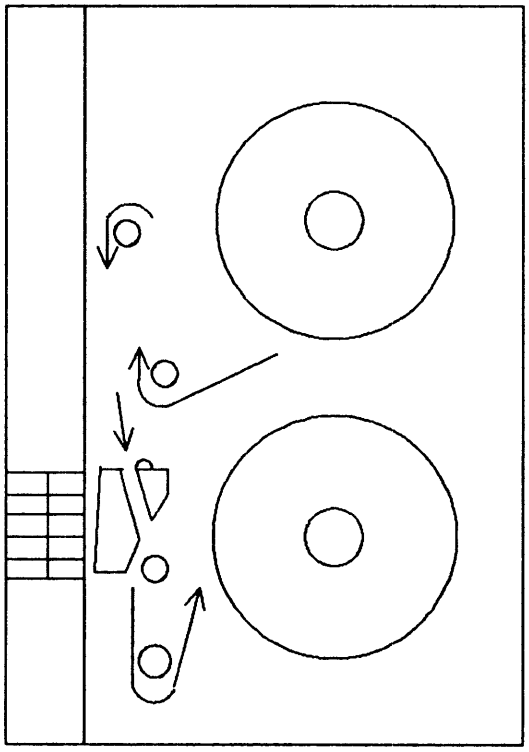

Figure (3) 1-1 Threading Diagram

Loading the Tape ---

NOTE

Trying to execute a Load command with a slack tape may cause the load operation to fail.

First, close the tape path door.

Press the LOAD button. The drive will search forward for the BOT marker. During the search the BOT light blinks. If the marker is not found within 30 feet of the point at which you gave it the Load command, the drive reverses direction and searches backwards (toward the beginning of the tape). If the BOT is not found in the reverse direction, the drive eventually rewinds the tape off the takeup reel, thereby unloading the tape drive. The error message F2 (cannot find BOT) appears in the two-digit display.

If the BOT is found, the BOT light stops blinking and remains on. The tape drive is at the start point.

Press the ONLINE button to place the drive online.

NOTE

The ONLINE button may be pressed immediately after pressing the LOAD button. The command to go online will be held until the load operation is completed and the Online command can be executed.

Rewinding and Unloading Tape ---

Tape may either be rewound online through Host commands, or offline by use of the REWIND button on the front panel.

When the Host commands a rewind operation, and the tape is somewhere between the BOT and EOT markers, the tape rewinds to the start point. The drive remains online.

To unload the tape, the operator must press the OFFLINE button to gain control of the drive, and then press the REWIND button. The tape will unload.

The Host may also command a combination rewind and go offline command. In that case, the tape drive is placed offline at the completion of the rewind command. The OFFline light comes on.

To unload the tape, the operator need only press the REWIND button.

Two situations may come up when manually unloading a tape, depending on whether the drive currently holds a valid start point in its memory or not.

If the tape drive has been placed offline (through normal commands) with the tape located between the BOT and EOT marks, and the drive has established a start point, pressing the REWIND button causes the tape to return to the start point at rewind speed. Pressing the REWIND button a second time unloads the tape.

If a load was aborted in mid tape, the start point information is lost. Pressing the REWIND button causes the tape to rewind at 75 ips and continue until the tape is unloaded.

Restart After Power Failure ---

A long-term power failure (longer than 20 ms) causes the tape drive to revert to a power-on situation. The drive automatically executes a power-on selftest when power returns. When the sequence of tests completes, the drive will be in an offline state.

If power failed when the tape was somewhere between the start point and EOT marker, first manually remove all slack in the tape and then press the LOAD button. The drive will establish tension on the tape, search forward (about 30 feet) for the BOT and, if not finding it there, search backwards until that marker is found. Press the ONLINE button when ready to resume online operations.

If the tape was at start point (which is actually a small distance short of the BOT to allow ramping up to read/write speed), the sequence is the same as just explained. However, when the drive begins its forward search for the BOT, it immediately finds the mark. The drive re-initializes itself at start point. Press the ONLINE button when ready to continue online operations.

Recovery From Tape Spooling Off Supply Reel ---

Using the blue line as a guide, thread the tape backwards through the tape path and wind it onto the supply reel in a *counterclockwise* direction. Continue winding the tape onto the reel until the EOT marker appears on the top of the reel. The marker may be up to approximately 30 feet from the physical end of the tape.

Close the tape path door.

Press the LOAD button. The drive will establish tension and then search forward until it finds a marker. In this case the marker is an EOT marker which causes the drive to reverse direction and rewind the tape at 250 ips until it reaches the BOT.

SETUP PROCEDURE

DESCRIPTION OF OPERATOR CONTROLS AND INDICATORS

The operator control panel is located on the left side of the tape path door. This panel contains 6 buttons and 12 indicator lights to control and monitor all operations of the drive. Refer to Figure (3) 1-2.

The buttons, from top to bottom, are labeled LOAD, ONLINE, OFFLINE/RESET, REWIND, ENTER, and TEST/ADDRESS. Indicator lights, across the top and down the right side, backlight the words WRITE ENABLE, 1600, 6250, DOOR OPEN, BUSY, BOT, ONLINE, OFFLINE, REWIND, TEST, and ADDRESS.

Below the REWIND light there is a light bar which indicates STATUS. To the right of this light bar is a two-digit alphanumeric display.

NOTE

The following paragraphs describe both the operation of the operator control buttons and normal responses of the tape drive to the use of the each button. Refer to Figure (3) 1-2 for the location of the control buttons.

LOAD BUTTON (1)

Purpose:
Pressing the LOAD button when the drive is offline initiates a tape load operation.

Conditions and Responses:
The tape drive must be offline. The tape must be threaded from the supply reel, through the rollers, and around the takeup reel.

While the the load operation is in progress the BOT light flashes. When the load operation completes, the BOT light comes on steady and the prerecorded density of the tape is shown in the density lights. If there is no ID BURST on the tape, both density lights will be lit.

Any errors in establishing tension or finding the BOT marker are reported to the front panel display. A load operation can be aborted by pressing the OFFLINE/RESET button. The LOAD button is inactive when the drive is online, or while an error message is shown in the display.

ONLINE BUTTON (2)

Purpose:
Pressing the ONLINE button places the drive online.

Conditions and Responses:
A tape must be currently loaded. If a load operation is in progress, the Online command is held in waiting until the load operation completes successfully. During this wait, the ONLINE light flashes. The ONLINE button is inactive while an error message is in the display, or the drive is already online.

OFFLINE/RESET BUTTON (3)

Purpose:
Places the drive offline if it is online. Resets the drive if pressed when the drive is offline.

Conditions and Responses:
If the drive is online and Host commands are being processed when this button is pressed, a warning message is placed in the display indicating that any further Host commands will be rejected because the drive has

gone offline. This warning message remains until all pending Host commands have been executed and reported back to the Host.

Pressing this button while the drive is offline terminates a load, rewind, or unload operation. All diagnostic tests approved for use by an operator (explained in Section IV) are aborted by use of this button. If the drive was placed offline by pressing the OFFLINE/RESET button as described in the previous paragraph, all pending commands from the Host are purged if the button is pressed again while offline.

This button also aborts the selection of an HP-IB address or diagnostic test number (see TEST/ADDRESS button description).

REWIND BUTTON (4)

Purpose:
Initiates a rewind or unload operation.

Conditions and Responses:
If the drive is offline and positioned beyond the start point on the tape, a rewind to the start point is initiated. If the tape is positioned prior to the start point, or if the start point is not found, the tape unloads. Rewind and unload operations both cause the REWIND light to be on steadily and the BOT light to flash until the operation is complete.

When in test mode (see TEST/ADDRESS BUTTON), the button may be used to increment the test number by 10.

This button is inactive when the drive is online, or while an error message is in the display.

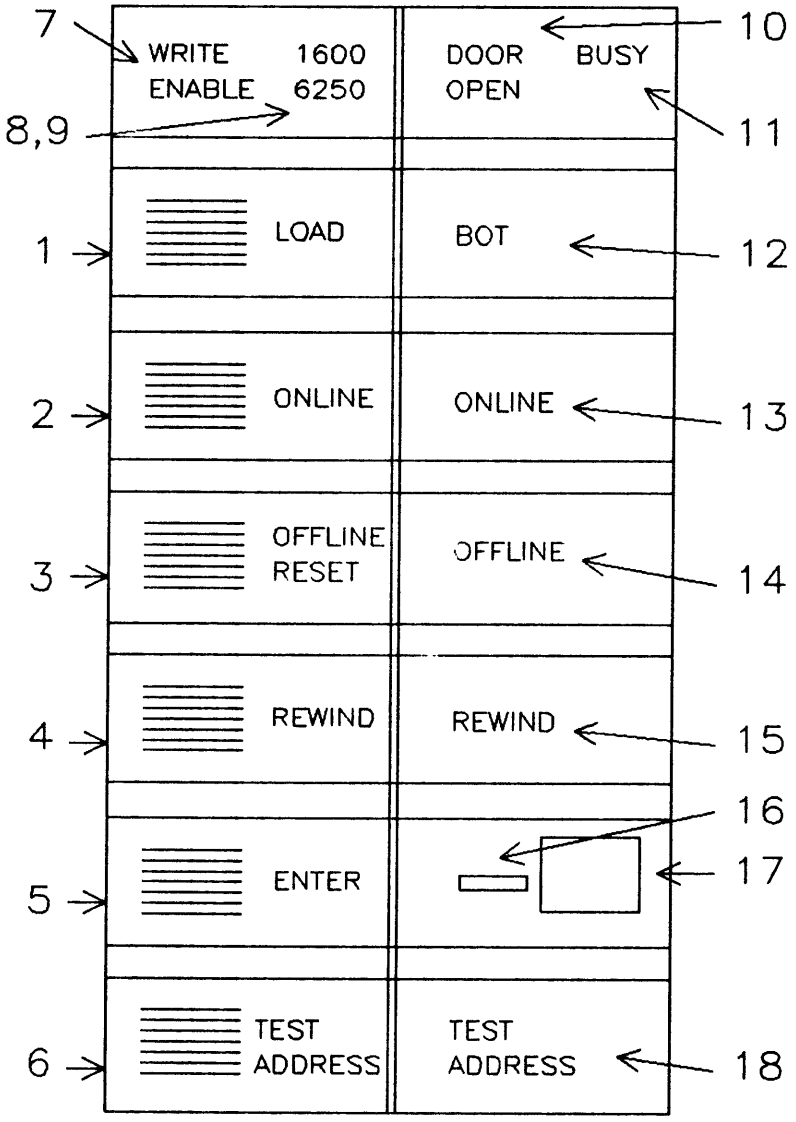

Figure (3) 1-2 Front Panel Controls and Indicators

ENTER BUTTON (5)

Purpose:
Enters the selected test number or HP-IB address into the drive.

Conditions and Responses:
See the next description, TEST/ADDRESS BUTTON.

TEST/ADDRESS BUTTON (6)

Purpose:
A two-function button: 1) pre-selects the diagnostic test mode or the HP-IB address-setting mode and 2) increments the test or address number.

Conditions and Responses:
Active only while the drive is offline. If this button is pressed while the two-digit display is off, the TEST light illuminates. Pressing this button a second time causes the TEST light to go out and the address light to be lit. Successive presses toggle between the TEST and ADDRESS modes. When the desired mode (TEST or ADDRESS) is lit, pressing the ENTER button selects that mode. The operation of the TEST/ADDRESS button then changes to that of incrementing the test number or address number.

If the ADDRESS mode is selected, the current HP-IB address is shown in the two-digit display. The range of possible addresses is from 0 through 7. Each press of the TEST/ADDRESS button increments the displayed HP-IB address by one. Holding the TEST/ADDRESS button down causes the displayed address to be incremented twice per second.

If, after incrementing to an address, the ENTER button is pressed within 10 seconds, the drive interface initializes to the number shown in the display. If neither the ENTER button nor TEST/ADDRESS button is pressed within 10 seconds the HP-IB address selection process is aborted. Address selection is also aborted if the RESET button is pressed.

Entering TEST mode causes Test Number 00 to be shown in the display. Each press of the TEST/ADDRESS button increments the displayed test number by one. Holding the TEST/ADDRESS button down increments the displayed test number four times per second. In this mode, pressing the REWIND button increments the test number by ten. Test numbers range from 0 through 79.

If, after incrementing to a test, the ENTER button is pressed within 10 seconds, the diagnostic test number shown in the display is initiated. If neither the ENTER button nor TEST/ADDRESS button is pressed within 10 seconds the test selection process is aborted. Test selection is also aborted if the RESET button is pressed.

If the selected diagnostic test passes, the display is cleared, otherwise the display shows a diagnostic error message.

POWER SWITCH (on back electronics panel inside rear cabinet door)

Purpose:
Control application of power to the tape drive.

WRITE ENABLE LIGHT (7)

Purpose:
Indicates when a write enable ring is present on the tape reel.

Conditions and Responses:
The light comes on if a write enable ring is detected during a load operation and remains on until the tape is unloaded.

DENSITY LIGHTS (8) and (9)

Purpose:
These two lights, 1600 (PE) and 6250 (GCR) indicate the current density of a loaded tape.

Conditions and Responses:
The lights are set by the Host and show the density of the tape after a load operation completes. If no tape is tensioned or if the tape is blank, both lights stay off. Tapes of unknown densities (including 800 cpi NRZI) are indicated by both lights coming on.

After a valid processing of any write density operation the density lights will be updated to reflect the current recording density. When the tape is unloaded, the density lights go off.

DOOR OPEN LIGHT (10)

Purpose:
Indicates that the tape path door is open.

Conditions and Responses:
Rather than always lighting when the door is opened, this indicator comes on only when the door is open and the drive needs the door closed to complete a tape operation.

BUSY LIGHT (11)

Purpose:
Lights whenever the drive is executing a command.

Conditions and Responses:
The command being executed may be either from the Host or the front panel. The light also comes on during execution of diagnostics.

BOT LIGHT (12)

Purpose:
Indicates that the tape is currently positioned at the start point.

Conditions and Responses:
This light stays on continuously after the completion of a load or rewind operation. While performing these operations, the light flashes.

ONLINE LIGHT (13)

Purpose:
Indicates that the drive is online and able to process tape motion commands.

Conditions and Responses:
A tape must be loaded. If the ONLINE button is pressed during a load operation, the command to go online is stored until the load operation is completed. The ONLINE light flashes until the load operation completes, then the online command is executed and the ONLINE light comes on steadily.

When the drive is placed offline this light goes out.

OFFLINE LIGHT (14)

Purpose:
Indicates that the drive is offline.

REWIND LIGHT (15)

Purpose:
Illuminates whenever a rewind command is being executed.

Conditions and Responses:
Rewind operations may be commanded by the Host or through the front panel REWIND button. When the rewind operation completes, the REWIND light goes off.

STATUS LIGHT (16)

Purpose:
Indicates the status of the drive.

Conditions and Responses:
The STATUS light bar shows green when a power-on selftest passes and red when the power-on test fails or a error message is in the display. The light shows amber whenever a warning message is in the display.

When an error condition is cleared or warning condition is corrected the light reverts to the indication appropriate to the power-on selftest status (green - passed, red - failed).

DISPLAY (17)

Purpose:
Used by the operator to set test numbers and the HP-IB addresses. Used by the drive to send messages to the operator.

Conditions and Responses:
The two-digit display is used for five categories of messages: runtime warning messages, runtime error messages, HP-IB address numbers, diagnostic test numbers, and diagnostic error messages.

An explanation of how the HP-IB address numbers appear in the display is in the TEST/ADDRESS button and ENTER button descriptions in the previous subsection. Warning messages, error messages, and diagnostic test number displays are explained in Section IV, "DIAGNOSTICS AND BASIC TROUBLESHOOTING".

TEST/ADDRESS LIGHTS (18)

Purpose:
Indicate whether test mode or address mode is selected.

Conditions and Responses:
The first press of the TEST/ADDRESS button activates the selection process. The TEST light comes on. Each subsequent press of the TEST/ADDRESS button changes the mode available for execution from test selection mode to address selection mode and back again.

When the ENTER button is pressed, the mode currently shown (TEST light or ADDRESS light on) becomes the active mode in the drive.

If no test number or address is supplied by the operator within 5 seconds of selecting the test mode or address mode, the selection is canceled, the indicator light goes out, and the STATUS light comes on.

[2] INSTALLING AN OPTION 132 (ADDITIONAL HP 7978A DRIVE MODULE)

2.1 OPTION 132 INSTALLATION

WARNING

Two people are necessary to safely unpack and install an additional drive in the cabinet.

1. Unplug tape drive unit. Disconnect HP-IB cable from system.

2. Raise levelers. Pull unit out to work area. Pull pins out of the two stabilizer foot mounts and extend stabilizer feet. Re-insert pins to lock feet in extended position. Lower levelers to the floor in front and back.

3. Remove lower front panel. Entry from the rear of the cabinet is necessary (Figure (3) 2-1).

4. If the unit currently installed in the cabinet is a HP 7974A, the spacer panel (#0784-04700, 29.2 mm) will have to be used. Mount 2 clip nuts on the panel first, and then mount the panel on the front rails as close to flush with the bottom of the HP 7974A as possible. The mounting screw holes in the panel are slightly off the horizontal centerline; mount the spacer panel so that screws are on the top half (Figure (3) 2-2).

5. Install 4 clip nuts on bottom spacer panel (#07978-00201, 198 mm) an d install panel on the front rails of the cabinet. The bottom of the panel lines up with the bottom of the drive cabinet base plate (Figure (3) 2-3).

6. Install clip nuts on the front and back vertical rails in preparation for mounting the HP 7978A Drive (Figure (3) 2-4).

   The vertical rails mounted in each corner of the drive cabinet are angle irons. Five clip nuts will be placed on the front face of the front vertical rail. The placement of these clip nuts is as follows:

   1 on each side: 3 3/4" (7 holes) down from bottom of upper spacer panel (or bottom of HP 7978A, if applicable)

   1 on each side: 3 3/4" (7 holes) up from the top of the lower spacer panel.

   1 on left side: 13 1/2" (15 holes) down from the top clip nut.

   The placement of the clip nuts on the side faces of the front and rear vertical rails, in preparation for mounting the electronics cage brackets, is shown in Figure (3) 2-5.

   Top clip nuts are 6 3/8" up from cabinet baseplate surface. The clip nuts for the bottom screws of the rail are 2 holes below the top clip nuts.

7. Install both electronics cage brackets.

   Hold the rails up as the screws are tightened. To provide support to the drive electronics cage, the brackets have to ride as high on their screws as possible.

8. Lift the HP 7978A out of the shipping carton. Each person should lift the drive by placing one hand under the drive electronics cage near the front and one hand about two thirds toward back of the cage. Most of the weight is towards the front and you want to leave a portion of the rear of the cage free to rest on the brackets as you slide the drive into the cabinet.

9. Slide the drive unit in. The press-in nuts on the sides of the electronics cage will catch slightly as you slide the cage in. Jiggle the drive as necessary to get past these nuts. Slide the cage straight back.

10. Open casting access panel. Use screwdriver and loosen casting screw. Open casting (Figure (3) 2-6).

11. Position the left side of the electronics cage so that a 10/32" socket-head screw can be inserted through the slit in the top left corner of the electronics cage and into the clip nut on the vertical rail. Use a lockwasher and flat washer as shown in Figure (3) 2-6.

12. Position the right-hand side of the electronics cage to allow insertion of a 10/32" socket-head screw in the top hole of the casting frame. Because of the angle, a 4 mm ball driver is needed to insert the screw. Before inserting this screw, tape the shaft of the ball driver to prevent marring the paint on the transport casting (Figure (3) 2-7).

13. Insert the bottom screw on the right side and two remaining screws on the left side.

14. Close the casting. Use a screwdriver to lock the casting screw.

15. Attach the 2-metre HP-IB cable. Daisychain the cable onto the HP-IB connector on the upper unit. Run the power cord out the lower hole in the rear door of the cabinet.

16. Close rear door and use a screwdriver to lock.

If there will be no access to the rear of the drives after they are rolled back to their operating location, press the HP 7978A Power Switch to the ON position before closing and locking the rear door.

17. Attach HP 7978A power label to the outside of the rear door as shown in Figure (3) 2-8.

18. Attach warning for double power cords on front of cabinet, between drive units, as shown in Figure (3) 2-9.

19. Retract the levelers to give ample floor clearance. Remove the stabilizer foot locking pins and retract both stabilizing feet. Re-insert the locking pins.

20. Roll the drives back to their operating location.

If there will be no access to the rear of the drives after they are in place, lower the rear levelers to within 1/8" to 1/4" of the floor before rolling the cabinet into position. Also, you may want to plug in the power cord and HP-IB cable.

21. Lower the levelers to the floor.

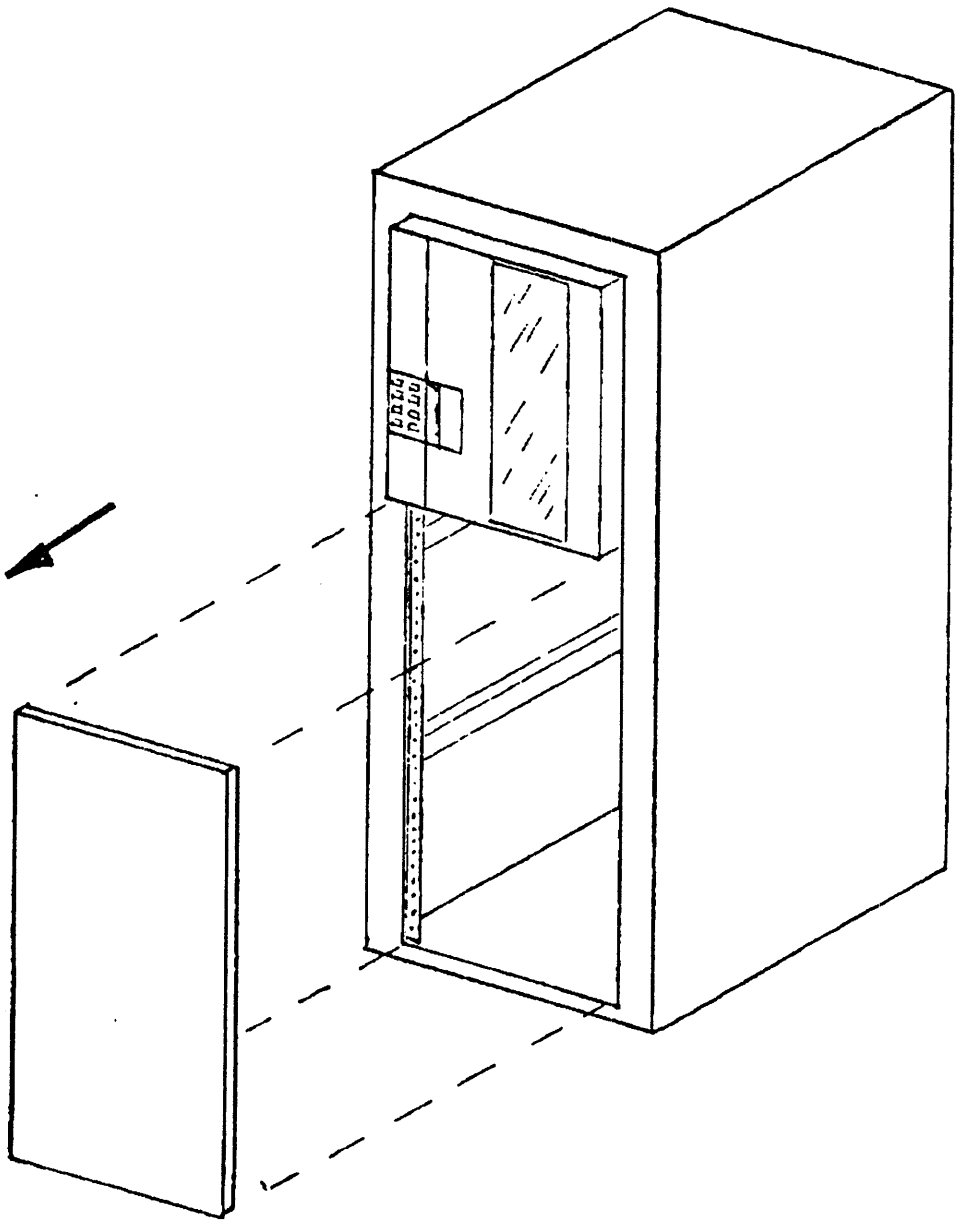

Figure (3) 2-1 Option 132 Installation- Lower Front Panel

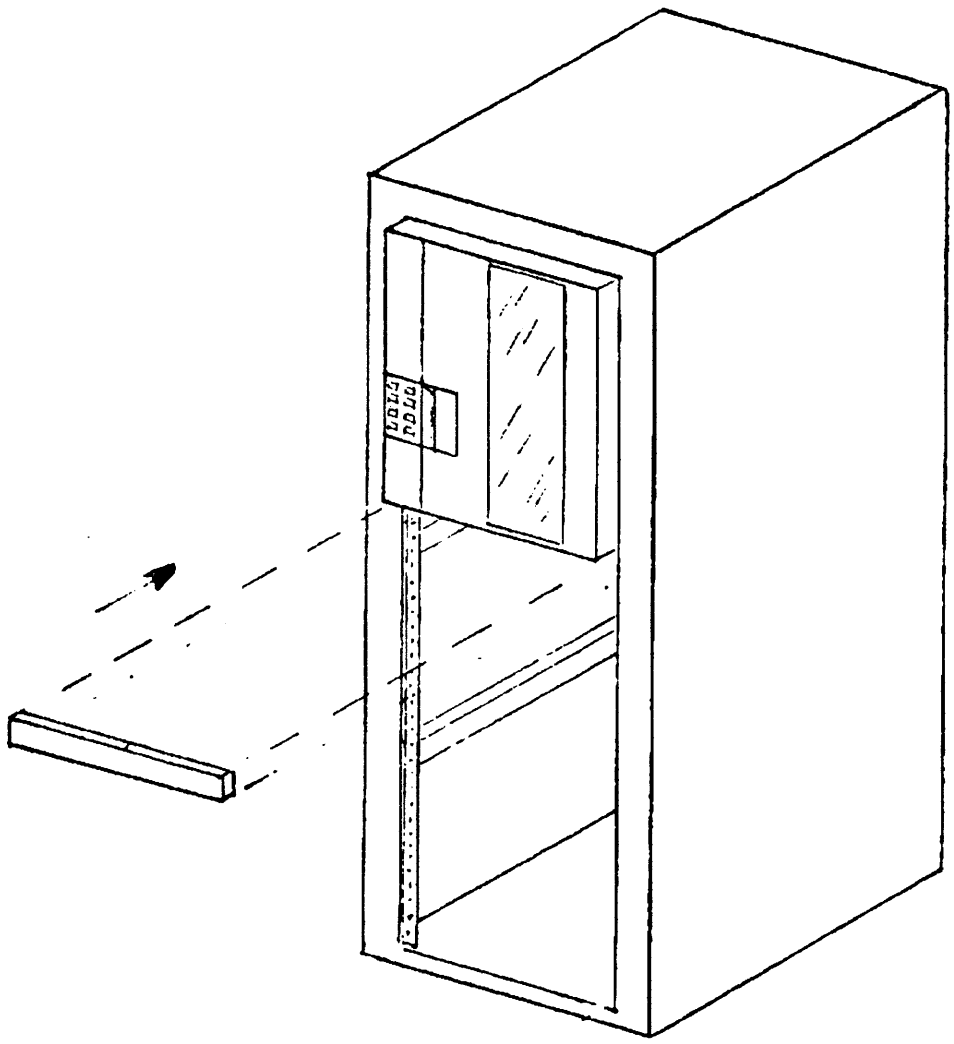

Figure (3) 2-2 Option 132 Installation- Upper Spacer Panel

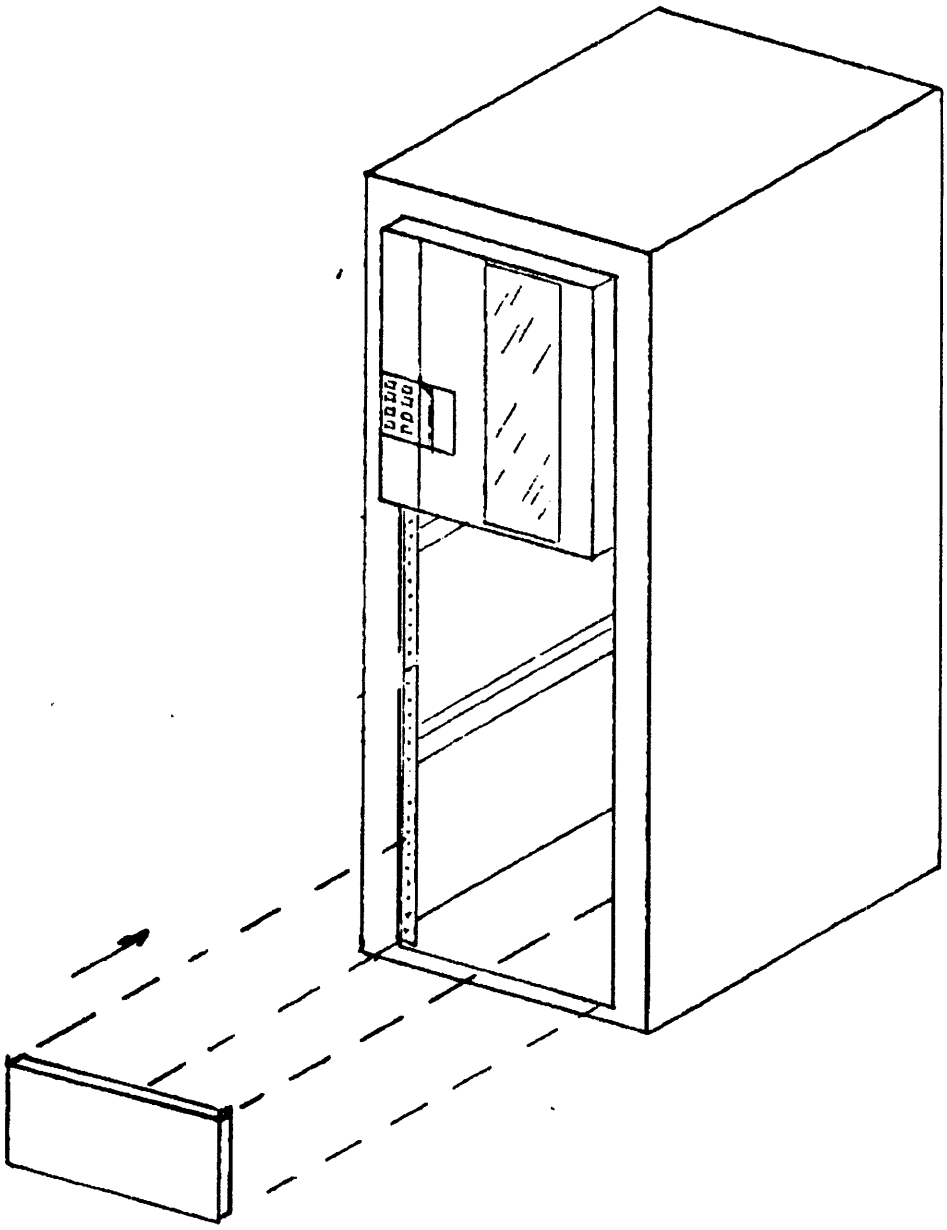

Figure (3) 2-3 Option 132 Installation- Lower Spacer Panel

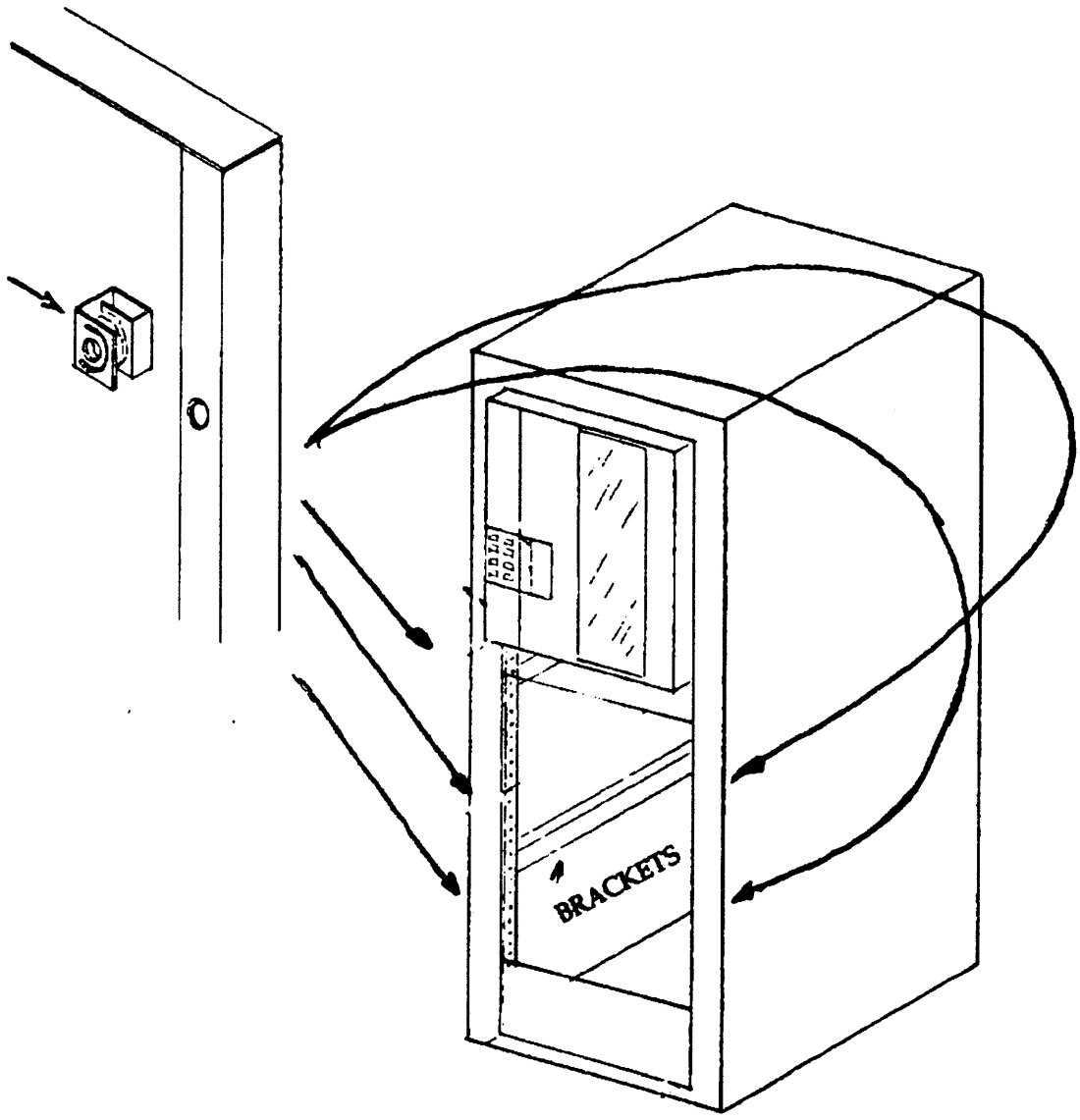

Figure (3) 2-4 Option 132 Installation- Front Rail Clip Nuts

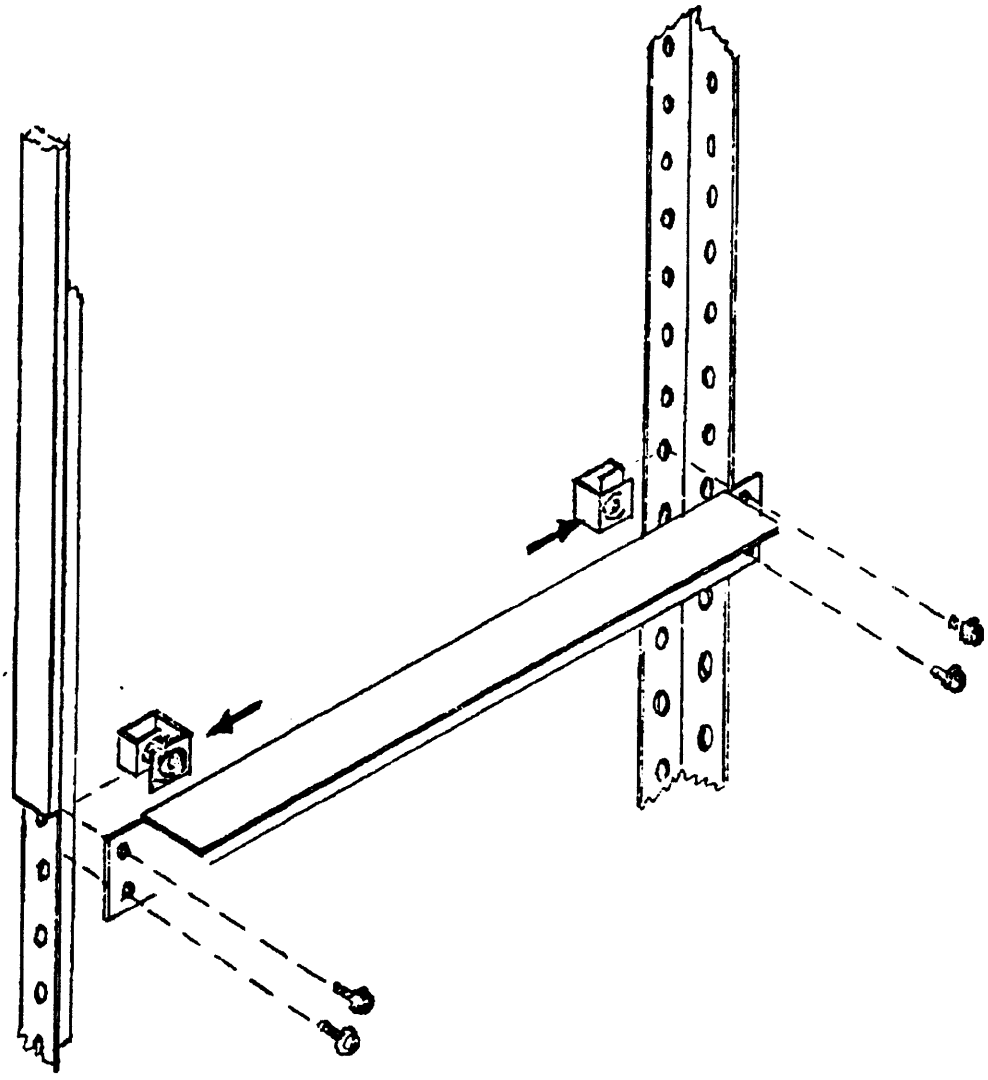

Figure (3) 2-5 Option 132 Installation- Side Rail Clip Nuts

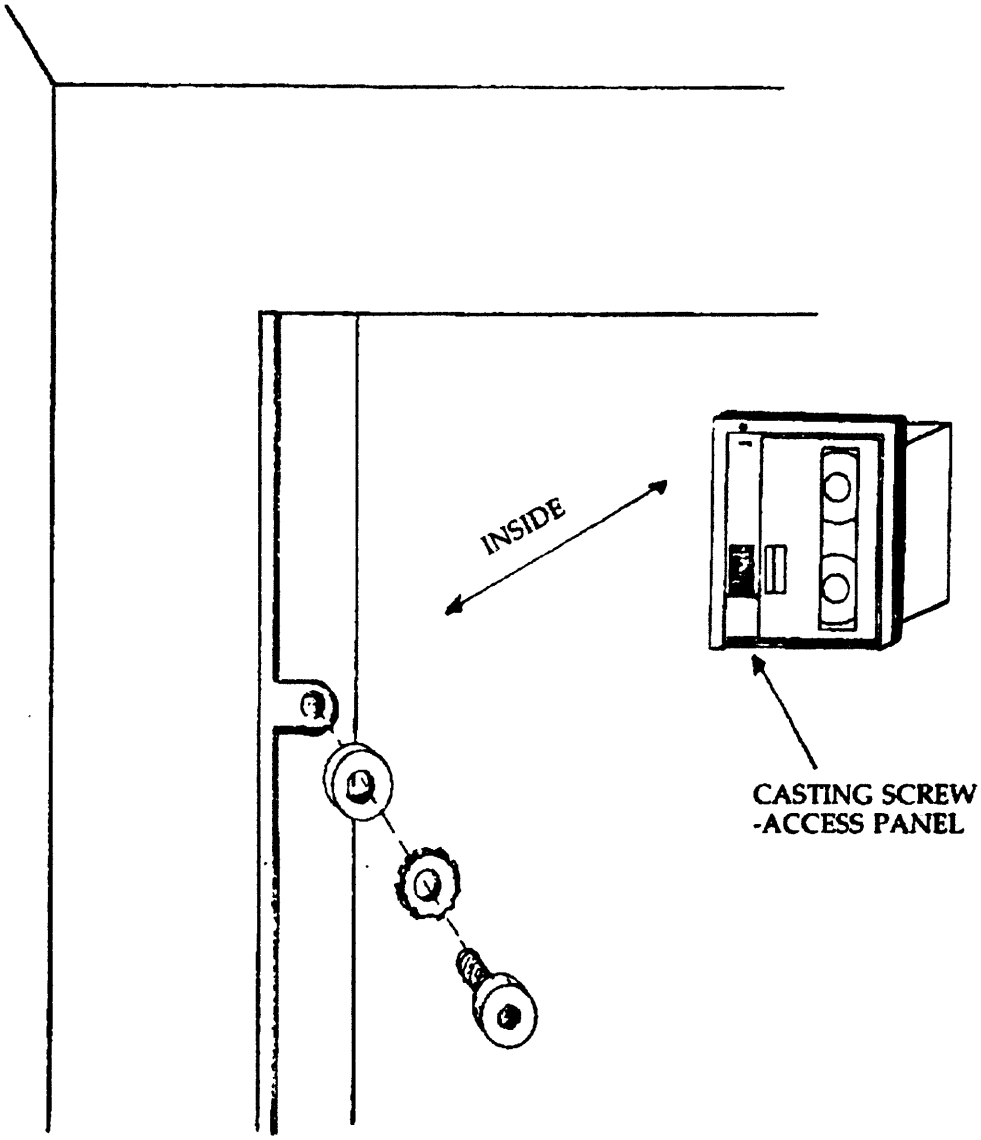

Figure (3) 2-6 Option 132 Installation- Access, Left Chassis Mounting

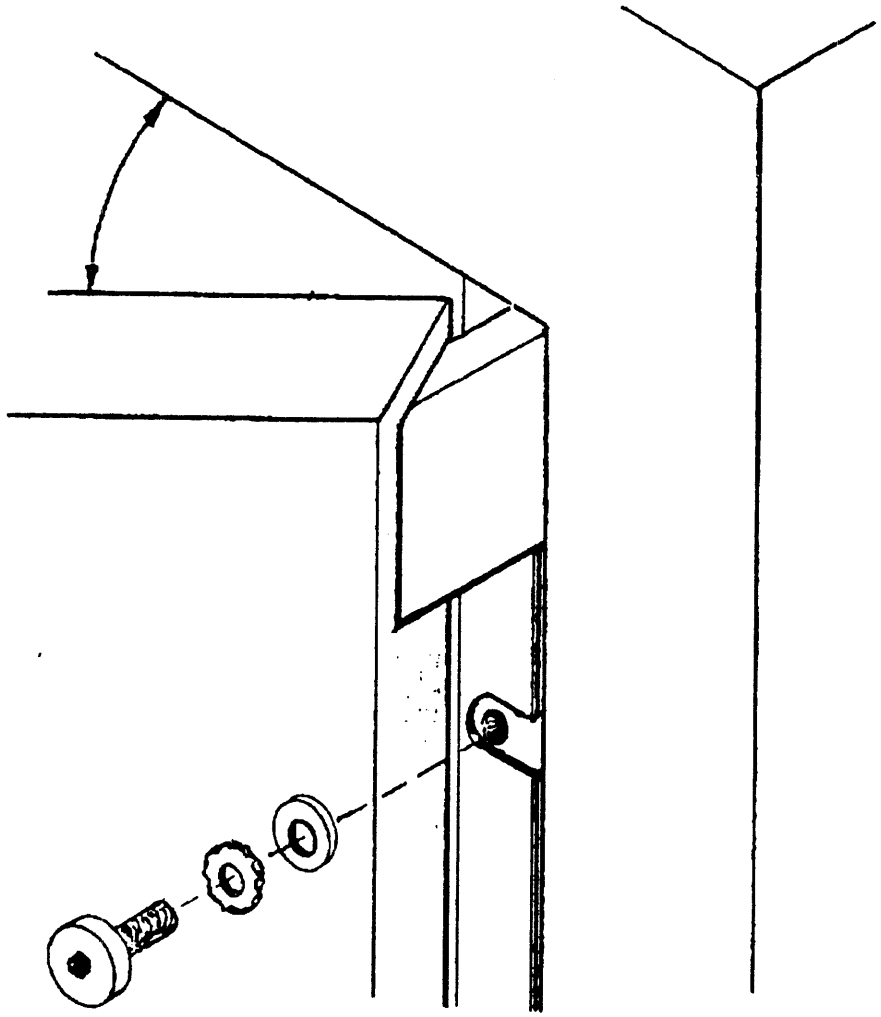

Figure (3) 2-7 Option 132 Installation- Right Chassis Mounting

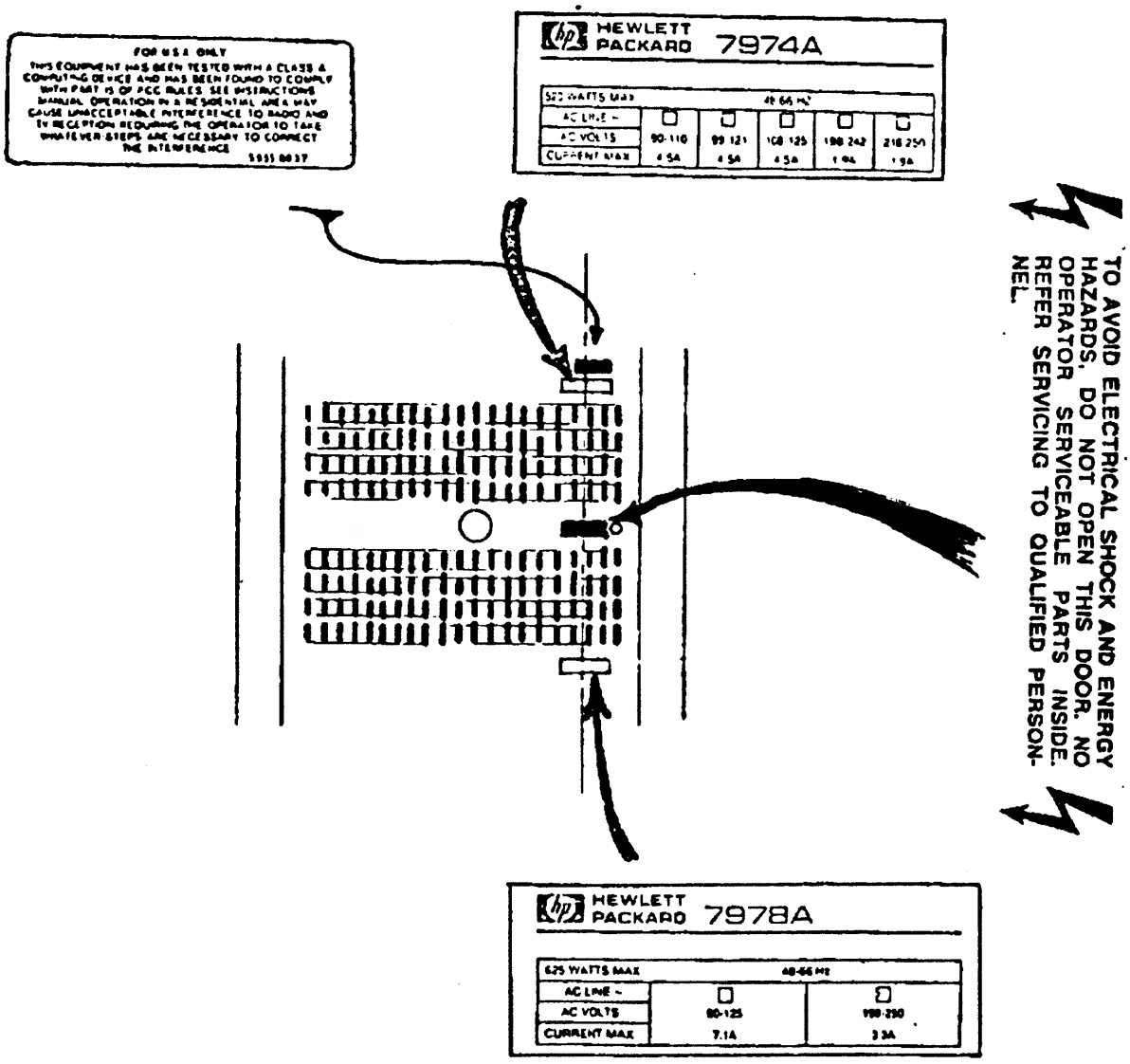

Figure (3) 2-8 Option 132 Installation- Power Label Location

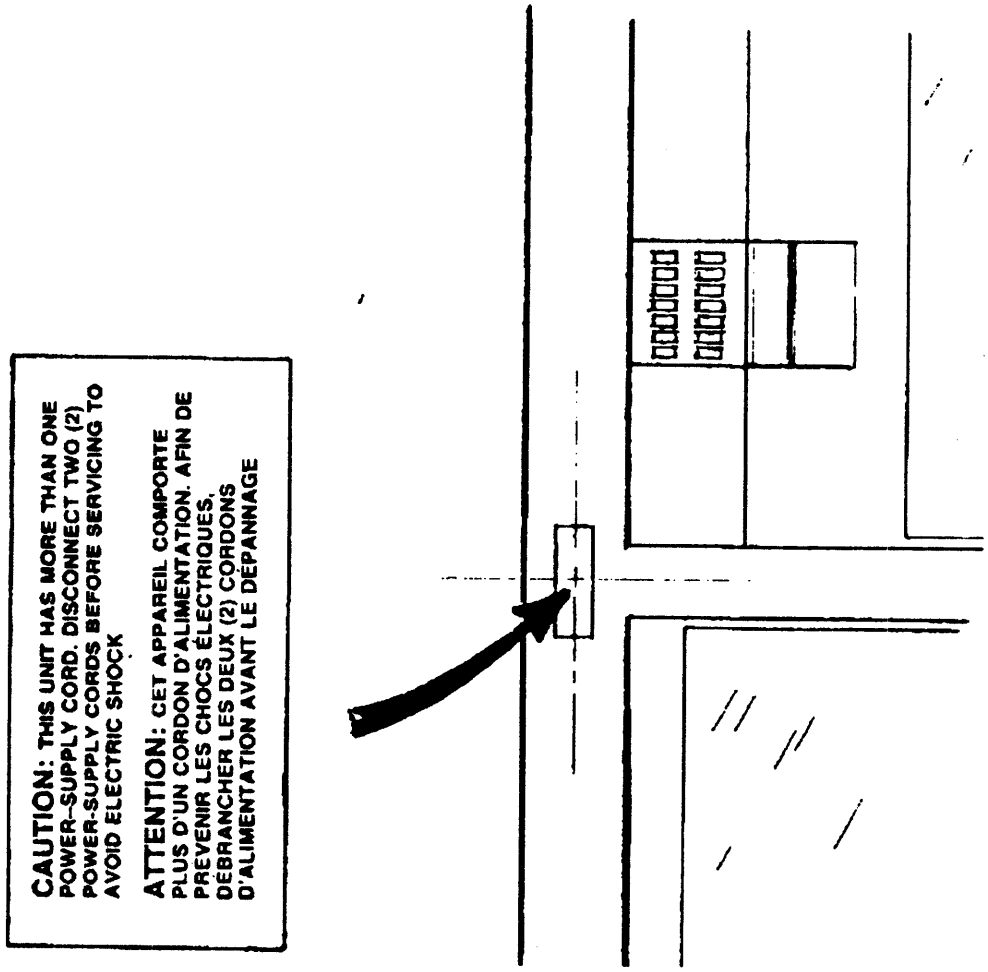

Figure (3) 2-9 Option 132 Installation- Double Power Cord Warning

2.1 OPTION 132 CONFIGURATION

See Subsection 1.2, CONFIGURATION OF STANDARD DRIVE UNIT.

[3] INSTALLING AN HP 7974A

3.1 HP 7974A OPTION 131 INSTALLATION

Refer to the HP 7974A Service Manual.

3.2 HP 7974A OPTION 131 CONFIGURATION

Refer to the HP 7974A Service Manual.

PREVENTIVE MAINTENANCE

SECTION
IV

IV PREVENTIVE MAINTENANCE
- [1] CLEANING SCHEDULE GUIDELINES
- [2] CLEANING SUPPLIES
- [3] CLEANING PROCEDURE

[1] CLEANING SCHEDULE GUIDELINES

Many transport problems can be traced to either improper cleaning or the use of poor quality tapes that leave oxide and binder on the tape path. Without frequent cleaning, collected particles contaminate tapes, cause transport failure, and, in extreme cases, ruin the tape head. Replacing the head is costly.

The tape path should be cleaned regularly. The path should be inspected for any of the following problems:

BROWN STAINING: Low humidity levels cause brown deposits of oxide to accumulate on the head. As the stain grows, tape-to-head separation increases until the head becomes useless. Once ruined, the head must be replaced.

CLEAR FILMING: Every time a tape is used it sheds oxide and binder which forms a clear film upon the head. If not removed with cleaning solvents at frequent intervals, tape-to-head separation errors occur.

CAUTION

Clear films can build up until cleaning with solvent is no longer effective and replacement of the head becomes necessary.

Frequency of cleaning depends on three factors: usage, operating environment, and tape quality. The following definitions should be used as guidelines for developing an appropriate cleaning schedule.

MINIMUM: A thorough cleaning of the tape path every shift (eight hours). Minimum cleaning is appropriate under the following conditions:

- less than 10 reels are used per shift (eight hours)
- there is no visible debris on tape head after each reel of tape
- there is no reason to suspect a high level of dust in the computer center from vacuuming, delivery of supplies, etc.

NORMAL: A thorough cleaning of the tape path after every 10 reels of tape (roughly every 1.5 hours of continuous running). Normal cleaning is appropriate under the following conditions:

- more than 10 reels are used per shift
- there is no visible debris on the tape head after each reel of tape
- there is no reason to suspect a high level of dust in the computer center.

HEAVY: A thorough cleaning of the tape path after each reel of tape under the following conditions:

- visible debris appears on the tape head after each reel of tape
- uncleaned interchange tapes from outside your computer center are being read
- uncleaned new tapes which have been used only once or twice are being used (new tapes usually contain additional debris from the slitting process during manufacture).

SPECIAL: A thorough cleaning of the tape path under the following conditions:

- abnormal dust level in the computer center because of custodial activity, equipment moves, supply delivery, etc.
- extended periods (days) of tape drive inactivity prior to use.

Most users find that they need to clean the transport once after every eight-hour work shift. However, if any of the problems listed listed previously develop or the excessive soft-error rate message **A3** begins to occur regularly, the transport should be cleaned more frequently. If an increased cleaning schedule does not improve reliability, check the tapes. Are the tapes old, worn, or kept in a dirty environment? All old and worn tapes should be copied immediately and then discarded.

If error problems persist after taking all the steps outlined above, the drive hardware may possibly have a problem.

[2] CLEANING SUPPLIES

CLEANING SOLVENT

HP supports ONLY the use of *liquid* Freon TF (trichlorotrifluoroethane) as a tape path cleaning solvent. Freon TF cuts oil and grease, evaporates quickly, leaves no residue, and will not damage the transport. Use HP Head Cleaner #8500-1251 for all cleaning on the HP 7978A.

CAUTION

Do not use cleaner solutions which contain lubricants. Lubricant deposited on the tape head degrades performance.

Do not use soap and water on the tape path. Soap leaves a thick film and water may damage electronic parts.

Do not use standard hub cleaners or strong alcohol solutions (>20%). These solutions will damage the guides and rollers in the tape path.

Do not use aerosol cleaners, even if they are freon TF. The spray is difficult to control and often contains metallic particles which damage the tape head.

WIPING MATERIALS

Use non-abrasive lint-free cloth and swabs. Discard these materials after use; even if they appear clean, they contain contamination.

CAUTION

Do not use facial tissues or cotton-tipped swabs. Although seemingly effective, they introduce highly abrasive lint into the tape path.

[3] CLEANING PROCEDURE

a) Pour a small amount of solvent into a clean container, such as a small UNWAXED paper cup.

CAUTION

Freon TF dissolves wax. If a waxed cup is used, the wax will be transferred to the tape path.

b) Dab all cloths and swabs into the container, as needed.

NOTE

To prevent debris from being redeposited on clean surfaces, clean the tape path from top to bottom.

c) While applying gentle pressure in the direction of tape path, clean the following surfaces. Give attention to the inner edges of rollers and guides. (Refer to Figure (4) 3-1 for locations).

(1)-buffer arm roller

(2)-supply reel roller

(3)-top fixed guide

(4)-top horizontal surfaces on the head assembly enclosure

(5)-tape cleaner; clean scraping surfaces and inside debris traps

(6)-read/write/erase heads (3 surfaces)

(7)-bottom edge guide

(8)-speed sensor roller

d) Use a damp, lint-free cloth to wipe the

(9)-lower left corner of the casting

(10)-inside surfaces of the takeup reel (carefully draw cloth through).

CAUTION

Be careful with the takeup reel. If it is bent or broken, damage to tapes may result.

(11)- Periodically you may also want to wipe off the rubber gripping surface on the supply reel with a dampened cloth. Hold the write ring sensor (shiny ring) back towards the casting as you wipe.

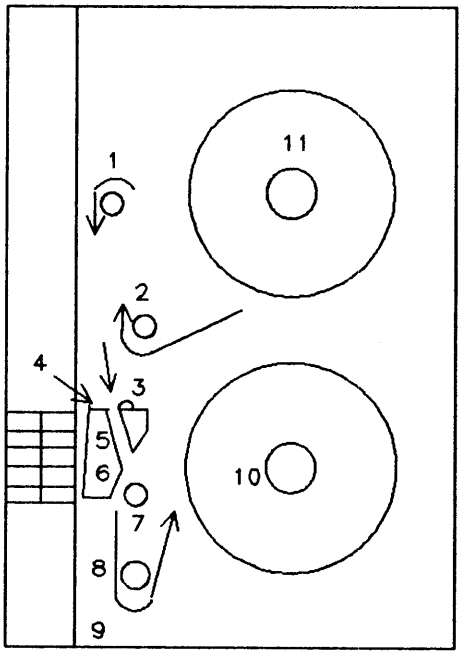

Figure (4) 3-1 Cleaning Points

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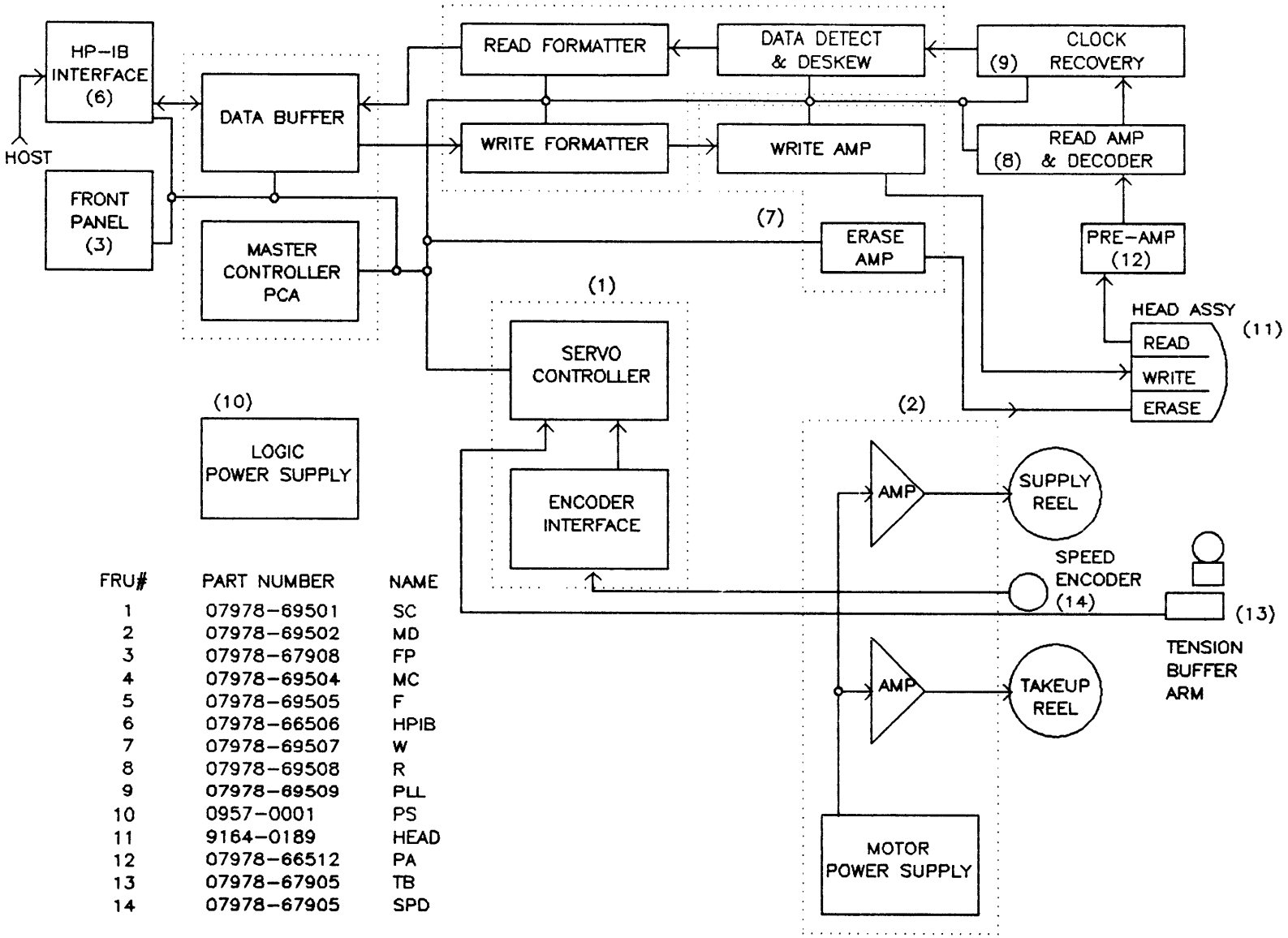
V FUNCTIONAL DESCRIPTION

Figure (5) 0-1 Overall Block Diagram



FRU#	PART NUMBER	NAME
1	07978-69501	SC
2	07978-69502	MD
3	07978-67908	FP
4	07978-69504	MC
5	07978-69505	F
6	07978-66506	HPIB
7	07978-69507	W
8	07978-69508	R
9	07978-69509	PLL
10	0957-0001	PS
11	9164-0189	HEAD
12	07978-66512	PA
13	07978-67905	TB
14	07978-67905	SPD

[1] DATA PATH

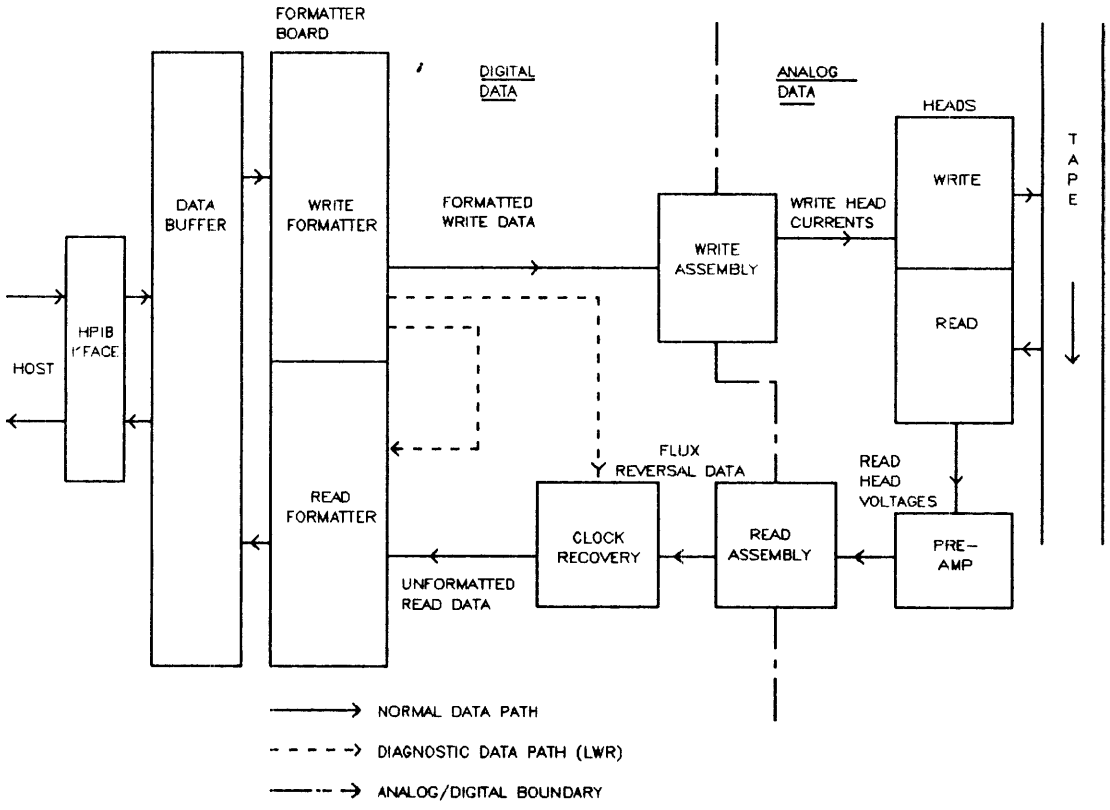


Figure (5) 1-0 HP 7978A Data Path

1.1 HP-IB INTERFACE

The ABI chip provides the high speed interfacing between HP-IB and the Master Controller as well as the Data Buffer. Together with its four transceivers, the ABI chip provides complete electrical and logical interfacing.

The interface provides 1 Mbyte/s transfer rate, parity control for data integrity, and error state handling. The interface is easily updated.

The following are the functions of the interface:

Master Controller - Read and write all ABI registers

- Write external control word
  - *clear interrupt
  - *disable interrupt
  - *buffer read
  - *buffer write
- Read external status word
  - *five bits for interrupts
  - *write request
  - *read request
  - *read or write control line
- Poll line
  - *EOR
  - *parity error
  - *secondary command
  - *EOI
  - *ABI interrrupt

Data Buffer - Read and write FIFO's via latches

- Write request when:
  - *write flag
  - *latch empty
  - *read cycle
- Read request when:
  - *read flag
  - *latch full
  - *write cycle

- send odd parity bit to buffer
- check odd parity bit from buffer
- tag byte with EOI when EOR from buffer
- set EOR when EOI
- stop transfer when:
  *EOI interrrupt
  *secondary interrrupt.

OPERATION

The ABI appears to the Master Controller as a bank of eight addressable registers and all interaction with HP-IB is performed by reading and writing to these registers. In addition, the ABI chip provides buffering for inbound and outbound data through two 8-byte FIFO's which can be accessed by the Master Controller. (Refer to the block diagram on the following page for this discussion.)

The lines provided by the ABI chip for interfacing to the Master Controller and buffer include the following:

- a 10-bit-wide data bus
- three register select lines for selecting among eight registers
- a data direction line for specifying either writing or reading to the selected register
- handshake lines to coordinate the data transfer
- an interrupt line to alert the Master Controller.

The interfacing between the I/O board and the Master Controller processor is done through the MASTER CONTROLLER CONTROL BUS, MASTER CONTROLLER DATA BUS, and the INT line. The interfacing between the I/O board and the Data Buffer is done through the DATA BUFFER CONTROL BUS, DATA BUFFER DATA BUS, and the EOR and PAR lines.

To the Master Controller processor the board appears as a set of registers. Eight of these registers are in the ABI. By writing to or reading from the registers in the ABI the processor can set the transfer conditions, transfer direction, HP-IB address of the board, send data to the Host,etc. The Master Controller can also read the status of the ABI chip, determine the reason for an interrupt, receive data from the Host, etc.

The other registers are located on the board in the EXT REG block. These registers are the CONTROL REGISTER, STATUS REGISTER, and REGISTER LATCH. The formats for these registers are as follows:

NOTE

An asterisk (*) after a signal name means that the signal is active low. This symbol takes the place of a bar over the signal name, which does not exist in the character font used for this manual.

CONTROL REGISTER (write only)
address 30810H

MSB 6	5	4	3	2	LSB 1
INT CLR	PINT CLR	BUFF RD	BUFF WR		

BIT 1 - not used

BIT 2 - not used

BIT 3 - BUFF WR. When this bit is set HIGH the transfers from buffer to ABI are enabled. This means that a buffer write request (IWRQ*) is generated for the buffer and when a byte is received IOGO* will be generated for the ABI. This bit should never be set HIGH when BIT 4 is HIGH.

BIT 4 - BUFF RD. When this bit is set HIGH the transfers from ABI to buffer are enabled. This means that IOGO* is generated for ABI when a byte becomes available. Consequently, a read request for the buffer (IRRQ*) is generated. This bit should never be set HIGH when BIT 4 is HIGH.

BIT 5 - PINT CLR. When this bit is set LOW the parity error interrupt (PAR INT) is cleared. This bit must be set HIGH to enable parity error interrupts.

BIT 6 - INT CLR. This bit has the same function as BIT 5 except for EOI interrupt, SEC interrupt, and EOR interrupt.

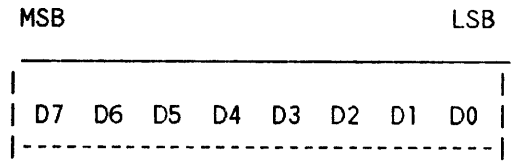
STATUS REGISTER (read only)
address 30812H

MSB 8	7	6	5	4	3	2	LSB 1
ABI INT	PAR INT	EOR INT	SEC INT	EOI INT	WR+RD	IRRQ*	IWRG*

BIT 1 - IWRQ*. Represents the status of IWRQ* line.
BIT 2 - IRRQ*. Represents the status of IRRQ* line.
BIT 3 - WR+RD. This bit is set when BUFF WR or BUFF RD bits are set in the CONTROL REGISTER.
BIT 4 - EOI INT. This bit is set when an End-of-Information interrupt is generated.

BIT 5 - SEC INT. This bit is set when a Secondary Command interrupt is generated.
BIT 6 - EOR INT. This bit is set when an End-of-Record interrupt is generated.
BIT 7 - PAR INT. This bit is set when a parity interrupt is generated.
BIT 8 - ABI INT. This bit is set when an ABI internal interrupt is generated.

LATCH REGISTER (read only)
address 30810H



This register contains the last byte transferred from ABI to the buffer. It holds the secondary command byte in case it comes from the Host during a HP-IB -to-buffer transfer.

To the buffer, the I/O board appears as a read/write register. The I/O board initiates transfers by asserting a READ REQUEST or WRITE REQUEST. The buffer handshakes these with the READ STROBE and WRITE STROBE signals. Matching between the DATA BUFFER CONTROL BUS signals and the ABI signals (IOGO, DMARQ, IOEND, etc.) is ensured by the logic state machine ABI CONTROL. This state machin also handles the enabling and clocking of the LATCH interposed between the ABI chip and the DATA BUFFER DATA BUS. Another function of the state machine is to disable data transfers when the INT block detects an interrupt condition.

The PAR block checks for odd parity on data transferred from the BUFFER DATA BUS to the I/O board and adds an odd parity bit to the data transferred from the I/O board to the DATA BUFFER DATA BUS.

Between the MASTER CONTROLLER DATA BUS and the ABI chip DATA BUS there is a buffer (BUFF) which, together with the tri-stateable latches (LATCH) enables the ABI chip to talk to either the MASTER CONTROLLER DATA BUS or the DATA BUFFER DATA BUS.

Between the ABI chip and HP-IB there is the standard configuration of transceivers (TR).

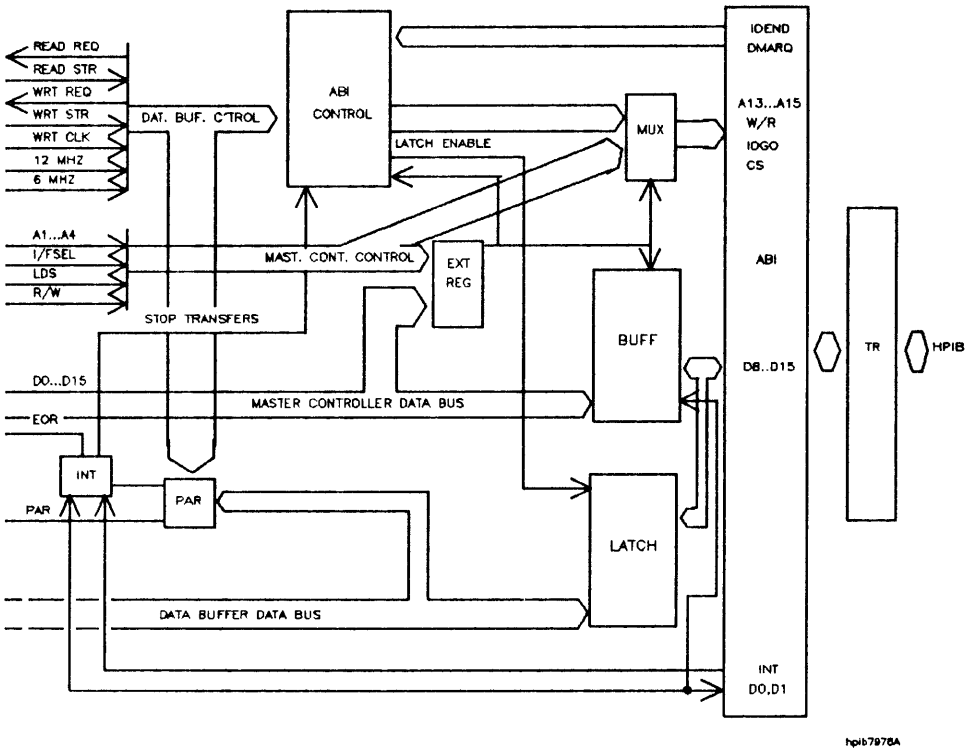


Figure (5) 1-1 HP-IB Interface Board Block Diagram

1.2 DATA BUFFER

The HP 7978A provides 32 Kbytes of Data Buffering. This buffer space enables the use of command queuing by freeing up the Interface channel between data transfers, enhances Interface channel utilization by accepting large bursts of data, and provides a data holding space for autorecovery of tape recording errors.

The HP 7978A Data Buffer is a time-multiplexed circular FIFO buffer. Push and Pop memory cycles of 333 ns are alternated. The Memory Timing and Transfer Request Logic synchronizes the requests from the peripheral subsystems to the Data Buffer's Push and Pop cycles. When a transfer request has been made, this logic generates the peripheral strobe and the memory timing signals necessary to transfer the data byte between the peripheral subsystem and the memory.

The Data Buffer Controller is a 3-MHz state machine which is programmed into the desired mode by the Master Controller. The Data Buffer Controller is implemented in two LSI chips and several TTL packages. The first LSI chip contains a 16-bit Push address pointer, a 16-bit Pop address pointer, a 16-bit 2-to-1 multiplexing address register, programmable address wraparound logic, and Master Controller Interface logic. The second LSI chip contains a 16-bit buffer fullness counter, a 16-bit transfer length counter, two 8-bit control registers, an 8-bit status register, and Master Controller Interface logic.

The Buffer memory array is twenty 16 Kbit static RAMs. Each word location has a 8-bit data byte, a parity bit, and an end-of-block flag bit.

All data bytes passing into the Data Buffer are checked for odd parity. The Master Controller is flagged if a parity error occurs.

Under normal operation the Data Buffer provides enough space for two 16 Kbyte records. If smaller records are written or read then more than two records can be buffered. When writing to the tape each record is held in the buffer until it has been successfully verified by read-after-write. When reading from the tape, each record is held in the buffer until its checksums have been successfully verified by the Read Formatter. Retry and error correcting is automatic. This is known as our autorecovery mode and is meant to relieve the Host system of normal tape drive related problems.

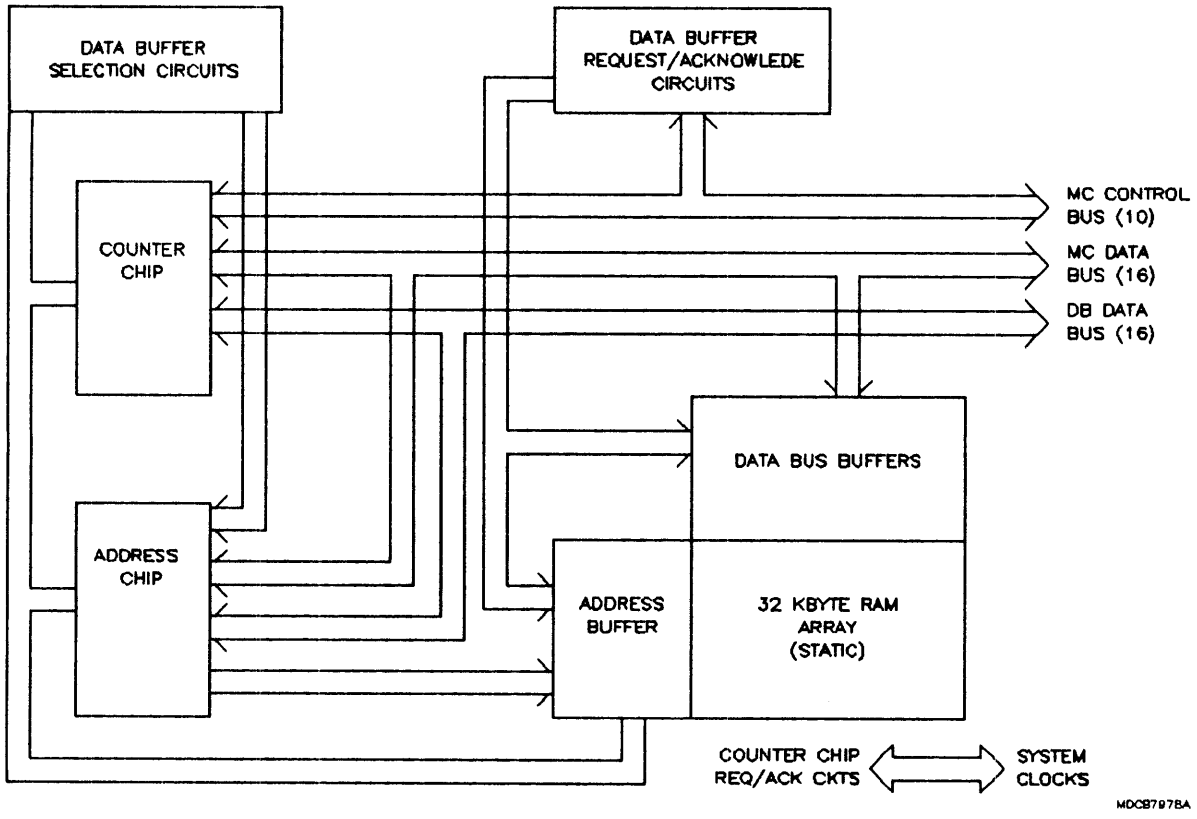


Figure (5) 1-2 Data Buffer Block Diagram

1.3 WRITE FORMATTER

The Write Formatter subassembly is the link between unformatted ASCII data to be recorded and formatted and encoded bit patterns on the tape. The three densities that can be recorded require that various marks and check characters be inserted before, during and after the data on the tape. GCR further requires that a 4-byte-to-5-byte encoding process be performed where 4 bytes of actual data are expanded to 5 bytes for storage on tape.

The Write Formatter accomplishes the formatting and mark generation with two LSI chips plus outboard TTL logic. The two LSI chips are the Write Controller and the Write Formatter. The Write Formatter is a custom LSI chip which is in the data path and does all of the actual encoding and formatting of the data. The Write Controller is a semi-custom LSI chip which manipulates the control lines of the Write Formatter chip to produce the proper data format for the density of recording chosen. The Write Controller also interfaces to the Master Controller Data Bus for commands and status.

1.4 WRITE SUBSYSTEM

The Write Subsystem can be divided into four separate sections: the Master Controller Interface, the Erase Data Circuit, The Write Data Circuit, and the Write Clock Circuit. The main control signals for these sections come from the Master Controller, but other signals are used by the Write Subsystem which are not controlled by the Master Controller. Nine of these signals are the Data Signals (DA1-DA9) from the Write Formatter. The other two signals which are not controlled by the Master Controller are the Power Good Signal (PWRGD) from the main power supply, and the Write Ring Signal (WRT RING) which comes from an optical sensor on the main casting via the Servo Controller Subsystem. These last two signals are used to protect data on tape.

MASTER CONTROLLER INTERFACE

The Master Controller Interface provides two write registers and one read register. The write registers are called register 0 and register 1. Register 0 controls the frequency of the Write Clock and Register 1 controls the Write Data Circuit and the Erase Data Circuit. The Read Register is used to provide status and diagnostics data used by the Master Controller.

SIGNAL DESCRIPTION

The input signals to the Master Controller Interface are D0 thru D15, RS1, WS not, R/W*, WRT SEL not, SYSTEM RESET, WRT RING, CLK COUNT(8 bits), ERASE ON, and WRT SAFE. Output signals from the Master Controller Interface are the two write registers REG 0 and REG 1 (to Write Subsystem hardware), and the Read Register (to Master Controller).

Input Signals --

D0 thru D15 - The lower and upper bytes of the Master Controller Data Bus.

RS1 (Register Select 1) - Selects either Register 0 (RS1="0") or Register 1 (RS1="1") to receive data from the Master Controller.

WS* - The write data strobe from the Master Controller.

R/W* - Selects the direction of the read/write operation from the Master Controller.

WRT SEL* - The Write Subsystem select line (active low during any read or write operation from the Master Controller to the Write Subsystem).

WRITE RING - An input to the Read register on bit D0 from the Servo Subsystem. WRITE RING="1" indicates to the Master Controller that the Write Subsystem is not write protected.

WRT SAFE - An input to the Read register on bit D1 from the Write Data Circuit. WRT SAFE="1" indicates to the Master Controller that the Write Subsystem is write protected.

ERASE ON - An input to the Read register on bit D2 from the Erase Data Circuit. ERASE ON="1" indicates to the Master Controller that the Write Subsystem is erase protected.

CLK COUNT - An 8 bit value located in the upper byte (D8-D15) of the Read register. This value is an output from the WRITE CLOCK CIRCUIT which is approximately equal (plus or minus one count) to the System Clock(12MHz) divide by N number minus two . It is used by the Master Controller to verify proper operation of the Write Clock Circuit.

Output Signals --

WRITE SUBSYSTEM WRITE REGISTERS

REGISTER 0 (REG 0)-

This is an 8-bit register which controls the frequency of the Write Clock Circuit. The value in REG 0 is the 2's complement of the desired divide-by-N number of the System Clock (12 MHz).

REGISTER 1 (REG 1)-

D0 to D3 - 4 bits which control the program voltage supply VBIAS.

D4 to D6 - 3 bits which select the duration of the Write Clock Delay signal COMP.

D7 - This bit of REG 1 is not used.

D8 to D13 - 6 bits which control the value of the signal VI. VI is the steady state write current control voltage.

D14 - This bit enables the Erase Data Circuit. If WRT RING="1", then D14 turns on the erase current(65mA).

D15(WREN) - This bit enables (WREN="1") the Write Data Circuit. If WREN ="0", then bit D1 (WRT SAFE) of the Read register should be set(WRT SAFE = "1").

ERASE DATA CIRCUIT

The Erase Data Circuit has three main functions. Its first function is to erase all flux transistion data from the magnetic tape media. The second function of the Erase Data Circuit is to not erase "write protected media" (tapes without a plastic write enable ring inserted). The third function of the Erase Data Circuit is to not destroy data during a power up, power down, or power failure sequence.

The Erase Data Circuit has three input signals and two output signals. The input signals are PWRGD (Power Good from the power supply), ERASEN (Erase Enable from bit D14 of REG 1), and WRT RING (from Servo Subsystem). The two output signals are Erase Head Current and ERASE.

The basic erase circuit is simply a current source which is in series with a transistor switch. The current source is made from a darlington transistor and an op amp. The DC value of this current source is approximately 65.3 mA.

The switch is a NPN transistor with its base driven by an open collector TTL AND gate. The PNP darlington circuit connected in series between the erase circuit NPN transistor switch and the erase head connector pins is the PWRGD shutdown circuit. This circuit is controlled by the PWRGD line from the main power supply and is normally turned on by a voltage on the PWRGD line which is greater than .7 Vdc.

WRITE DATA CIRCUIT

The main function of the Write Data Circuit is to record the 9 bit parallel data stream on the DA input lines (DA 1-9 correspond to track 1-9 on the tape and magnetic head) by converting logic transitions on the DA lines to magnetic flux transitions on the tape. This is accomplished by switching current inside a bifilar-wound, center-tapped, magnetic (mu-metal) write head.

The secondary function of the Write Data Circuit is to provide a secure "write protect" system. This is accomplished using four separate means:

1) User Initiated (i.e. removal of the write enable ring)
2) Power Supply protection (PWRGD signal low)
3) Protection during system turn-on(RESET line)
4) Feedback to Master Controller using WREN and WRT SAFE

The Write Data Circuit is composed of 9 write current driver circuits and three other circuits which support the write data function. These circuits are the Write Compensation Delay Circuit, the Write Current Supply (VI), and the Write Driver Bias Supply (VBIAS).

The Write Current Driver Circuit is basically a cascode differential NPN transistor connection with a programmable current souce in the emitter circuit. This current source provides the steady state current drive for the Write Current Driver Circuit. The magnitude of the current source is set by the Write Current Supply and is equal to the voltage VI/25 ohms. Also connected in the emitter circuit of each Write Driver are the two Pulse Compensation Resistors.

These two resistors (valued 316 & 590 ohms) which are connected to the outputs of two open collector NAND gates set the magnitude of the compensation current pulse. The compensation current pulse is switched on by any transition of the Data Input Line (DA line) and it is switched off by Write Compensation Delay Circuit in approximately 80% of a minimum bit window. A positive transition of a DA line switches on the gate with the 316 ohm pull-up and a negative transition of a DA line switches on the gate with the 590 ohm pull-up.

Data and Inverted Data from the DA lines are input to open collector AND gates which alternatingly drive the lower bases of the cascode differential drivers. This switches current from the center tap of the write head thru either side of the write coil winding. The other input on each AND gate is driven by Register 1 bit D15 (WREN1 & WREN2). When this bit is low, the write current is disabled. The bases on the upper transistors of the cascode differential drivers are parallelled together and connected to the Write Driver Bias Supply (VBIAS). Note: When the voltage VBIAS is < .8 V the write current is disabled.

The collectors of the upper transistors of the cascode differential drivers are connected to the write head through a response compensation network. The series 82.5 ohm resistors, the 390 ohm resistors, and the 16V zener diode help to damp the response of the write current when it is switched. The series 82.5 ohm resistors also help dissipate power to protect the driver transistors. The 4.7 ohm carbon composition resistor which is connected in series between the +12 V power supply and the write head center tap acts as a fuse to protect the write head windings in case of a short circuit connection.

The Write Compensation Delay Circuit is composed of a set of cascaded serial to parallel shift registers, a trigger latch, and a digital 8-line-to-1-line MUX. A positive transition of the Write Clock triggers the circuit and causes a pulse (TTL) to be clocked down the shift register by the 12 MHz System Clock. The duration of the delay is set by the digital MUX selecting different taps from the shift register. The MUX is controlled by bits D4,D5, and D6 of write register 1 (REG 1).

The Write Current Supply (VI) sets the steady state write driver current.

The output is padded to 2.00 V full scale. The circuit is composed of an 8-bit current-steering digital-to-analog converter and an op amp which is connected in a current to voltage converter mode. The output (VI) is connected to each track's current source voltage input (the + terminal of the current source op amp). The DAC uses the +2.5 +/- 1% voltage reference (VREF) and the 6 most significant bits in the upper byte of Register 1 (D8-LSB to D13-MSB).

The Write Driver Bias Supply (VBIAS) is composed of a buffered op amp current-to-voltage converter and an 8-bit current steering DAC. The DAC is used in the 4-bit mode with the four lower bits pulled high and the 4 upper bits controlled by Register 1 D0-LSB to D3-MSB. The output at VBIAS ranges from about .5 V to 9 V full scale. When the circuit is disabled, the output can be as low as 0.1 V.

The Bias Supply has many functions. It provides a write current disable when it is lower than .8 V and, when operational, it controls write current rise time and write driver transistor array power dissipation. These are the conditions which cause the Bias Supply to disable the write current

WRITE CLOCK CIRCUIT

The Write Clock is a divide-by-N counter which is derived from the 12-MHz System Clock. The main function of the Write Clock is to clock write data out of the Write Formatter Circuit during a record data operation. The Write Clock also triggers the Write Data Circuit's pulse compensation circuit in sync with the write data and provides a clock at the expected data rate for the Read Board Threshold Circuit.

The Write Clock Circuit also contains a secondary counter which counts 12-Mhz edges between each write clock pulse and stores the count (CLOCK COUNT) in the upper byte of the Read Register on the Write Subsystem.

The Write Clock is composed of two cascaded 4-bit counters. The circuit operates by counting up to FF H which generates a ripple carry out pulse (83.3 ns or one 12-MHz period). This pulse is inverted and used to initiate a load sequence in the counters. The ripple carry is also input to a D latch which is clocked by the inverted 12-MHz System Clock. The buffered output of this D latch is the Write Clock signal. The control bits (lower byte) are stored in Register 0. In order to obtain a certain divide by N from the Write Clock Circuit, the two's complement of N (N bar + 1) must be written to Register 0.

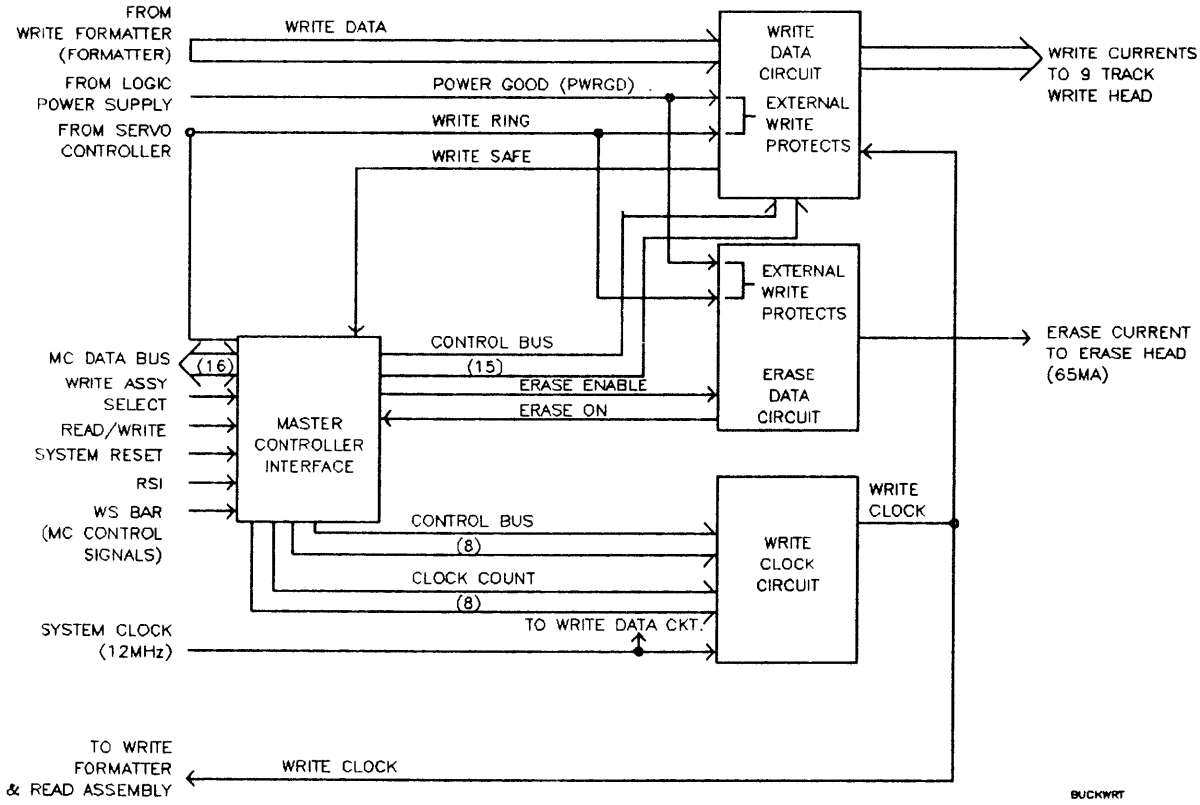


Figure (5) 1-3 Write Subsystem Block Diagram

1.5 HEAD ASSEMBLY

TO BE FILLED IN

1.6 READ PREAMPLIFIER

The Read Preamplifier board amplifies the analog signals recovered from the tape via the read head. These analog signals are converted back to digital information later.

The input to the preamplifier is the read coil. The coil has a center tap to ground which creates two balanced ouputs that are fed into the differential inputs of the preamplifier. These balanced inputs are also terminated with resistors to ground. The resistor becomes the dominate parallel resistor seen by the read coil. By doing this the Q factor of the coil is lowered and is more controlled. The Q is lowered such that the amplitude of signals from the tape are not decreased significantly, but unwanted higher frequency signals are attenuated. This type of termination is helpful in decreasing radiated susceptibility.

The amplifier consists of one chip per channel. This chip is a Signetics video amplifier (NE592) which has three non-padded gain settings. The three possible gains are 10, 100 and 400. The preamp is set for a gain of 100. The reason for setting the gain to 100 is because the amplitude of PE data is high enough that the output of the preamp would be saturated if a gain of 400 were selected.

The output stage of the preamplfier consists of a simple RC lowpass filter. The cutoff of the filter is approximately 5 megahertz. The reason for the filter was to make the NE592 chip more stable. The NE592 has a bandwidth of 120 megahertz and since a long cable is being driven the chip could oscillate at a high frequency due to the radiated feedback from output to input. A cutoff of 5 megahertz was chosen because it is at least a decade above the highest frequency of signals coming off the tape. This cutoff ensures the filter will have no effect on the data being recovered.

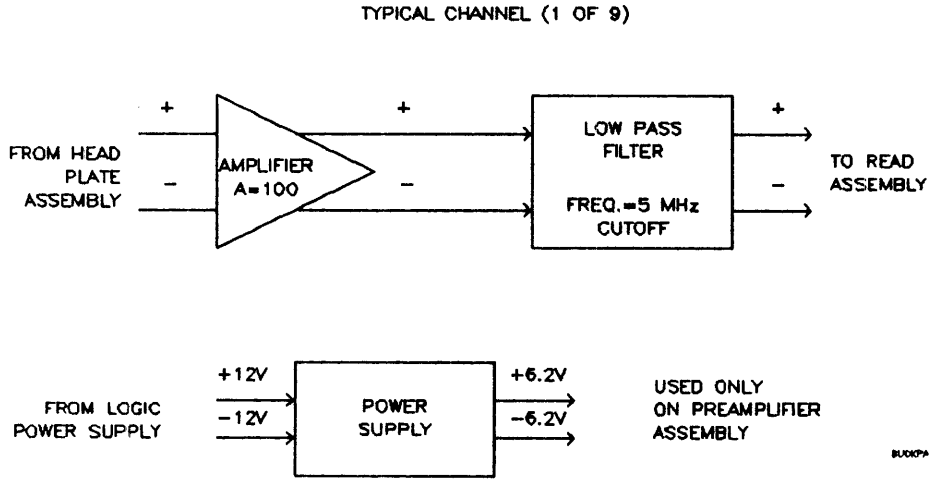


Figure (5) 1-4 Preamplifier Block Diagram

1.7 READ AMPLIFIER

The function of the read amplifier board is to convert the analog signals recovered from the magnetic tape into digital transitions that then can be converted back into real data. The Read Board does this conversion by detecting when any meaningful information is on the tape. This meaningful information is called a block or a record. The read board then creates a digital transition for every time the analog waveform of the detected record reaches a peak. These transitions are sent to another board to be converted into the real data.

The Read Board consists of two main sections, a data path (DP) section and a data path contoller (DPC) section. The main purpose of the DP is to manipulate the waveform coming off the tape and turn it into digital information. The DPC sets up the data path based upon the density of the tape (PE or GCR) and based on previous calibration done on each channel. The DPC section is also used to help calibrate each of the 9 channels.

DATA PATH

The HP 7978A is a nine track tape drive, therefore the data path consists of nine identical channels. Even though each channel is identical they have to be calibrated separately because of the variances in their components. The Master Controller interacts with the DPC to do this calibration. The rest of this section will describe one data path channel with the understanding that there are actually nine of these channels on the Read Board.

This is a self-calibrating drive. The read channel has a variable gain stage to adjust the signals recovered from the tape to a pre-defined amplitude. The varible gain stage also allows the adjustments in amplitude needed for the HP 7978A to switch between the PE and GCR densities.

The input signal to the variable gain stage is the preamp output. The variable gain amplifier consists of a motorola linear integrated circuit (MC1496). The MC1496 is primarily used in balanced modulation and demodulation applications but, because of its transistor structure it can be configured to be a variable gain circuit. The MC1496 is configured to be a differential amplifier with dual output stages. The output stage sums both the inverting and non-inverting sides of the amplifier together. This summation allows the gain to be varied by changing the gain of the inverted or non-inverted side of the output stage. If both sides were turned on equally the gain would be minimum or if one side was turned on all the way with the other side shut off the gain would be maximum. The MC1496 gain is adjusted by using a DAC current source to control the bias of the bases on the output transistors. The variable gain stage is specified to have a gain range of .1 to 8. This range was selected because it will handle all of the channel's gain requirements with plenty of margin. The bessel filter is driven directly with the collectors of the output stage transistors. This setup allows the use of the collector bias resistors as the termination resistors for the bessel filter. The bessel filter is an equal termination 4th order bessel with unity DC gain and a 1dB cuttoff at 450KHz. The cuttoff frequency was selected so it would be high enough not to effect the linear phase of GCR data frequencies (120KHz-333KHz), but low enough to be an effective filter for PE frequencies (60KHz-120KHz).

PEAK AND LEVEL DETECT

The peaks of the analog data need to be converted into digital transitions. The read channel does this conversion by differentiating the waveform so that the peaks of the waveform now cross through zero voltage levels which can be detected using a voltage comparator. The read channel uses a NE592 video amplifier to

do the differentiating. This chip is a differential amplifier that allows you to put a feedback network between the emitters of the amplifier's first gain stage. The capacitor between these terminals makes it a a differentiator.

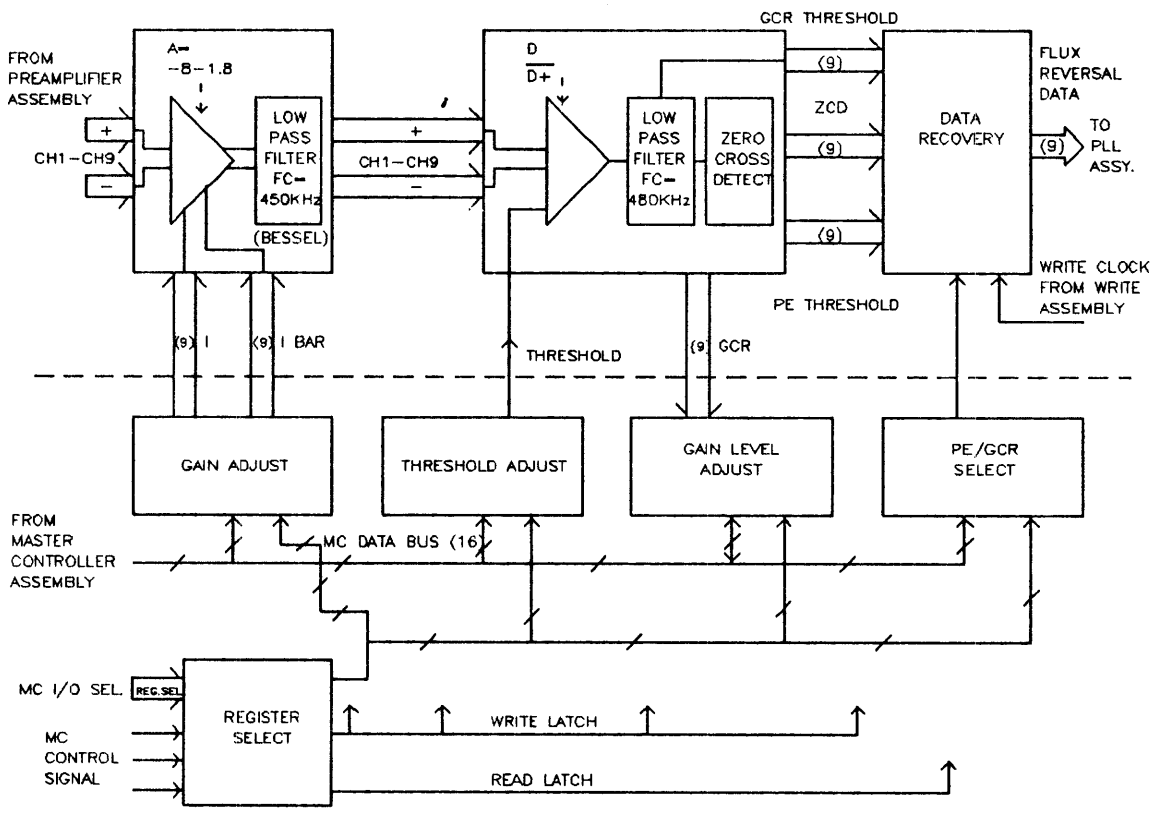


Figure (5) 1-5 Read Assembly Block Diagram

DATA RECOVERY

The data recovery portion of the data path is made up of standard TTL gates that qualify the zero cross detects (ZCD) with the level detects (TDGCR or TDPE). In GCR mode the TDGCR signal is used to detect if a GCR record is on tape, if true then it allows all ZCD data to go through to next board which is the clock recovery board. There is a digital filter which will shut off the ZCD data after the TDGCR signal has gone away for eight bit windows. The eight bit windows are simulated by using the write clock signal to clock a four bit counter. The write clock must be set at the same frequency as the data rate to simulate the bit window size. In PE mode each bit window is qualified for a ZCD by the TDPE signal. If TDPE is low then the data recovery will allow a ZCD to go through to the clock recovery board. The ZCD data that is allowed to go onto the clock recovery board is called flux reversal data (FRD1-FRD9).

DATA PATH CONTROLLER

The data path controller (DPC) is the controlling circuitry that interprets commands from the Master Controller and converts them to signals that control the data path. The DPC's interface to the Master Controller consists of ten write registers and one read register.

REGISTER SELECT

The register select section decodes which of the ten registers the Master Controller wants to write to or if the Master Controller wants to read status. The enable' to the ten write registers is decoded using a four-line-to-ten-line decoder. The four inputs to the are register select lines (RS1-RS4) from the Master Controller bus interface. The write and read latch signals are decoded from the READSEL ,R/W and WS signals coming from the Master Controller.

GAIN ADJUST

The gain adjust section consists of nine identical circuits which control the gain of the variable gain stage in the data path section. Each of the nine circuits consist of a register and digital to analog converter (DAC). The storage register is a octal D-type flip flop and the DAC is a PMI DAC-08. The nine registers make up the write registers one through nine and their inputs are D0-D7 from the Master Controller data bus. The DAC-08's convert the digital data stored in the registers to a current level which controls the gain of the variable gain stage. The DAC-08 has differential current outputs that have been biased so the sum of the two currents is equal to 1mA. The reference current to the DAC-08 is tightly controlled using a voltage regulator (MC1403) which regulates 5 volts to 2.5 volts. The 2.5 volts is then buffered using 3/4 of a LM348 quad operational amplifier. The reason for buffering the reference voltage is because the MC1403 doesn't have the capability to drive all the DAC's reference currents. The 2.5 volts is divided across 2.49K ohm resisters to get a reference current of 1ma.

THRESHOLD ADJUST

The threshold adjust section controls the DC level of the threshold signal to the comparators in the data path. The threshold circuitry contains a stage register, a DAC, an op amp, and an analog buffer. The storage register is part of a pair of registers that make up write register zero. The inputs to write register zero are D0-D15 of the Master Controller data bus. The DAC is uses only the six most significant bits of its input lines (D8-D13) of write register zero. Only six input lines were used because six lines provide enough resolution to generate the different threshold voltages needed. The current bias of the DAC uses the same 2.5 volt reference as the gain adjust section uses, but the current is biased to 2.5mA using a 1K ohm resister. Only the non-inverting current output is used and this current drives 1/4 of a quad op amp which converts the current to a positive voltage with a range of 0 to 2.47 volts. This voltage is then buffered using a voltage follower buffer. The reason the threshold voltage is buffered is because the op amp will sometimes oscillate due to the capacitive load that needs to be driven with the threshold voltage. The voltage follower can drive a much larger capacitive load than the op amp can.

PE, GCR SELECT

The PE, GCR select is a control bit that sets the data path into either GCR or PE mode. The data path uses this bit to control a quad two-to-one mux that switches between the GCR or PE thresholding discussed in the data recovery section. The register used for this control line is bit D15 of write register zero.

GAIN LEVEL DETECT

The gain level detect section is a feedback mechanism for the Master Controller to do an auto-calibration on the data path. The Master Controller controls the gain level detect section along with the gain adjust and threshold adjust sections to do the calibration. The gain level detect circuitry consists of an input register, output register, 8-to-1 digital multiplexer, and a dual JK flip flop. The multiplexer multiplexes the outputs of the comparators that detect the gain level in the data path channels 1 through 8. The multiplexer is controlled by bits D4-D7 of write register zero. The output from the mulitplexer is fed into the clock input of a JK flip flop. The flip flop is a which is configured in a latch and hold mode.

This configuration means that once the flip flop is clocked, the output will change to a high level and stay high until it is cleared externally. Data path channel 9 gain level detect comparator output is fed into the clock of the other flip flop. Both flip flops are configured the same way. The clear inputs of the flip flop are controlled by bit D14 of write register zero. The output register is a quad D-type flip flop with tri-state outputs. Three status bits are put onto the Master Controller data bus during a read from the Read Board. The status bit on D3 of the Master Controller data bus indicates if a gain level has been detected in data path channels 1-8. The status bit on D4 of the Master Controller data bus indicates if a gain level has been detected in data path channel 9. The status bit on D13 of the Master Controller data bus indicates whether the read board is in PE or GCR mode based on bit D15 of write register zero.

MASTER CONTROLLER INTERFACE

The Master Controller interface section is the communication interchange between the Read Board and the Master Controller.

READ BOARD WRITE REGISTERS

REGISTER 0:

D0-D3 *** Not Used

D4-D7 *** Selects Channel for Gain Level Detector

D7	D6	D5	D4	
0	0	0	0	*** Channel 1
0	0	0	1	*** Channel 2
.	.	.	.	
.	.	.	.	
1	0	0	0	*** Channel 9

D8-D13 ** Controls Threshold Voltage Level

D13	D12	D11	D10	D9	D8	
0	0	0	0	0	0	** Thresh = .000V
0	0	0	0	0	1	** Thresh = .039V
.	.	.	.	.	.	
.	.	.	.	.	.	
1	1	1	1	1	1	** Thresh = 2.47V

D14 ***** Enables Gain Level Detectors

D14	
0	**** Resets The Detectors
1	**** Enables The Detectors

D15 ***** Selects GCR/PE Mode

D15	
0	**** GCR mode
1	**** PE mode

REGISTER 1-9: (CONTROLS CHANNELS 1-9 RESPECTIVELY)

D0-D7 *** Controls The Gain Of Channels 1-9

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	*** Gain ~ 8(max)
.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	
1	1	1	1	1	1	1	1	*** Gain ~ .1(min)

READ BOARD READ REGISTER

```
REGISTER 0:

    D0-D2 ***** Not Used

    D3 ******** Gain Detect Status For Channels 1-8
                D3
                 0 *** Gain Level Not Reached
                 1 *** Gain Level Reached

    D4 ******** Gain Detect Status For Channel 9
                D4
                 0 *** Gain Level Not Reached
                 1 *** Gain Level Reached

    D5-D12 **** Not Used

    D13 ******* GCR/PE Mode Status
                D13
                  0 *** Read Board In GCR Mode
                  1 *** Read Board In PE Mode

    D14-D15 *** Not Used
```

1.8 CLOCK RECOVERY

Information received off the tape is made up of transitions with no clocking information except at the beginning and end of the block and at the resync groups. These points provide the initial clock and rechecks to what the clock frequency should be. In between the above mentioned points, information to maintain clocking is obtained from each transition edge.

Because the transition edges occur close to the correct time, the Phase-lock loop is able to recover a clock out of the varying transition spacing. Basically, the PLL then averages the information. The result is a "clocks" for each channel that enables the data to be latched and processed.

The control latch receives information from the Master Controller, such as whether the current operation is in PE or GCR mode, if a loopback (and which one) is being performed, and if a RESET is to be done. The Master Controller must address the latch before the above information is held.

Input select is used during a Loopback 2 procedure. If Loopback 2 is in effect, the Clock Recovery Board receives its nine channels of information from the Write Formatter. If Loopback 2 testing is not being done, the nine channels of information come from the Read Board.

Data is taken from the read channel, generates pulses from that in the pulse generator. The pulse generator feeds the pulses into the phase detector.

The phase detector does a comparison between the pulse data coming in and the clock generated by the VCO. The comparison generates information about whether the clock is ahead or behind the pulse data. In addition, it gives some proportionality information (i.e. how far ahead or behind the data the clock is from the data coming in.

The information of "which direction" and "how much" is fed into the loop filter to take out noise, and then summed into the VCO. The loop filter is a 2-pole filter that rolls off at 45 KHz.

The filtered phase information is summed into the VCO. The VCO uses that control voltage to generate the clock (as the control voltages varies, the clock will vary and, since the loop is closed, it will track the data coming in.

The Divide-by-N network on the output of the VCO divides the VCO frequency by either a value needed for PE or one needed for GCR.

The discriminator (there is one for each of the nine channels) looks at the data coming in on each track and tries to determine when the phase-lock loop is locked and when it has drifted out of lock. When the discriminator sees an "all 1's" pattern, it sets the lock detect signal true. When a gap or dropout is entered (8 clock cycles of no data), lock detect is set low. This indicates that lock *may* have been lost. A switch is not made immediately to the write clock, however. The circuit is allowed to drift and wait for a new lockon. If lockon is not obtained, a gap is assumed and then the switch is made to the write clock to maintain center frequency (or something near it).

The clamp signal is taken away when valid data is seen. Then, instead of the write clock generating what the VCO is following, the VCO follows the data-- and lock detect is again set true.

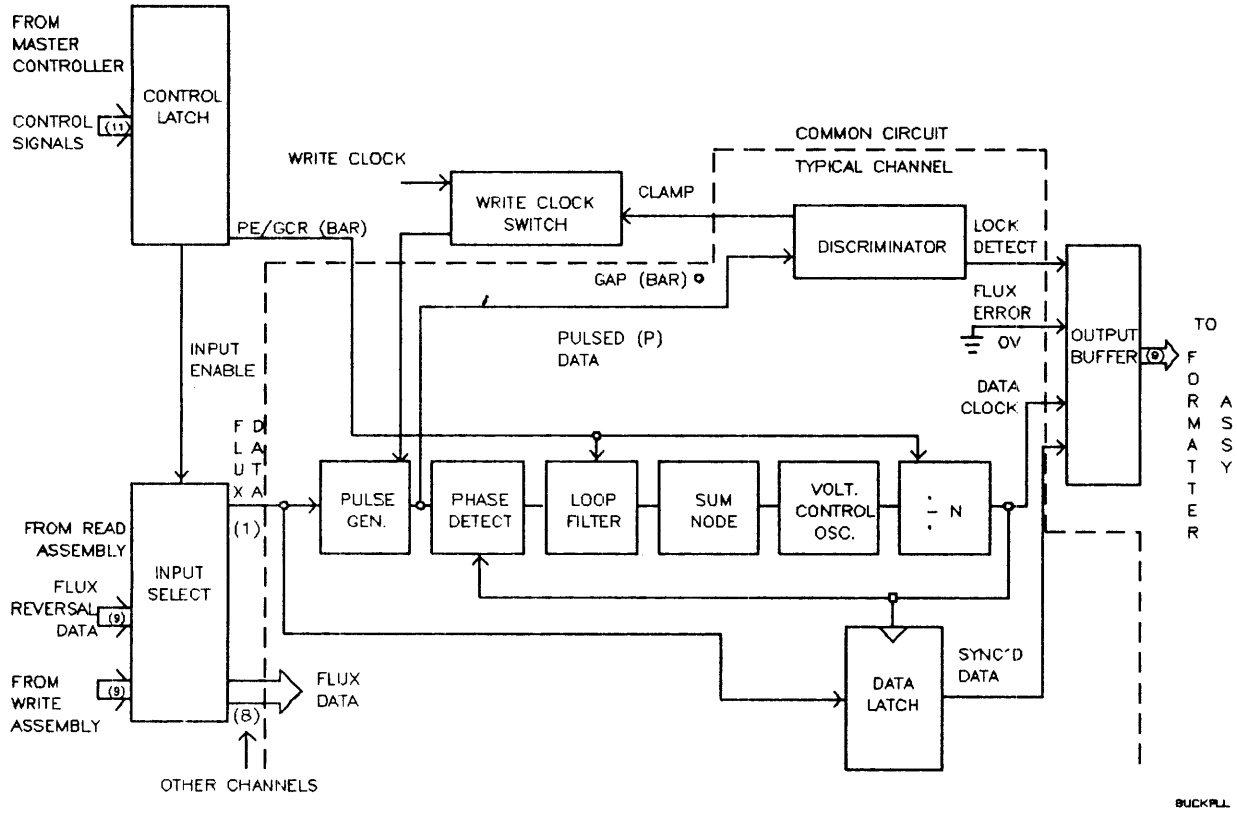


Figure (5) 1-6 Clock Recovery Block Diagram (typical channel)

1.9 DATA DETECT AND DESKEW

The Data Detect and Deskew (DDD) performs the function of translating digital flux reversal information into binary data and re-aligning the tracks to get rid of the skew introduced by the analog channels and mechanical tolerances in the system. The data is sent to the DDD on a trackwise basis; each track independent of the others. Each data bit is accompanied by a flux clock and two error signals. The flux clock is the output of the phase-locked loops in the read channels. The first error signal indicates that the flux data is either out of phase or low in amplitude. The second error bit indicates when the flux clock is not locked on frequency.

The data, clock, and error signals are stored in a FIFO buffer. The data and error signals are clocked into the FIFO using the flux clock, and out of the FIFO using the system clock. The combination of all of the FIFO outputs being ready causes the synchronous section of the DDD to clock out a parallel flux byte.

The magnetic flux byte is used to detect the specific type of block being read. Valid blocks include the density identification blocks, the ARA burst and ID block in GCR, tape marks, data blocks, and interblock gaps (IBG). This information is sent to the Master Controller.

The decode circuitry converts flux bits to data bits according to the tape format specified by the Master Controller. In 6250 cpi GCR encoding format, a flux reversal indicates a "1" and no flux reversal indicates a "0". In the case of 1600 cpi PE, phase encoding is used, in which the data cycle is divided into two windows; a data window and a clock window. Logic levels are determined by the direction of the transition in the data window. Also, a track-in-error signal is generated from the two error signals with the flux bit.

When a data block is detected, the deskew circuitry looks for synchronization fields. Individual tracks are held until all tracks have reached the same point. When all of the tracks are in sync, the DDD sets the sync OK flag, and resumes sending data bytes to the Read Formatter.

1.10 READ FORMATTER

The read formatting function for the HP 7978A tape drive is performed by a two-piece set of LSI and a small amount of support circuitry. The meat of the data path is contained in a custom chip (1RB3-6001) called the Buckhorn Read Chip (BRC). The control for the BRC is contained in a semicustom USM (1RB2-0015) called the Read Formatter Controller (RFC). These two chips together perform the decoding, error correction and error detection for the two data formats-- 6250 cpi GCR and 1600 cpi PE.

The subsystem operates synchronously at 1.5 MHZ. Data is made available to it from the Data Detect and Deskew subsystem in nine-bit parallel format, true data. (That is to say, a '1' is represented by a 5 volt level, a '0' by a 0 volt level.) Data can be input at any frequency up to 1.5 MHZ using a data strobe to indicate valid data. Any falling clock edge surrounded by a high data strobe is interpreted as valid data and is used.

The subsystem operates in several modes. In Idle, the Read Formatter accepts data but does nothing with it. In Verify, the Formatter accepts data, performs any decoding, error correction and error detection possible on the data and logs errors, but does not send data to the Data Buffer. In Read mode, the data is also sent to the Data Buffer after the steps of Verify have been performed.

The capabilities of the Read Formatter are best described in a table. These are based on the inherent power of the codes used for the different formats and the built-in correction and detection capability of each.

RECORDING DENSITY	#TIE POINTERS	#TRACKS IN ERROR	TIE REFRESH	COMMENTS
GCR	0	1	GROUP	
GCR	1	1	GROUP	TIE MUST MATCH ERROR.
GCR	2	1	GROUP	1 TIE MUST MATCH ERROR.
GCR	2	2	GROUP	BOTH TIES MUST MATCH ERROR TRACKS.
PE	1	1	BLOCK	TIE MUST MATCH ERROR.

In addition, GCR gives some post-correction detection to determine the success of the correction. Two detection circuits indicate the correctness of the data. PE has no post-correction error detection.

The Read Formatter is a data path block consisting of two major LSI chips and some interfacing TTL. For the most part, the function of the Read Formatter can be described by giving the function of the BRC, the chip containing the data path circuitry. The BRC has a pipelined architecture, allowing real time processing of data without the high speed circuitry necessary for other implementations. Data is accumulated in a shift register until the required operations have been performed at a relatively low frequency and is then propagated to the next stage of the chip. This introduces a total delay of 46 input data windows through the chip for data. Control outputs will occur at various delays from the inputs that cause them, based on the sequence of processing.

Because of the lack of a hard reset, a special operation is required to set the system to a known state. By setting all the data inputs low and asserting RESET, the subsystem can be assured to be clear by clocking a minimum of 62 clock cycles. This in effect links the storage nodes in the BRC together into a long shift register, and then brute forces all stored data to a low state.

The Master Controller is required to assert RESET only in the following circumstances. First, at power on, the subsystem wakes up in reset mode. It must remain in this mode until the rest of the command register has been configured. Second, if the tape stops in any fashion such that a gap is not recognized by the Data Detect and Deskew and the gap information transferred to the Read Formatter, the formatter must be reset to insure a clean slate for CRC's and other polynomials.

[2] DIGITAL CONTROL SYSTEM

2.1 MASTER CONTROLLER

MASTER CONTROLLER HARDWARE

The Master Controller PCA is actually two boards in one: the Master Controller and the Data Buffer. Their interaction is unique because they use the same clocks and many of the same data bus lines.

In many places in the following discussion, the terms Master Controller and Data Buffer are shortened to MC and DB respectively.

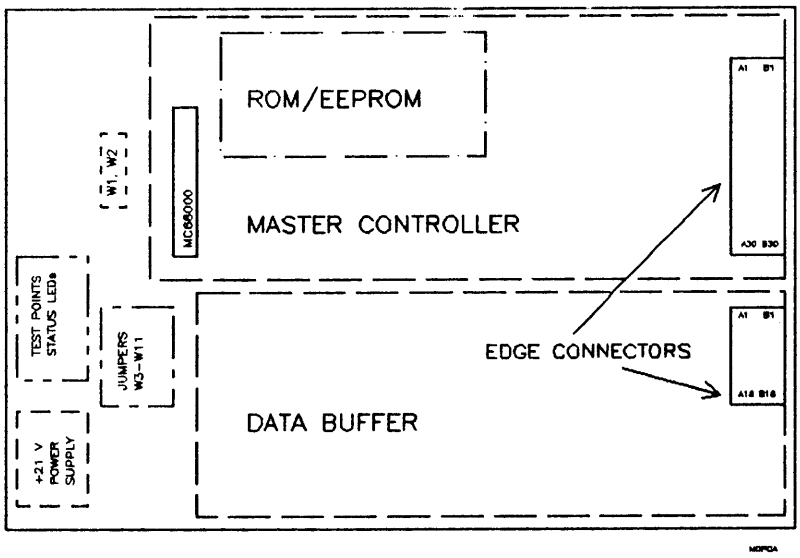


Figure (5) 2-1 Master Controller PCA

MASTER CONTROLLER SUBSECTION

The function of the MC hardware is to execute firmware and coordinate all of the subsystem functions necessary for normal tape operation and running diagnostic procedures. It provides a communication path for commands, status, and control signals between the firmware and the DB, interface, Read Formatter, Write Formatter, Data Detect and Deskew, Front Panel, Servo Controller, Read Board, and Write Board subsystems. Interactions between the MC and subsystems is for the purpose of monitoring status and giving commands as the MC is not involved with the high-speed data path.

Communication between the MC and subsystems is accomplished by means of the MC Data Bus, MC Control Bus and MC I/O Select lines. These signals along with the system clocks form a general purpose data transfer bus allowing the MC to read and write to subsystems as if accessing memory. In addition, because

the 68000 and the DB both use the same 6-MHZ clock, transfers between the MC and the DB are synchronous eliminating possible metastable states.

The MC is implemented as a simple microcomputer consisting of a high performance microprocessor, miscellaneous microprocessor bus control circuits, ROM, RAM, EEPROM, a programmable timer, I/O bus interface circuitry, and system clock generators.

Figure (5) 2-2 is a block diagram of just the MC Section of the board. All of the edge connector signals are actually buffered as they are driven by the MC. A small number of gates are shared between the MC and DB sections. The important sharing is the reading of EEPROM status bits by a DB register.

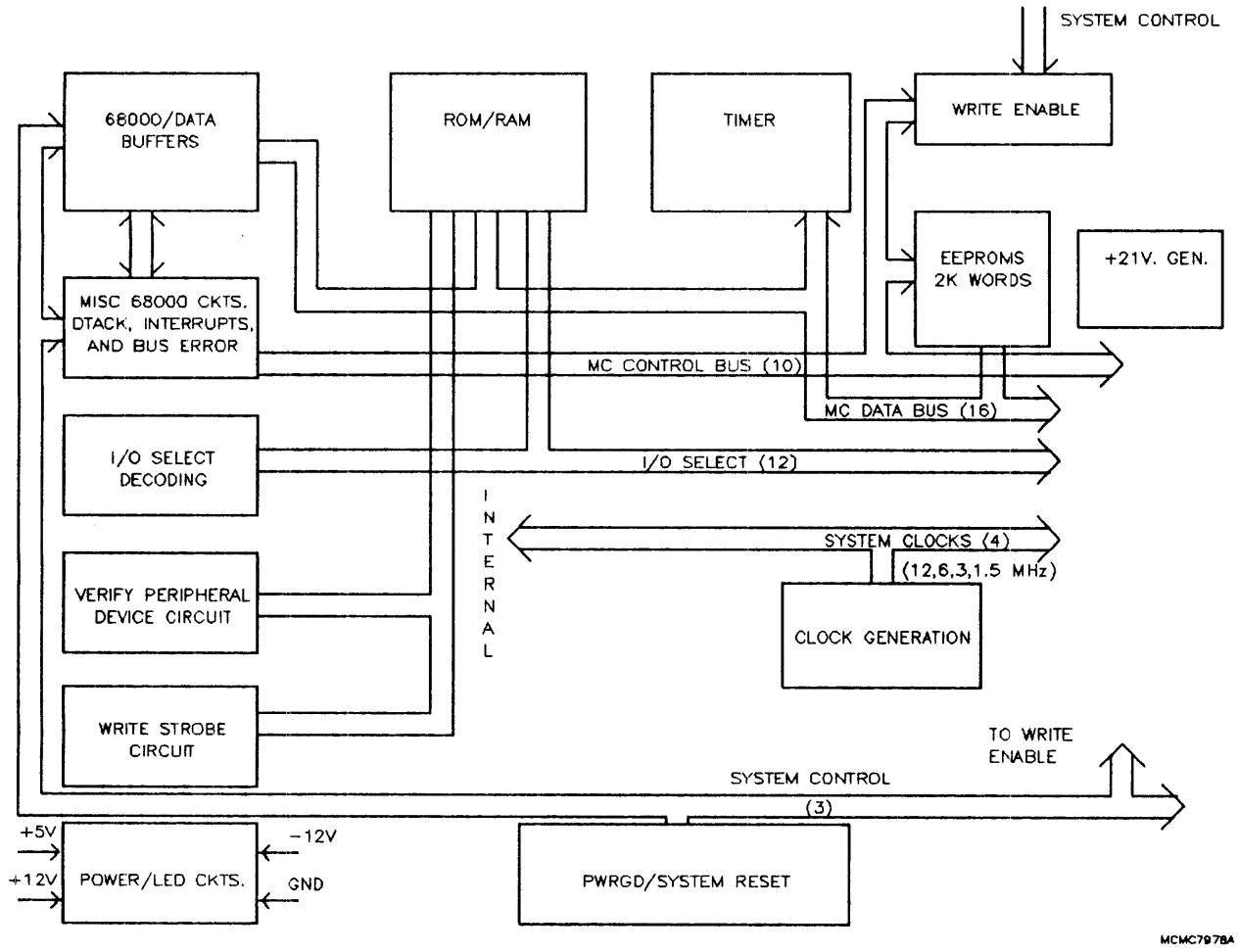


Figure (5) 2-2 Master Controller Block Diagram

MC68000 AND MC DATA BUS BUFFERS

The processor used in the MC runs at 6 MHz in order to use the same clock as the formatter subsystems. This reduces the possibility of metastable states occurring because of asynchronous data transfers between the MC and DB subsystem.

Output drive capability of the MC68000 is sufficient to drive 8 low power schottky (LSTTL) loads from the address bus, and 12 LSTTL loads from the data bus and memory control signals. This eliminates some buffering for signals which do not need to be driven off-board.

MISCELLANEOUS MC68000 CONTROL CIRCUITS

NOTE

An asterisk (*) after a signal name means that the signal is active low. The asterisk is used instead of a bar over the signal name because the superscript bar does not exist in the font used for this manual.

HALT* and RESET* are unique signals on the MC68000 in that they can be driven both by the processor and by external circuitry. When HALT* and RESET* are both driven low by external circuitry the MC68000 performs a complete reset. Whatever program was executing at the time is aborted and the processor begins its power-up procedure. The HALT* line being driven low by the MC68000 indicates that a bus error was detected while the processor was attempting to handle another bus error. The processor will not perform bus cycles while it is driving the HALT* line low. The execution of a RESET instruction by the MC68000 will cause it to drive the RESET* signal low for 128 clock cycles. This allows the firmware to reset hardware and continue execution with the next instruction. RESET going low causes the SYS RST signal to go low, resetting the other boards in the system. Firmware will then set the SYS RST high.

The MC must be able to communicate with two types of subsystems which have very different timing requirements. Subsystems which communicate with the Master Controller by means of a USM must do so only on certain clock edges, while other subsystems can perform transfers asynchronously.

Data transfers between the MC and USM-based subsystems (DB, Write Formatter, Data Detect and Deskew, Read Formatter) and between the MC and the HP-IB Interface will be accomplished by inserting wait states into the processor memory cycle until the subsystem has had enough time to complete the transaction. The MC waits for a handshake line (xx-DTACK*) from the subsystem to be asserted before it completes the bus cycle. Each subsystem has a seperate DTACK* line to the MC. The lines are multiplexed using tri-state buffers so that only the line from the selected subsystem is transmitted to the processor.

Should a subsystem fail to provide a valid DTACK* (data acknowledge) signal within about 25 microseconds, a bus error signal will be generated. This signal causes the processor to begin executing an exception routine which can take appropriate action depending on the circumstances of the failure.

Subsystems which do not use USMs are able to meet the same timing specifications as memory. The MC therefore generates xx-DTACK* for these subsystems just as it does for memory. This ensures that there are no unnecessary wait states inserted into the bus cycle.

Interrupt requests to the MC are prioritized to seven levels by a priority encoder. Several interrupt sources may share levels as necessary to accomodate all devices. There is a vector associated with each level which contains the address of the interrupt handling routine for that level. If several devices share a level the firmware must determine the actual source by polling the devices on that level. The processor is able to generate the proper vector number from the level due to the assertion of VPA during the interrupt acknowledge cycle. Interrupt inputs to the MC controller are connected to pull-up resistors to allow interrupt sources to be wire-ORed on each level.

ROM/RAM CIRCUITS

The memory for the MC currently consists of 128k bytes (64k words) of program memory (ROM), 4k bytes (2k words) of RAM, and 4k bytes (2k words) of EEPROM. The memory chips used may be easily upgraded to higher density parts as these parts become available. A write strobe signal is provided to supply enough data hold time for the EEPROMs.

The memory map shown in Figure (5) 2-3 illustrates the addresses each type of memory responds to. It is possible to use different sized memory devices merely by moving three jumpers on the MC board. For instance, Figure (5) 2-3 is based on jumpers being installed in W6, W7, and W8. This allows memory devices organized as 16k X 1 such as 27128's to be used for program storage. If, however, the jumpers were installed in W3, W4, and W5 the RAM would start at address 10000H, the Data Buffer at 18000H, and the EEPROM at 19000H. This configuration would require devices organized as 8k X 8 such as 2764's to be used as program memory. Jumpers in W9, W10, and W11 would cause RAM to start at 40000H, the Data Buffer at 60000H, and the EEPROM at 61000H. Memory devices organized as 32k X 8 such as 27256's would then need to be used for program memory. Note that the jumpers must all be moved in groups of three and that they have no effect on the size of RAM or EEPROM chips which can be used.

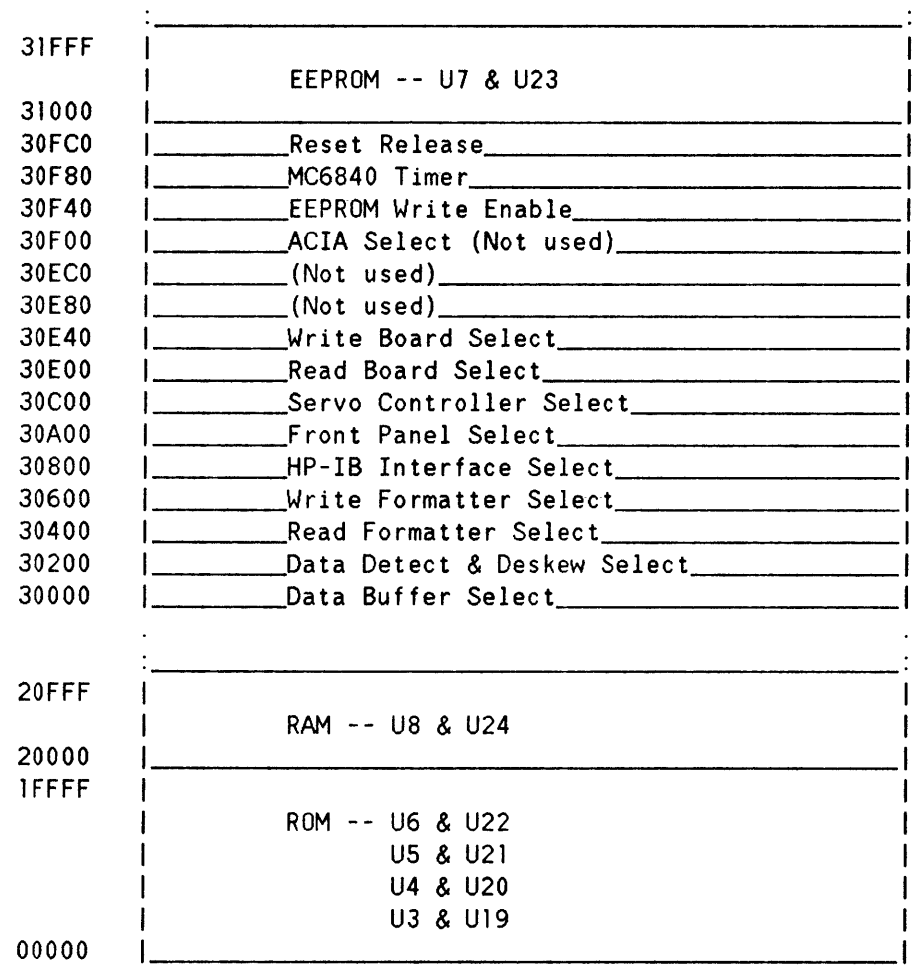


Figure (5) 2-3 Memory Map of MC 68000 Address Space

The RAM, ROM, and EEPROM chips used on the MC must have a read access time from address valid to data valid of 250 nanoseconds or less. In addition, the outputs must be capable of driving at least 2 TTL loads and at least 80 picofarads of capacitive loading.

It is possible to use either EPROM or ROM for program storage. When jumper W2 is installed, pin 1 of each EPROM chip is pulled to Vcc which allows a 128K EPROM to work. When W1 is installed, pin 1 of each ROM chip is tied to address line A15 from the processor which allows a 256K EPROM to work. Obviously, both W1 and W2 should never be installed at the same time or A15 would be connected to Vcc, thus destroying the MC68000.

The memory map of the MC68000 address space assums jumpers W6, W7, and W8 are installed for memory configuration (see Figure (5) 2-3). Each I/O location wraps around within its own address space until the next shown I/O location is reached.

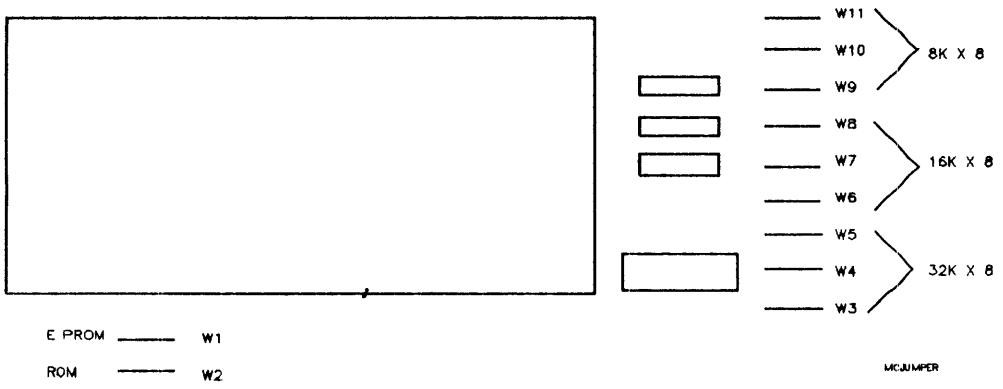


Figure (5) 2-4 Master Controller Memory Configuration Jumpers

The four Register Select lines (RS1-RS4) can be used to decode sixteen unique registers within each I/O address space, but addressing any location more than sixteen beyond the initial I/O address will wrap around and access one of the sixteen registers.

The dotted lines indicate that the addresses between RAM and the Data Buffer Select I/O address also wrap around. Addresses higher than the EEPROM adresses will also wrap around.

EEPROM CIRCUITS

The MC uses two 2k X 8 2817 EEPROMs to create nonvolatile memory for various functions. A brief summary of EEPROM contents follows.

HP-IB bus address
GCR Read Board gain setups
PE Read Board gain setups
Read board setup values (defaults, autogain, density id)
Phase Lock Loop Setup
Write Board gain setups
Write clock setups
Misc values (read retry, gap length, write holdoff,...)
...
Firmware updates and linkage area (about 3.5k bytes of space)
...
Diagnostic Locations (reference values, R/W test cells)
Checksum value

The 2817 EEPROM is considered to be 'intelligent'. This is a fancy word for saying that a read operation for EEPROM is the same as for the ROMs or RAMs but data is 'latched' internal to the EEPROM for write operations and the processor need only check at a later time to verify the Ready/Busy* bit is high (Vih=ready for next write).

+21V Power Generation

NOTE

The +21V regulator circuit discussed below is found only on REV A versions of the 07978-66504 board. Later versions will use the 2817A EEPROM which generates its own programming voltage on the chip itself.

The +21V programming voltage supply for the 2817 EEPROMs is generated from the +12V supply using a TL497AC switching regulator. The worst-case current requirements on the +21V generation circuitry occurs while programming both EEPROMs. Each chip requires a maximum of 15 mA while programming. The power supply can keep the +21 volts within specifications from 0 to 50 mA.

DATA BUFFER SUBSECTION

The Data Buffer is explained in Subsection 1.2.

EDGE CONNECTOR SIGNALS

In discussing the MC board there are really 2 discrete subsystems on the same board, the MC and the Data Buffer (DB), and they share some of the same power and bus sigals. Because of the interconnection between the MC and the DB, and the fact that both generate signals that drive other boards, a third partition was created to describe the signals that are seen external to the board by the rest of the system. The edge connector signals are divided into 9 groups by function. They are as shown in the following table.

NOTE

An asterisk (*) after a signal name means that the signal is active low. The asterisk is used instead of a bar over the signal name because the superscript bar does not exist in the font used for this manual.

1. Power	- +12V, +5V, GND, -12V
2. System Clocks	- 12MHZ, 6MHZ, 3MHZ, 1.5MHZ
3. System Control Lines	- PWRGD, SYS RST, GEN CLEAR
4. MC Data Bus	- D15..D0
5. MC Bus Control Lines	- R/W*, WS*, UDS*, LDS*
	- DDD DTACK*, RF DTACK*, WF DTACK*, IF DTACK*
	- SC INT*, RFA INT*
6. MC I/O Select Lines	- RS4, RS3, RS2, RS1
	- DDD SEL*, RF SEL*, WF SEL*, IF SEL*, SC SEL*, READ BD SEL*, WRITE BD SEL*, FP SEL*
7. DB Data Bus	- DB7..DB0, EOR, PAR
8. DB Transfer Request Lines	- FRRQ*, IRRQ*, FWRQ*, IWRQ*
9. DB R/W Strobe Lines	- FRS*, FWS*, IRS*, IWS*, DBRS*, DBWS*

Subsystems which need to interact with the MC can do so by means of the MC Bus Control lines, MC I/O Lines, and the 16 bit bidirectional MC Data Bus. Synchronization of the MC data bus cycle with subsystems differs depending on whether the subsystem uses the DTACK handshake protocal. The processor talks to the interface board and subsystems using USM's (either 1.5 or 3.0 MHz) by stretching the MC bus cycle until a handshake signal (xx-DTACK*) is received from the subsystem. The bus cycle for other subsystems on the MC data bus is identical to that for a normal memory access.

The following paragraphs describe the signals as seen from the edge connector. For all practical purposes the Data Buffer sees the same signals except that they are connected on board.

POWER SIGNALS

The MC board receives power at +12V, +5V, and -12V. The +5V supply is used to power the digital logic on the board. +12V is used primarily to generate the +21V programming supply for the EEPROMs. The only use for -12V is to provide a backup source of negative substrate bias for the USMs should it ever be needed. All of the above voltages are used to drive LEDs which give a gross indication that there is at least some voltage coming from the power supply.

The worst case power requirement for each of the supply voltages is as follows:

+12V	-	85 mA
+5V	-	6.84 A
GND		----
-12V	-	25 mA

SYSTEM CLOCKS

All of the clocks used in the tape drive are generated on the Master Controller. The clock frequencies used are 12.0 MHz, 6.0 MHz, 3.0 MHz, and 1.5 MHz. These are all derived from the 12.0 MHz signal generated by the crystal oscillator.

A synchronous counter is used to divide the clock frequency to the necessary values. The outputs of the counter are buffered before use. A unique requirement on the clock generation circuitry is that the 6.0, 3.0, and 1.5 MHz clocks must change only on high-to-low transitions of the 12.0 MHz clock.

12MHZ Clock
- Generated by MC clocks
- All synchronous signals within DB are refernced to 12MHZ clock edges
- External timing signal specifications measured with respect to 12MHZ clock edges
- Leading edges of 12MHz must be accurate to within 0.1%
- 6MHZ, 3MHZ, and 1.5MHZ clocks change state on Vih to Vil transitions.

6MHZ Clock
- Generated by MC clocks
- Used by DB in the generation of read and write strobes
- Must be synchronous to 12MHZ
- 6MHZ must toggle not prior to but within 22 nsec of every leading edge of 12MHZ

3MHZ Clock
- Generated by MC clocks
- Used by DB in the generation of read and write strobes
- Defines a full DB transfer cycle
- Clock for the DB LSI control chips
- Must be synchronous to 12MHZ
- 3MHZ must toggle not prior to but within 22 nsec of every second leading edge of 12MHZ (edge where 6MHZ toggles from Vil to Vih)

1.5MHZ Clock
- Generated by MC clocks
- Used by DB to distinguish DB push cycles from DB pop cycles
- DB push cycle (data being transferred from peripheral subsystem to DB) is the 3MHZ clock cycle occurring while 1.5MHZ = Vih.
- DB pop cycle (data being transferred from DB to peripheral subsystem) is the 3MHZ clock cycle occurring while 1.5MHZ = Vil.
- Must be synchronous to 12MHZ
- Must toggle not prior to but within 22 nsec of every forth leading edge of 12MHz.
- 1.5MHZ will toggle only on the leading edges of 12MHZ at which both 6MHZ and 3MHZ toggle from Vil to Vih.

SYSTEM CONTROL LINES

PWRGD Power Good Signal
- Generated by the Boschert power Supply
- If PWRGD=Vil then +5V is out of specification
- If PWRGD=Vih then 4.75V<+5V<5.25V (+5V in tolerance) Implies +12V, -12V are in spec, but no guarantee
- Power up condition; PWRGD=Vil until +5V is in tolerance; No observed glitches
- Power fail warning; PWRGD transitioning from Vih to Vil says +5V is only guaranteed to be in spec for 5msec more.
- TTL compatible for 1 load

SYS RST* System Reset
- Asserted low by MC firmware or PWRGD=Vil
- Allows firmware to reset all hardware subsystems
- Remains @ Vil until firmware toggles it to Vih
- Toggles to Vil following the execution of a RESET instruction by the processor or PWRGD = Vil

GEN CLEAR General Clear
- Generated by the Write Formatter subassembly
- Allows Timer 2 in the MC6840 to count gap lengths

MC DATA BUS

D15 . . . D0 -- These 16 bidirectional lines (buffered from MC circuitry) provide a data path between the subsystems and the MC. Subsystems should restrict loading of this bus to 1 LSTTL input and one tri-state output per subsystem per data bus line.

MC BUS CONTROL LINES

R/W* Read/Write
Vih level on this line indicates the MC needs to read data from the selected subsystem while a Vil level means data for the subsystem will be placed on the data bus.

UDS*, LDS* Upper Data Strobe, Lower Data Strobe
These low-asserted lines indicate that there is or should be valid data on the upper byte, the lower byte, or both bytes of the data bus. During a write operation data is valid on the selected byte of the data bus at both the falling and rising edges of the data strobes. These signals can be used as part of the logic equation to enable bus drivers or latch data, or may be ignored by subsystems which use eight bits or less of the data bus and have no need of the timing information the data strobes provide.

WS* Write Strobe
This low-asserted signal is a combination of R/W*, UDS*, LDS*, and other signals on the MC to create a signal useful for latching data by the various systems into registers. WS* has some very specific timing restrictions so see the detailed discussion in section 4.5.6.

xx-DTACK* Data Acknowledge from I/O Subsystems
These low-asserted signals are handshake lines from subsystems unable to meet the processor bus cycle minimum timing requirements. DTACK is generated by the MC for other subsystems and memory. Subsystems which need to supply DTACK are:
1) DDD DTACK* Data Detect and Deskew DTACK
2) RF DTACK* Read Formatter DTACK
3) WF DTACK* Write Formatter DTACK
4) IF DTACK* Interface DTACK (HP-IB)

SC INT*,IF INT* Interrupts
These low-asserted signals are individual interrupt line for each required subsystem. Only the HP-IB Interface (IF INT*) and the Servo Controller (SC INT*) interrupts come from off-board.

MC I/O SELECT LINES

RS4, RS3, RS2, RS1 Register Select Lines
These four high-asserted signals are address lines from the MC that are buffered. When decoded, they select which register in the subsystem the MC is accessing. Register select lines are stable when the subsystem's XX'SEL* line is asserted low.

xx-SEL* Subsystem Select Lines (I/O Select Lines)
These low-asserted output lines indicate that information on MC data and control buses is stable and is intended for the selected subsystem. Timing diagrams for transactions will be discussed in the MC Section. The subsystem select lines currently defined are:

a) Data Detect and Deskew Select (DDD SEL*)
b) Read Formatter Select (RF SEL*)
c) Write Formatter Select (WF SEL*)
d) Interface Select (IF SEL*)
e) Servo Controller Select (SC SEL*)
f) Read Board Select (READ BD SEL*)
g) Write Board Select (WRITE BOARD SEL*)
h) Front Panel Select (FP SEL*)

DATA BUFFER DATA BUS

DB7..DB0 DB Data Bus -- The DB data bus is a bidirectional, positive-true, 8 bit data bus which is used by all read and write data to move between the HP-IB Interface (IF), the data buffer, and the formatters. DB7 is the most significant bit and DB0 is the least significant bit. This data bus has the capability of transferring 3 Mbytes/sec. Transfer cycles are time multiplexed. DB push cycles (data being transferred from a peripheral subsystem to the DB) occur while 1.5MHz is high. DB pop cycles (data being transferred from the DB to a peripheral subsystem) occur while 1.5MHz is low.

PAR Parity Bit -- PAR is a bidirectional data parity bit signal used as a validity check of the data on the DB data bus. This bit must be set to Vih (high) if there is an even number of 1's in the data byte on DB7..DB0. Likewise, this bit must be set to Vil (low) if there is an odd number of 1's in the data byte. The transmitting subsystem is responsible for sending a correct data parity bit if the data is valid. The receiving subsystem is responsible for detecting parity errors.

EOR End of Record Bit -- The end of record bit is a bidirectional, positive true signal that signifies the last data byte of a data record. This bit must be set to Vil (low) for all data bytes of the data record except the very last byte. This bit must be set to Vih (high only with the last data byte of each record.

DATA BUFFER TRANSFER REQUEST LINES

FRRQ* Formatter Read Request
- DB Input
- Read Formatter Output

IRRQ* Interface Read Request
- DB Input
- Interface Output

A read request signal signifies a request from either the Read Formatter or interface to the DB to transfer one data byte. The data byte will be read from the subsystem and written into the DB.

FWRQ* Formatter Write Request
- DB Input
- Write Formatter Output

IWRQ* Interface Write Request
- DB Input
- Interface Output

A write request signal signifies a request from the Write Formatter or interface to the DB to transfer one data byte. This data byte will be read from the DB and then written to the subsystems.

DATA BUFFER R/W STROBE LINES

FRS* Formatter Read Strobe
- DB Output
- Read Formatter Input

FRS* is sent by the DB to the Read Formatter to acknowledge a FRRQ*.

IRS* Interface Read Strobe
- DB Output
- Interface Input

IRS* is sent by the DB to the interface to acknowledge an IRRQ*.

DBRS* DB Read Strobe
- DB Output
- Interface Input

DBRS* is an extra signal needed by the interface to simplify its design. DBRS* occurs whether or not an actual DB read occurs. However, when data is read from the DB, the DB will use this signal to enable its driving of DB7..DB0.

FWS* Formatter Write Strobe
- DB Output
- Write Formatter Input

FWS* is sent by the DB to the Write Formatter to acknowledge a FWRQ*.

IWS* Interface Write Strobe
- DB Output
- Interface Input

IWS* is sent by the DB to the interface to acknowledge a IWRQ*.

DBWS* DB Write Strobe
- DB Output
- Interface Input

DBWS* is an extra signal needed by the interface to simplify its design. It occurs only to latch in the data off of DB7..DB0.

POWER AND STATUS LED INDICATORS

The eight green LED status indicators at the left edge of the board are used to display the status of certain signals. All eight LEDs should be illuminated

during normal operation. There are eight test points at the left edge of the board which correspond to the eight LEDs. Extreme caution should be exercised when using the test points to check the signals. These test

points are not buffered from the signals in any way and it is very easy to short two or more test points together. This can destroy components on the board and render a working board worthless in no time.

+5V. The +5 volts test point indicates the level of the +5 volt supply for the tape drive. This should be at 5.0 volts +/- 2.0 percent.

+12V. The +12 volts test point indicates the level of the +12 volt supply. This point should be at 12.0 volts +6/-3 percent.

-12V. The -12 volts test point indicates the level of the -12 volt supply of the tape drive. It should be at -12 volts +/- 4 percent.

PWRGD. The PWRGD test point indicates the level of the PWRGD signal from the power supply. PWRGD should normally be at Vih. This signal is buffered between the test point and the LED by several components, so it is not safe to assume that the PWRGD signal is at Vil just because the LED is out.

+21V. The +21V test point indicates the level of the +21 volt supply used to program the EEPROM chips. On REV A boards if the 21 volt supply (generated from +12V supply on the 07978-66504 board) is less than 20.0 volts or greater than 22.0 volts the EEPROM chips could be damaged or it may be impossible for the tape drive to store important data in its nonvolatile memory. REV B and later revisions of the MC PCBs do not use 21 volts for the EEPROMs and so this testpoint and the 21 volt supply circuitry has been removed.

EE RDY. The EE RDY test point indicates whether or not the EEPROMs at U7 and U22 are ready to be accessed. This signal should be a TTL Vih unless the processor is currently writing to the EEPROMs.

SYS RST. The SYS RST test point indicates the state of the SYS RST* signal. This signal is used by the Master Controller to force the hardware in the tape drive to go to a known, reset state. SYS RST* will remain at Vil until the processor accesses an address location to release the reset state, after which it should be at Vih while the processor is executing. On REV A boards the LED is always on but on REV B boards it follows the state of SYS RST*. There are 3 conditions when SYS RST* should equal Vil; 1) at power up, 2) during selftest or diagnostics, and 3) if the firmware detects a condition where it determines hardware is very 'confused' (ie in an indeterminate state) it has the option in an error handling routine to assert SYS RST* to Vil and try to restart the system.

HALT. The HALT test point indicates that the processor thinks it is executing instructions properly. If an instruction is fetched from memory which is completely undecipherable by the processor it will halt itself and pull this line to Vil. Usually this signal is only asserted to Vil in the event of an unrecoverable bus error.

MASTER CONTROLLER FIRMWARE

OPERATING SYSTEM

The responsibilities of the Operating System include scheduling the HP 7978A firmware, allowing the firmware to establish data transfers with the Data Buffer, provide an accurate clock for timing functions, service all interrupts, and manage the shared data structures. The firmware consists of the Channel, Device, and Diagnostic Programs. The word firmware is used in this manual when all three of the programs are implied.

The Scheduler alternates between the Channel and Device Programs with 1.3 milliseconds given to each. The Scheduler is activated whenever a time slice is complete (known via a timer interrupt). A program gives the remainder of its time slice back to the Scheduler, back to the Device Program, or the Operating System is initialized-- depending on the type of interrrupt.

When a program calls an Operating System routine or a diagnostic routine, that routine will temporarily become a part of the program which called it until the routine finishes.

The Data Buffer is a hardware resource used by the firmware. The firmware utilizes the Data Buffer by calling an appropriate Data Buffer utility routine. Each utility routine performs a single task and may require another Data Buffer utility routine to be performed prior to the one being called.

Records handled by the Data Buffer may range from 1 to 16K bytes. The Channel Program may request the Data Buffer to write a data record in bursts to the Interface. This will only be done by the Channel Program when instructed by the Host.

The timing function supported by the Operating System is twofold. A hardware timer is used for short timing functions, and a memory location is updated by the Scheduler from the hardware timer for long timing functions. The hardware timer will run continuously from the initialization of the HP 7978A firmware until either the power is turned off or the Diagnostic Program takes over operation of the drive. The hardware timer completes a cycle once every 873.81 milliseconds. The Scheduler updates the memory location 16 times every cycle, which is once every 54.6 ms. The memory location will have a single cycle of 7.6 years.

All interrupts are serviced by the Operating System. The interrupts are serviced according to the protocol used by the 68000 CPU. The 68000 acknowledges an interrupt by priority level. Priority Level 7 is the highest priority interrupt and it is nonmaskable. When an interrupt occurs, it is serviced if its priority level is greater than the current priority. During the servicing of an interrupt, all priority levels of the same or lesser value are masked. If an interrupt service routine is interrupted by a higher priority interrupt, it will be suspended until the higher priority interrupt's ISR has been completed. Any interrupt which occurs while it is masked will remain pending until the interrupt which masked it has completed processing. The interrupts that are generated are: timer, Servo Controller, Read Formatter, and Data Detect and Deskew.

The Front Panel consists of twelve indicators, a 2-digit hexadecimal display, six buttons, and a door open switch. The displays and buttons are polled by the Channel Program. The Channel routines are also available to the Diagnostic Programs. These routines provide means to change the displays, enable the buttons, and read the status of the buttons.

The shared data structures are used to pass information between the Channel and Device Programs. These structures are the command queue, report queue, and the tape log. The Channel Program reads information in the report queue and the tape log, and writes information into the command queue. The Device Program reads information in the command queue, and writes information into the report queue and the tape log.

The Channel Program handles commands from the Front Panel initiated by an operator, and all communications with the Host through the Interface using the 74/78 protocol. The Device Program interacts with the tape drive hardware to perform tape functions. The third program available in firmware is the Diagnostic Program. Diagnostics will have the capability of using existing firmware routines present in the Channel and Device Programs. This capability requires the calling diagnostic routine to provide the necessary predefined input values to insure the proper operation of the called routine.

Program Scheduler

The Scheduler executes when:

1) The timer interrupt occurs. (The timer is set to a time slice of approximately 1.3 millisecond)
2) The currently running program doesn't need the processor anymore during its time slice
3) The power-on initialization has been completed.

The Scheduler saves the pertinent information about the user program that was running. Since the Channel Program and the Device Program are the only programs that are scheduled, the processor alternates between the two user programs. The Diagnostic Program is never scheduled, but is called by the Channel Program. When a program calls an Operating System routine or a diagnostic routine, that routine temporarily becomes a part of the program which called it until the routine finishes.

Data Buffer

The Data Buffer is a hardware resource which is used by the firmware. The Data Buffer allows the drive to read and write variable-sized data records. Data records are classified into two categories: long records or normal records. Long records are defined as data records whose length exceeds 16 Kbytes. The length of long records is not restricted to the length of the Data Buffer. Normal records that reside in the Data Buffer are the only data records that may be retried. The Data Buffer allows data records to be burst only by the Channel Program. When a data record is burst, the data record is transferred by segments rather than in its entirety. To burst a long record, the segment of the data record that is burst must reside in the Data Buffer and cannot exceed 16 Kbytes. The firmware uses the Data Buffer by calling an appropriate Data Buffer utility routine, each of which will perform a single task.

The Channel Program may request the Data Buffer to write a data record in bursts to the Interface, or to read a data record in bursts from the Interface. A data record that is burst is transferred in segments rather than in its entirety. The Channel Program will only burst a data record when it is requested to do so by the Host during a cold load.

Timing Functions

The timing function that is supported by the Operating System is twofold. A hardware timer is used for short timing functions, and a software clock is maintained by the program Scheduler for long timing functions. A hardware timer is started when the drive is initialized. The hardware timer runs continuously until drive power is turned off or the Diagnostic Program stops it. The hardware timer completes a cycle in 873.81 milliseconds with a resolution of 13.3 microseconds. Once the cycle completes, the hardware timer is automatically restarted. A routine is available for use by the firmware whenever a timing function is being

performed which requires a time less than 873 milliseconds. This routine for short times returns the time in the hardware timer.

The program Scheduler reads the time in the hardware timer to update a software clock. The software clock's resolution is +0.0 milliseconds and -54.6 milliseconds because it is updated by the Scheduler once every 54.6 milliseconds. Since the software clock's resolution is -54.6 milliseconds, it is only used for long timing functions. The software clock runs 7.6 years before completing a cycle.

Both the hardware clock and software clock routines are used together whenever a long timing function is needed that requires greater accuracy than the 54.6 milliseconds allowed by the software clock.

CHANNEL PROGRAM

The Channel Program is responsible for processing all user interactions with the drive. These interactions include interface requests over the HP-IB from the Host, and front panel requests from an operator. During normal operation the Channel Program has full control of the HP-IB interface, the front panel buttons, and the front panel LEDs and display.

HP-IB Interface

The HP-IB interface chip (ABI) and all supporting circuitry are controlled by the Channel Program. All HP-IB interface utilities are resident within the Channel Program. These utilities include: * Getting possible interface requests (includes secondary address commands and data byte commands).

* Sending status type data back to the Host.
* Enabling and disabling data transfers from the interface to the data buffer (write data transfers).
* Enabling and disabling data transfers from the data buffer to the interface (read data transfers).
* Detecting the end of data transfers (including abnormal conditions such as a secondary command received, device clear received, or an operator reset).
* Detecting the device-clear primary commands.
* Setting a parallel poll response for the Host.
* Setting an Amigo identification code in the ABI chip.

Communications with the Device Program

All communications with the Device Program use operating system procedures which manage shared data structures.

Commands --

The Channel Program is responsible for sending commands to the device program. These commands are sent in response to requests over the HP-IB by the Host, or requests from the front panel by the operator. Table 1 gives a list of available commands. All Host and operator commands consist of a single command sent to the Device Program, except for the write record sequence which requires two commands, and during readahead operations where a variable number of commands may be needed to process a Host request.

Reports --

The Channel Program will receive reports from the Device Program. These reports represent success or failure of each command issued. The reports may come from two places. Some reports come from the normal report queue, while others may be taken from a special readahead queue. If the Channel Program wishes to use a readahead report in response to a Host request, it must send the readahead report thru the report queue. If necessary, the Channel Program may have to send internal commands to the device to remove unwanted readahead operations and restore the logical tape position.

To guarantee synchronization of the command and report queues, the Channel Program maintains its own pending command queue which is used to verify that all reports received from the Device Program are in the proper sequence. This verification is done thru the use of transaction-IDs assigned to each command, and returned in each report.

Status --

The Channel Program provides the Device Program the ability to light the door open LED if the Device Program needs to wait on the door. If a Host command is pending, a transparent door open message is also sent to the Host.

The Channel Program also supplies the device with information telling it whether it should perform a write hold off (during immediate reporting of writes).

The Device Program must supply the Channel Program with general status of the drive and the currently mounted reel. This status includes the drive type, the densities available on this drive, whether or not a tape is loaded, and if so whether it is write protected and the current density of the tape.

The Device Program must also supply the Channel Program information on the current tape position. This status includes whether or not the tape is positioned at BOT (load point) or EOF (end of file), and whether or not the tape position is past the EOT (end of tape) marker. It is used in sending idle status to the Host, and the BOT indication is used to update the front panel load point light as well as distinguish between a front panel rewind and unload request.

During readahead operation the Channel Program my update the Tape Status Log when processing a Device Program readahead report.

Exceptions --

The Channel Program has the ability to reset the Device Program using a system reset procedure. This reset is needed when the operator requests a reset, a device clear is received from the Host, or a Host protocol error is detected by the Channel Program. The result of the system reset will be to abort any tape operation, and purge all entries in the command and report queues.

Communications with the Diagnostic Program

The Channel Program will communicate with the diagnostics program to request diagnostic tests, obtain diagnostic results, initiate diagnostic utilities, and obtain status monitoring information.

At power-on the Channel Program will request the results of the power-on self test from diagnostics. Pass or failure status will be shown on the front panel, and the diagnostic results will be available to the Host.

Diagnostic tests can be initiated thru the front panel by the operator, or thru the HP-IB interface by the Host. The diagnostic results are then displayed or made available to the Host.

Diagnostic utilities are also available thru the HP-IB interface. These utilities include downloaded diagnostic tests, remote firmware updating, reading the firmware update code, and reading the status monitoring log and other information.

Host/HP-IB Interactions

The Channel Program is responsible for all communications with the Host over the HP-IB interface. Communications follow the protocol as described in the HP-IB Interface Specifications. The protocol is processed by five separate phases--

-command phase
-report phase
-idle request phase
-cold load phase
-protocol recovery phase.

During normal tape operations the protocol is processed by the command and report phases. The command phase is used to process tape command requests and receive Write Record data from the Host. The report phase is used to send command reports and Read Record data to the Host.

The command phase obtains an optional unit select command from the Host. If a cold load select was issued control is transferred to the cold load phase, otherwise non cold load mode is assumed and the command phase continues. A tape command is now obtained from the Host. The Channel Program determines the queueing status to see whether it should reject the command.

The neccessary commands needed to process the Host request will then be sent to the Device Program. If a Write Record command was received, a special sequence will be entered to process it. This sequence will parallel poll the Host when there is room in the buffer to accept the write data, or to return command reject status.

A Device Specified Jump (DSJ) will be sent to the Host telling it whether or not the write record command was accepted. If the write was accepted the Host can send a Write Execute Secondary command followed by the write data. The Channel Program will set up a data transfer from the interface to the data buffer, send a write record command to the Device Program, wait for termination of the data transfer, and then send status of this write to command queuing procedures.

The report phase is called after a command complete poll response is sent to the Host, and the Host requests its DSJ. The DSJ sent to the Host will be based on the success or failure of the queued command. This information is obtained from the report status provided by the Device Program, and the queuing status kept in the Channel Program's pending command queue.

Following the DSJ, the Host can request to read status, and also read the byte count. This report sequence is then terminated with an END "Complete" type command.

If the report obtained from the Device Program is a send_data_report, a special sequence will be entered to process a read record report phase. A send_data report will be sent by the Device Program only

when valid data is available for a read record request.

The Channel Program sends a good DSJ to the Host indicating that read data is present. The Host can then issue a Read Execute Secondary command. The Channel Program will respond by enabling a data transfer from the data buffer to the interface, and then wait for the transfer to terminate. The Host can send an optional END "Data" command during or after the data transfer, and then optionally request a byte count. The Host should now request the actual report DSJ for the read record command, followed by an optional request for status and or byte count, and then terminate this sequence with an END "Complete" type command.

Interface requests other than a tape command when no commands are queued are referred to as an "idle request". The idle request phase is used to process idle DSJ, status, and end commands, as well as self test transactions and other diagnostic utilities.

The Idle DSJ will be based on whether the protocol is synced and power-on self test has passed. The idle status will be based on the online state, whether a loaded tape is write protected, the current density of the tape, the current tape position status, any active protocol, self test, or firmware error, and whether power has just been restored. Idle end commands allow the Host to enable an online parallel poll. All diagnostics are also initiated while the drive is idle (no commands queued).

The cold load phase is used to process a HP 7970-type cold load sequence. It contains its own command and report phases. Once entered the Channel Program remains in the cold load phase until a non cold load unit select command is received or a protocol error is detected. Since the Channel Program does not return to its top-level between each command, this phase must update the front panel, and check for reset presses.

The cold load sequence consists of processing select cold load, read record, forward space and backspace record and file commands, rewind, and the rewind-offline command. After each command

The protocol recovery phase is entered whenever the protocol is no longer valid. This occurs whenever a protocol or firmware error is detected. The purpose of this phase is to resyncronize the protocol between the Host and the drive. An error message will be shown in the front panel until the protocol becomes synced, or the operator resets the drive.

DEVICE PROGRAM

The Device Program has three major functions:

- -Executing commands sent from the Channel Program
- -Maintain streaming when no commands are present from the Channel Program by performing readaheads on reads and extending gaps on writes.

-React to the following exceptions:

Door open
System reset
EOT
Device Program errors

The Device Program receives commands from the Channel Program and calls the appropriate Device Program and Operating System (OS) modules to execute the commands. After execution, the Device Program sends a report back to the Channel Program indicating the results of the execution.

INTERFACE TO THE CHANNEL PROGRAM

The Device Program communicates with the Channel Program through the OS shared data structures. These inlcude the command queue, the report queue, the readahead queue, and two status logs. Additional flags and control variables inlcude a system reset flag, a door open function, (these are explained under Processing Exceptions), a write holdoff function, and the readahead control variables: readahead mode, and readahead complete flag (these are explained under Maintaining Streaming).

The Channel Program and the Diagnostics Program put commands received from the Host or Front Panel into the command queue. The Device Program then removes the commands from the queue one at a time and performs the required operations.

Valid non-internal commands are:

```
Tape handling dommands:     Load, Rewind, Unload
Read Record command
Tape Move commands
Write commands:             Record, File mark, Gap
Write ID commands:          PE,GCR
Diagnostic command:         On/Off/Auto gain
```

A command may be rejected if the drive is not in the proper state to accept that command. A table of conditions causing a command reject is found in the appendix.

If a command fails, is rejected, or certain unexpected conditions occur, the command queue is prior aborted. The prior abort occurs, by sending the current report to the report queue with the appropriate error set and the beginning purge bit set in the report flags.

The command queue is then cleared by pulling commands from the queue until a Purge Complete command is received. Whenever a write record command is encountered the data is removed from the data buffer as part of the purging process

The status logs are of two types, reel status and tape status. The reel status log contains the current tape density, write enable status, and tape loaded status. Loaded implies that the tape is not only tensioned but that BOT has been found, and the tape is positioned at or beyond that point. The reel status also contains information distinguishing the tape drive as a HP 7978A. It is updated only on load, unload, loss of tension or when a tape ID is written.

The tape log contains BOT, EOF, and EOT flags and is updated as conditions change.

Interface to the Diagnostics

The diagnostic program logs errors and maintains a usage odometer. The Device Program has responsibility in each of these areas. Normal runtime errors are reported to the Channel Program through command reports. The diagnostic program then obtains these from the Channel Program. Firmware errors do not use the report queue but are logged immediatly as they occur, bypassing the OS. The usage odometer is updated each time the tape is unloaded. The update value is obtained from the servo and sent to the diagnostics through the byte count field of the report. Explanation of the diagnostics log and usage odometer is contained in the diagnostic program documentation.

During certain diagnostics tests the diagnostics must access the hardware without the intervention of the Device Program. This privilege is requested and relinquished by sending the internal diagnostics use command to the Device Program.

Interface to the Hardware

The Device Program uses the following Buckhorn hardware subsystems for reading and writing data to the tape:

Write Formatter	(WF)
Write Electronics	(WE)
Read Electroncis	(RE)
Data Detect and Deskew	(DDD)
Read Formatter	(RF)
Servo Controller	(SC)

Read/Write Hardware --

Interfacing with the hardware subsystems is accomplished by writing to and reading from registers on the respective boards. The DDD interrupts the master controller whenever a block is detected, and the RF interrupts upon completion of reading a record. The interrupt service routine stores information concerning the interrupt, qualifying it with whether or not it was expected, and clears the interrupting subsystem. The scheduler is also called to give the Device Program one complete time slice immediately following the ISR.

Whenever the tape is stopped for any reason hardware subsystems are shut down by turning off the write and erase heads, and by setting the DDD and RF into reset mode. The appropriate subsystems are reenabled again when the tape is up to speed and in the proper position.

Servo Controller --

The servo controller is a state machine used to control the tape motion. Interfacing with the servo controller takes place through 16 emulated dual-ported RAM bytes. Desired states and conditions are written into

ram locations. The servo acts on these parameters and performs the necessary operations to reach the desired state.

Positioning information is controlled in a separate servo state machine which maintains the tape position of the end of each block, or any current tape position requested by the Device Program. The position of the previous block is also maint01ned so that it may be returned to during read/write retries.

Because the HP 7978A is a streaming tape drive, whenever the tape comes to a stop it does not stop within the interblock gap, but is positioned by the servo such that it can be brought up to speed and be moving in the proper direction in time.

Tape Command Descriptions

Command: LOAD

The load command assures that the tape is tensioned, finds BOT, and identifies the tape.

The servo controller is initially checked to see if the tape is tensioned. If not it is instructed to tension the tape. In order to read the ID, BOT must be located while moving forward at 73.7 ips. The search is begun by going forward at 73.7 ips until BOT is located or until a timeout corresponding to 30 feet of tape occurs. If the timeout occurs, the tape is stopped and started again in the reverse direction at 250 ips. The reverse search continues until BOT is found or tension is lost. Loss of tension indicates that there was no BOT within the first 30 feet of tape. Once BOT is passed going 250 ips in reverse, the tape is opped and BOT is located again while going 73.7 ips forward.

Identification of the tape is performed after finding BOT while going 73.7 ips forward, by polling the DDD until either a PE or GCR ID is detected and rified or a timeout occurs. If a GCR ID is detected, an ARA burst and an ARA ID must also be detected and verified. If detection or verification is not valid, the ID must be retried. For both PE and GCR the end of ID position is logged by the servo controller. If a 25 foot timeout occurs and nothing was detected by the DDD, the tape is considered blank. If any other block type is detected the ID must be retried.

Retrying the ID involves first finding the BOT again, by looking in reverse to position the tape before BOT then looking forward at 73.7 ips. After the BOT is relocated, the read ID sequence is repeated. If after three retries the identification is not successful, the density is set as unknown and the tape is repositioned about BOT.

Command: REWIND

A rewind command locates BOT then identifies the tape. The tape identification is read so that the tape may be positioned at the end of the ID. Rewind is only issued when the drive is beyond the BOT marker. BOT is located by moving the tape at -250 ips and polling the servo controller for BOT. Polling is begun as soon as the tape is up to -75 ips so as not to miss the BOT during the long ramp up to -250 ips. Once BOT is passed in reverse, the tape is stopped and BOT is located again while going the current read speed.

The identification process is the same as for the load command, except that if the result of the process does not agree with the density currently set, the identification has failed and the density is set to unknown.

Command: UNLOAD

This command instructs the program to move the tape in the reverse direction until tension is lost. It is only issued when the device is at or before the load point.

Command: READ RECORD

The read record command instructs the Device Program to read one record from the tape and to place it in the data buffer.

The read mode parameter in the command indicates the type of mode that the Device Program should operate in when the read is completed. "Stream" indicates that readaheads should be performed. "Single_step/Remove_readaheads" indicate that another command must be received before another read can be begun. In this mode streaming will only be maintained if commands are queued.

If the tape is moving (streaming or reading ahead), the read is started without checking the data buffer for room. Should a data overrun occur, the read will need to be tried again, so the tape is stopped and repositioned. Once stopped the read will not begin until 16k bytes of buffer space is available.

Whenever the tape is moving, the DDD is left on continuously to catch all blocks on the tape, whenever the Device Program is ready for a DDD interrupt to occur it sets up a DDD wait state. Any interrupt that occurs before the wait state is considered a DDD surprise. Once moving, first the DDD, and then the RF are polled for the result of the read.

Possible conditions and corresponding actions are as follows:

DDD	RF	ACTION
Data	EOD no errors	report with no errors
	EOD corrected	report with corrected error flag set
	no EOD, or uncorrected	retry
DDD surprise	NA	stop tape and restart
Tape Mark	NA	report TM, no retry
Other Types	NA	retry
No detect (in 25 feet)	NA	report tape runaway, stop the tape

A block is retried by repositioning back to the last servo position, which would be the end of the previous block or 12" whichever is shorter, and repeating the read sequence. A call must also be made to the OS to setup the usage counter and push pointer again. After seven retries are attempted the command is considered to have failed and the tape is repositioned around the end of the block.

After the read (including all retries), the result of the read operation is sent to the report queue.

Move commands

Move record commands instruct the Device Program to space over a single block without sending data to the data buffer. Move file commands instruct the Device Program to continue spacing over blocks on the tape until a file mark is spaced over.

The move commands do not use the RF. Only the DDD is used for block identification.

Forward moves require first that the tape be positioned such that it can be up to speed within the gap in the forward direction. The possible conditions and actions are:

DDD	RECORD	FILE
Data/Unknown	report no errors	continue
DDD surprise	stop tape and restart	stop tape and restart
TM	report TM	report no errors
No detect	report tape runnaway, and stop the tape	

Backward moves require first that the tape be positioned such that it can be up to speed within the gap in the reverse direction. The possible conditions and actions are:

DDD	RECORD	FILE
Data/Unknown	report no errors	continue
DDD surprise	NA	stop tape and try again
TM	report TM	report no errors
ID	report error and BOT (if detected)	
No detect	report tape runaway error, and stop the tape	

Retries on moves occur up to three times. After the final retry the tape is repositioned after the bad block. After the move (including all retries), the result of the operation is sent to the report queue.

Write Commands

The write commands instruct the Device Program to write a record of data, a tape mark, or to write a gap by erasing 3.5 inches of tape.

The write record command is received in two parts, write_record_setup, indicating that a write record has been requested, and write_record_full indicating that the entire record is in the data buffer. If streaming the write will begin as soon as a write_record_setup is received in an attempt to maintain streaming. If a data underrun occurs indicating that the entire record has not yet arrived, the tape is stopped and repositioned to wait for the write record full command. If stopped, the write will not begin until write_record_full is received.

For each of the write commands the erase head must either be on or must be turned on during the gap following the previous block. This implies that streamed writes may continue streaming, while any other condition will require that the tape be stopped, repositioned and started again so that the erase head can be turned on as it passes through the gap. If a tape mark or data is being written the write head is turned on when it is in the proper position and the WF is instructed to begin writing the proper pattern to the tape.

Verification of the write process is performed by the read electronics. Responses that expected are as follows:

BLOCK TYPE	DDD RESPONSE	RF RESPONSE
Gap	no detection for 3.5"	NA
Tape Mark	verified tape mark	NA
Data	Data with all tracks synced	End Of Record (EOR) detected, with no corrected or uncorrected errors

If a write is not successful, it must be retried by stopping the tape, repositioning back around the end of the previous block and going through the complete write process again. For a retry write record the data buffer usage counter and pop pointer must be set up again by a call to the OS.

Gaps are retried up to three times. Tape marks and data are retried up to three times at the current location, then if still unsuccessful, up to 15 write skips are performed. A write skip involves retrying the write after erasing 3.5 inches of tape. After the last retry the last block written is left on the tape and if it had errors the tape is positioned at the end of the block.

After the write (including all retries), the result of the write operation is placed in the report queue. Only one report is sent for each record written even though the write record instruction comes as two separate commands. If tension was lost during the write, the write and erase heads are turned off.

Write ID Commands --

The write ID commands instruct the Device Program to write an ANSI PE or GCR ID onto the tape.

The tape is repositioned far enough back that the tape can be brought up to speed and the erase and write heads turned on before reaching BOT. After the BOT is located, the proper ID is written to the tape and is verified by the DDD. If the command is a write_GCR, an ANSI ARA burst and ARA ID is also written and verified.

When errors occur anywhere in the ID the entire sequence must be retried, with up to three retries. If all of the retries are unsuccessful the tape is repositioned back around BOT.

After the write (including all retries), the result of the write operation is placed in the report queue.

Auto Gain Command --

The auto gain command is received from the diagnostics program after a Front Panel request. This command determines and saves new gain values for the read electronics. Initially an all ones pattern is written to the tape, then the tape is rewound and the pattern is read, varying the gain values for each track until the proper values are determined. The gain values are then written to the EEPROM to be accessed whenever the electronics are to be set up for a read. This process is repeated twice once at 73.7 ips for GCR, then again at 75 ips for PE.

The auto gain command requires that the tape be positioned initially at the load point and uses the first 28 feet of tape. The first three feet are erased, the next 25 feet receive the all ones patterns.

MAINTAINING STREAMING

The HP 7978A is a streaming tape drive and requires a relatively long period of time to stop, reposition, and start the tape again. The longer the tape can remain moving, the higher the throughput will be. Whenever the command queue is empty and the tape is moving an attempt is made to maintain streaming. If the previous command was a read or a forward move, a readahead is performed. If the previous command was a backward move, a backward moveahead is performed. If the previous command was a write the gap is extended.

Readaheads and Backward Moveaheads

Readaheads/backward moveaheads involve continuing to read blocks from the tape the same as with a normal reads and moves, placing read data in the data buffer, but placing the reports in the readahead queue rather than the report queue.

Whenever a read or move command is received from the channel program with the read mode parameter set to "stream", the device sets readahead mode in the OS to readahead or move backwards, and the readahead complete flag to false. This indicates to the Channel Program that the Device Program will be entering a readahead mode. After the current command is completed and placed in the report queue, readaheads/backward moveaheads are begun with the reports being placed in the readahead queue. The

drive continues to operate in a readahead mode with the channel obtaining all reports from the readahead queue until one of the following occurs:

- A command is received from the Channel Program. (the command queue is checked between readaheads to see if the Host has issued a command which cannot be met with the current readahead)
- The data buffer is filled.
- The readahead queue is filled.
- A readahead fails (no retries are attempted since the streaming is broken anyway).
- An exception requiring stopping the tape occurs
- A block of data is not detected within 20 inches.
- Any read error occurs during a readahead

When a condition occurs which requires readaheads to be stopped, the tape is positioned after the last successful read, and the readahead complete flag in the OS is set to true indicating to the Channel Program that no more reports will be placed in the readahead queue.

The Channel Program then sets the readahead mode back to not streaming when it acknowledges that the readahead is complete. Depending upon the command received from the Host, the Channel Program may need to purge the readahead queue and have the tape moved back to it's location prior to readaheads. To do this the channel sends commands to the Device Program to back up over those records. This is done with the read mode parameter set to "remove readahead" to prevent overshooting.

The tape status and reel status logs are updated by the Channel Program as reports are pulled from the readahead queue.

Gap Extend

After the completion of any write command, if there is no command pending, a gap timer is started. The Device Program waits until either a command is received or the gap has been extended to a length which is set in EEPROM. If the timeout occurs, the tape is repositioned around the end of the last written block.

Write Holdoff

Although more related to drive wear than to performance, the write holdoff function aids in avoiding excessive tape repositioning by delaying the execution of immediate reported writes several records can be written at once.

When a write command is received, the Channel Program sets the write holdoff variable is the OS, and leaves it set until one of the following occur:

- The command queue is filled.
- Two sequential tape marks occur (end of reel).
- A non write command is queued.

The Device program in turn will not take a command out of the command queue until one of the following occurs:

- The OS write holdoff variable is cleared
- The data buffer has less than 16K of free space left.
- A timeout of 5 seconds occurs. (The actual timeout value is contained in the EEPROM)

If the drive is not in immediate report mode write commands are executed as they are received, without delay.

If any command is being executed such that the tape is moving when a write is received, the write command is executed immediatly.

PROCESSING EXCEPTIONS

Door Open

Whenever the door is opened, Buckhorn must come to a complete stop within one second to ensure operator safety. Certain operations are of short duration and can be completed and the tape stopped within the alotted time. Once one of these commands are started they will be allowed to finish before the tape is stopped. These are:

- Reads and Readaheads (once a block has been detected)
- Writes
- Record moves (once a block has been detected)

Commands of long duration are suspended by stopping the tape. Motion is resumed when the door is closed by repositioning back to the last known state and continuing after the appropriate setups are made. Readaheads are not resumed. These commands include:

- Load
- Rewind
- Unload
- Reads and Readaheads (before a block is detected)
- Record moves (before a block is detected)
- File moves

All commands wait until the door is closed before beginning.

System Reset

Whenever the system reset flag is set, the Device Program must abort any command in progress by stopping the tape, and purging the command queue. The queue is purged by removing commands until the queue is empty. None of the commands including the current command are reported on. The system reset flag is then cleared acknowledging to the Channel Program that the reset has been complied with.

EOT

The servo is checked after each command to see if the tape is beyond the End-of-Tape mark. If so the tape status log and report flag is set to indicate End-of-Tape.

Beyond EOT is also checked while waiting for a block detect in a read record. If it occurs the timeout length is reduced from 25 feet to 6 feet.

DEVICE PROGRAM ERRORS

Errors may be data errors, hardware errors or firmware errors. Data errors involve the inability to detect or recover data properly. These are retried according to the retry mechanism explained within this document for each command. Hardware errors can come from the formatters or the servo controller. Whenever hardware errors occur the operation is terminated. Data and hardware errors are reported to the Channel Program through the report queue being tied to the report of the command in which the error occurred. Firmware errors are not sent through the report queue but are reported immediately to the Channel Program bypassing the OS.

DIAGNOSTIC PROGRAMS

Built-in Diagnostic Overview

The HP 7978A's built-in diagnostics are grouped as Power-on self test and Operator/Host requested diagnostics. The power-on self test covers the Master Controller assembly, HP-IB assembly, the HP 7978A's digital data path, Servo Controller assembly, and partial testing of the BOT/EOT sensor, and speed encoder loop. Power-on self test has the goals: cover as much of the drive without tensioning tape (70-75% of the HP 7978A tested) and perform the testing in less than 30 seconds. Operator/Host requested diagnostics are initiated by an Operator from the HP 7978A's front panel or by a Host from the HP-IB. The diagnostics which are requested from an Operator or Host are grouped into utility and test diagnostics. A utility diagnostic returns status, performs a function (update EEPROM, set auto gain values), or changes the environment in which a diagnostic test is executed. A diagnostic test will perform a set of tasks involving the HP 7978A's hardware attempting to detect and isolate a failure. The goal of the HP 7978A's built-in diagnostics is to detect a failure 99% of the time, and correctly isolate 95% of the time the failure to at most three field replaceable units (FRU).

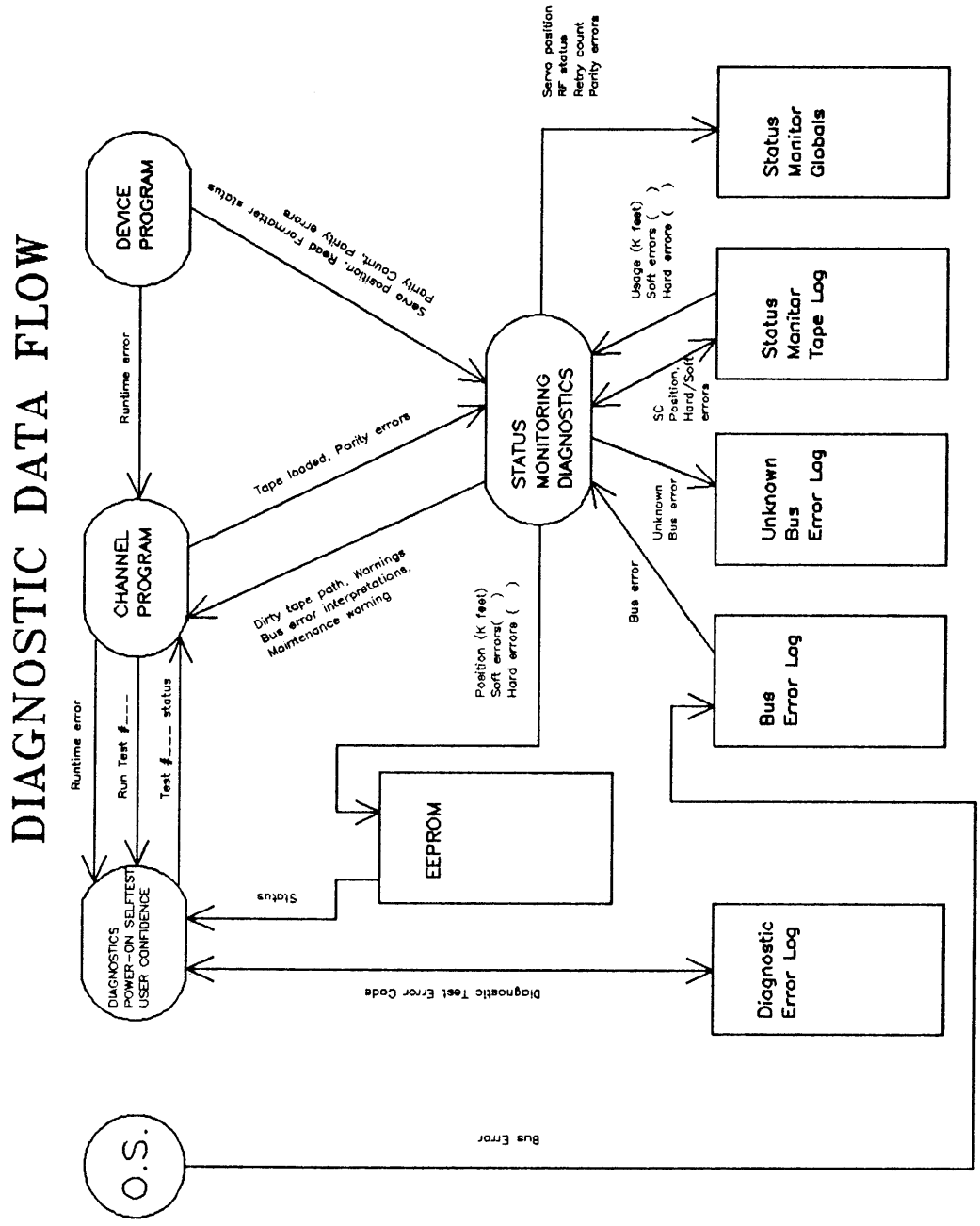


Figure (5) 2-5 Diagnostic Data Flow

Diagnostic External Interface

The HP 7978A's diagnostics are accessed through the HP-IB and Front Panel. The HP-IB is used by the Host, while the front panel is a keyboard used by an Operator. The Host requests a diagnostic by sending a diagnostic test number to the HP 7978A. The appropriate test is executed and the error message is returned to the Host. The Host may also request some special diagnostics through secondary protocol commands.

An Operator requests a diagnostic from the HP 7978A's front panel. An error message is displayed on the front panel upon completion of the diagnostic, if an error exists. When a diagnostic fails, the error message will be displayed on the front panel until the Operator presses the RESET button. Once the RESET button has been pressed, the front panel will reflect the HP 7978A's status prior to execution of the diagnostic.

Bus Error Handling

A Bus Error will occur whenever the Master Controller accesses certain subsystems which do not respond within an allowable amount of time. Since the Bus Error can occur right in the middle of a CPU instruction, it is not possible to return to the correct program location following a Bus Error. Rather than take the chance of allowing the Master Controller to execute unpredictably, the HP 7978A will be shut down following a Bus Error. An error code will be displayed on the front panel indicating the FRU the Master Controller was attempting to access when the Bus Error occurred. The power will have to be cycled in order to restart the drive.

Unexpected Exception Handling

The MC68000 CPU is capable of responding to a number of unexpected conditions which should never occur in the HP 7978A. Should one of these conditions be detected by the CPU a hardware or firmware failure is indicated. The HP 7978A will respond to these unexpected exceptions by displaying an error code indicating which exception occurred and shutting down as with a Bus Error.

Excessive Soft Error Rate Warning

The excessive soft error rate warning is displayed on the Front Panel when the error threshold has been met or surpassed. The error threshold used will be large enough to prevent a warning from occurring for acceptable soft error rates. The soft error rate is computed, using a command count and the retry count for the currently loaded tape, after each command is processed. The warning message is cleared from the front panel when the error rate declines below the error threshold, or a load command is executed. If, at the time of unloading the tape, the error rate equals or exceeds the maximum number of errors allowed on a tape the dirty tape path warning message will be displayed. The dirty tape path warning message will be displayed until the RESET button is pressed or a tape is loaded.

Tape Usage Odometer

The amount of tape that passed over the head is recorded dynamically in RAM and statically in EEPROM. The RAM based odometer is updated after every unload tape command. The odometer in RAM is measured in increments of .823 inches and is supplied by the Servo Controller. Once the RAM odometer reaches 20,000 feet of tape, which is about four reels of 2400 foot tape, the EEPROM odometer is increased by one. The tape usage odometer was made available for the customer engineer to help monitor head wear for service contract usage pricing.

Diagnostic Logs

The built-in diagnostics use two logs: the diagnostic error message log and the data error log. The diagnostic error message log contains the ten most recent failed diagnostic test error messages and the time, relative to Power-on initialization, that the error message was logged.

The data error log is used by diagnostics to compute the excessive error rate warning message. A new entry is used whenever a load command is executed. This is a twenty entries deep cyclic log which contains:

The time that this tape was loaded.
(The time value used is in 54.58 ms increments from when the drive was powered up.)

Hard error count.

Soft error count.

Number of reportable commands since the tape was loaded.

This log is only available to the Host via an image dump.

Individual Diagnostic Descriptions

Following is a list of each diagnostic and what it does. The term "local access" will be used when the Front Panel interface is used to access a diagnostic, while the term "remote access" will be used to designate Host access to the diagnostic via the HP-IB Interface. If neither of these terms are used, the diagnostic is available from both interfaces. The term "secondary" will mean that a secondary interface protocol command is needed to request the diagnostic. A "utility" diagnostic returns status, performs a function, or changes the environment in which a diagnostic test is executed. A "test" diagnostic will perform a set of tasks involving the HP 7978A's hardware attempting to detect and isolate a failure. If a diagnostic can be executed multiple times before returning the result of the diagnostic, the term "looping" will be used. The tape tests will reposition after each data block unless the diagnostic environment is set to "walk" down the tape. The term "Walking" will be used to indicate the walking capability. Tape position is considered lost after executing tests 35 through 59. All servo related tests require the drive to be offline. The tape diagnostics (tests 21, 22, 33 and 34) require the drive to be online when requested by a Host.

Test 0 -- Display the most recent diagnostic error message. Local access, Utility.

Test 1 -- Display the HP 7978A's diagnostic error message log. The most recently logged error will be displayed first. Subsequent entries will be displayed each time the Enter button is pressed until all errors in the log have been displayed. Local access, Utility.

Test 2 -- Clear the diagnostic error log and set the diagnostic environment to the default values of single execution and reposition of tape tests. Utility.

Test 3 -- Power-on self test failure override. This diagnostic will clear the command rejected status after a power-on self test failure occurs. Utility.

Test 4 -- This test will run the power-on self test in its entirety. (Tests 5 and 57). Test, Looping.

Test 5 -- The Master Controller Power-on self test, which is always performed at power-on, calls tests 6, 2, 7, 10, 11, 13, 14, 12 , 15 and 16. The RESET button may be pressed at anytime to abort the test sequence upon completion of the current test. When the RESET button is pressed during the power-on self test, pressing the rewind button is required to abort the test. Note: Tests 41 through 44 are performed at power-on but not as part of this portion of the power-on self test. Test, Looping.

Test 6 -- The kernal Master Controller tests verify the MC68000 CPU registers, addressing modes, and that the checksum for the Master Controller ROM is correct. It also calls tests 8 and 9 to check the RAM and timers. This test will not affect current HP 7978A status. Test, Looping.

Test 7 -- The front panel LED's are lit and extinguished one at a time, followed by rotating 00H, 11H, ..., FFH on the two digit hexadecimal display. This utility will leave all the LED's lit. Local access; however the Host has indirect access to this utility by requesting the Power-on self test. Utility.

Test 8 -- The RAM walking bit tests will cover the entire Master Controller RAM. A walking one test is performed on a pattern of zeroes followed by a walking zero on a pattern of ones. The RAM will be tested a single byte at a time. The data in the byte being tested is saved prior to testing and is restored upon completion of the test. Test, Looping.

Test 9 -- The three timers in the MC6840 PTM chip on the Master Controller are verified that they count down to zero and provide the correct status. Test, Looping.

Test 10 -- The EEPROM chips on the Master Controller are verified to be correct by reading some predefined addresses containing constant values, and performing a checksum. Test, Looping.

Test 11 -- This test will verify the Data Buffer's functionality and perform a marching RAM test on the Data Buffer's static RAM. A background pattern of 000H is written with verify from the lowest Data Buffer address to the highest Data Buffer address. The marching RAM test will then write with verify 3FFH from the lowest Data Buffer address to the highest Data Buffer address. Once at the highest address, the pattern is changed to 000H and descends to the lower address verifying what was written as it descends. Test, Looping.

Test 12 -- The Write Clock on the Write Electronics assembly is verified by setting it to run at PE and GCR frequencies. The Write Clock will be returned to the data rate of the currently loaded tape's density upon completion of this test. Test, Looping.

Test 13 -- The HP-IB internal loopback verifies that the FIFOs and the status' are correct. Host commands will be ignored during testing. Test, Looping.

Test 14 -- Data is looped from the HP-IB to the Data Buffer and back to the HP-IB. This test will verify the HP-IB/Master Controller interface. Host commands will be ignored during testing. Test, Looping.

Test 15 -- The digital loopback will test the Master Controller, Formatter, Phase Locked Loop and the Write Electronic assemblies. GCR and PE ID's, gaps, tape marks and data records are written (digitally) and verified during this test. The data used for the data records is: 0H, 1H, ..., FFH, 0H, ... The loopback data is sent from the Data Buffer through the Write Formatter to the Phase Locked Loop, through Data Detect and Deskew, into the Read Formatter and back into the Data Buffer. The data is checked for correctness upon reentry into the Data Buffer. Several tests are run to verify each density operates properly and that Formatter and Data Buffer error conditions can be detected. Whenever a failure is detected a loopback is performed without the Phase Locked Loop assembly. If this test passes, the Phase Locked Loop is reported to be the failure. Test, Looping.

Test 16 -- The Read Board test will toggle a bit on the read board to determine if it is present. Test, Looping.

Test 17 -- Non-existent test.

Test 18 -- Non-existent test.

Test 19 -- The worst case data patterns are written into a test word in EEPROM. By writing these patterns, a stuck bit (having a value of zero) will be found indicating the cells are saturated (worn), an internal address line is not working, or +21 volts is not available to the EEPROM chips. This test can be executed a minimum of 20,000 times, using two words for testing, before EEPROM cell wearout may occur. Test.

Test 20 -- This test will allow the user to press any button and have a code from 1-7 displayed on the front panel display. The uppermost button when pressed will display a '1', while the lowest button will display a '6' when pressed. When the door is opened a '7' will be displayed. This test requires pressing two or more buttons at once to exit. Local access, Utility.

Test 21 -- A single PE data record is written. A fixed data record will be created using binary data from 0 to 255. The data will be written with verify. This test will be considered 'failed' if any retries are necessary to write the data record or a hard error occurs. A scratch tape must be used for this test, otherwise any and all data may be unrecoverable on an application tape. If the loaded tape is not identified as PE a PE tape ID will be written. The drive must be online for remote access. Test, Looping, Walking.

Test 22 -- A single GCR data record is written. This test is identical to test 21, except the test pattern is the seven byte worst case pattern: 4, 32, 152, 188, 32, 4, 188, 0 and a GCR ID is written if the tape loaded is not identified as GCR. Test, Looping, Walking.

Test 23 -- Non-existent test.

Test 24 -- The default auto gain values are recomputed by creating a gains tape by writing to a scratch tape and reading the tape to adjust the gain values. Load a scratch tape on the drive. Enter the diagnostic test number and password. The password is: press the rewind button, press the RESET button, finally press the address button. The gains will now be computed. When the door is opened or the RESET button is pressed, the auto-gain utility will be terminated. After the gain values for each of the densities are computed, the tape will stop and display the gain average. The pass/fail led will indicate further information is logged in the diagnostic error message log when failure (red) is lit. Local access, Utility.

Test 25 -- This utility will set the local looping environment to single test execution. Remotely requested diagnostic tests and utility diagnostics are defaulted to single execution. Local access, Utility.

Test 26 -- This utility will set the local looping environment to infinite execution. The RESET button must be pressed and held to exit a test in the looping environment. The display will indicate the number of times (in hex) a test has been run. When the executing test first fails, the red pass/fail LED is lit and remains lit until the test is terminated. Local access, Utility.

Test 27 -- This utility displays the current Master Controller firmware revision number on the front panel display. It will remain on the display until five seconds have elapsed. Local access, Utility.

Test 28 -- This utility displays the static portion of the Tape Usage Odometer. The most significant word of the odometer is displayed first by alternating the two bytes in the display. The least significant word can be viewed in the same manner by pressing the test button. Local access, Utility.

Test 29 -- This utility will light the density LEDs supported in this tape drive. The LEDs will remain lit until five seconds have elapsed. Local access, Utility.

Test 30 -- The firmware can be updated in EEPROM using an HP firmware update tape. A version number is first input from the front panel. The tape will be searched for a data record containing a valid firmware update with the version number matching the front panel entry. If a matching record is not found on the tape an error message will be displayed and no firmware update will be done. A successful update will cause the tape drive to perform a power-on self test. Pressing the RESET button while the firmware is being written, will display the message D4H on the display upon successful completion. WARNING: turning off the tape drive while the update is being written may cause your drive to become inoperative. Local access, Utility.

Test 31 -- This utility will set the diagnostic environment to reposition after tests 21, 22, 33 and 34. This is the default mode which is set at initialization. Utility.

Test 32 -- This utility will set the diagnostic environment to "walk" tests 21, 22, 33 and 34 down the tape. Utility.

Test 33 -- A single PE data record is read from a prerecorded tape. If the tape passes EOT, a rewind operation will occur after the data block is read. This test will 'fail' whenever a retry or hardware error occurs. The drive must be online for remote access. Test, Looping, Walking.

Test 34 -- A single GCR data record is read from a prerecorded tape as in Test 33. Test, Looping, Walking.

Test 35 -- This utility will run the servo at PE speed with the erase head on. When the tape reaches EOT, the door is opened or the RESET button is pressed the tape will be rewound. The rewind operation will continue until BOT, the door is opened or the RESET button is pressed. If the BOT marker is detected, the tape is stopped and positioned below the BOT/EOT sensor. Note: A mounted tape must be reloaded by pressing the load button upon completion of the test to bring the drive online. Utility.

Test 36 -- This utility will run the servo at PE speed with the write and erase electronics on. A GCR ARA BURST is written, which is an all one's data pattern. When the tape reaches EOT, the door is opened or the RESET button is pressed the tape will be rewound. The rewind operation will continue until BOT, the door is opened or the RESET button is pressed. If the BOT marker is detected, the tape is stopped and positioned below the BOT/EOT sensor. Note: A mounted tape must be reloaded by pressing the load button upon completion of the test to bring the drive on-line. Utility.

Test 37 -- This utility will run the servo at GCR speed with the write and erase electronics on. A GCR ARA BURST is written, which is an all one's data pattern When the tape reaches EOT, the door is opened or the RESET button is pressed the tape will be rewound. The rewind operation will continue until BOT, the door is opened or the RESET button is pressed. If the BOT marker is detected, the tape is stopped and positioned below the BOT/EOT sensor. Note: A mounted tape must be reloaded by pressing the load button upon completion of the test to bring the drive on-line. Utility.

Test 38 -- This utility will run the servo at PE speed with the read electronics on. When the tape reaches EOT, the door is opened or the RESET button is pressed the tape will be rewound. The rewind operation will continue until BOT, the door is opened or the RESET button is pressed. If the BOT marker is detected, the tape is stopped and positioned below the BOT/EOT sensor. Note: A mounted tape must be reloaded by pressing the load button upon completion of the test to bring the drive online. Utility.

Test 39 -- This utility will run the servo at GCR speed with the read electronics on. When the tape reaches EOT, the door is opened or the RESET button is pressed the tape will be rewound. The rewind operation will continue until BOT, the door is opened or the RESET button is pressed. If the BOT marker is detected, the tape is stopped and positioned below the BOT/EOT sensor. Note: A mounted tape must be reloaded by pressing the load button upon completion of the test to bring the drive online. Utility.

Test 40 -- This utility will run the servo at PE speed in a worst case reposition pattern. Pressing the RESET button or opening and closing the door will terminate this utility. Note: A mounted tape must be reloaded by pressing the load button upon completion of the test to bring the drive on-line. Local access, Utility.

Test 41 -- The Servo Controller interface with the Master Controller is tested by sending a data byte from the Master Controller to the Servo Controller and waiting for the ones complement of the data byte to be returned from the Servo Controller. This handshake sends the data 1, 2, ..., 255, and 0 to the Servo Controller. Test, Looping.

Test 42 -- Servo Controller Power-on self test, which is always performed at power-on or after a reset command from the Master Controller. This test will verify the 8051 CPU's internal RAM and PROM. Test, Looping.

Test 43 -- The Servo Controller will perform a board test by sequencing through tests 49 - 55. Test, Looping.

Test 44 -- Servo Controller gap handling is verified by simulating gap interrupts. This test will not move tape. The Data Detect and Deskew is put into an idle state upon completion of this test and the Servo Controller will be reset. Test, Looping.

Test 45 -- The buffer arm is tested with the aid of an operator. Movement of the buffer arm by the operator is indicated on the front panel display. Local access, Utility.

Test 46 -- The speed encoder may also be fully tested using an operator to move the speed encoder and to watch the front panel display for the correct response of the hardware. Turning the speed encoder clockwise will decrement the display, while turning it counterclockwise will increment the display. The display will be changed approximately 16 counts per revolution of the counter. Local access, Utility.

Test 47 -- Non-existent test.

Test 48 -- This utility displays the current Servo Controller firmware revision number on the front panel display. The revision number will remain on the display until the RESET button is pressed or five seconds have elapsed. Local access, Utility.

Test 49 -- This tests the BOT, EOT, and Write Enable circuitry and detects problems in the BOT and EOT parts. The Write Enable signal is checked to verify that it propagates from the Servo Controller to the Write Electronics Board. Test, Looping.

Test 50 -- The Servo Controller checks to make sure that all the connectors on the Servo Controller Board are connected. Test, Looping.

Test 51 -- This tests to make sure that the Servo Controller can control the hard shutdown line that controls the relay on the Motor Drive Board. Test, Looping.

Test 52 -- This tests the zero-crossing detector by writing minimum and maximum values to the Servo Controller DAC. Test, Looping.

Test 53 -- This tests Servo Controller DAC circuitry. Test, Looping.

Test 54 -- This tests the Servo Controller speed encoder state machine. Test, Looping.

Test 55 -- This tests the Servo Controller in-position and gap interrupt circuitry by generating one in-position and gap interrupt to verify that the interrupts propogate throughout the system. Test, Looping.

Test 56 -- This is an interactive BOT/EOT sensor test. The front panel display will reflect the current status of the sensor. The RESET button must be pressed to exit the test. Local access, Utility.

Test 57 -- This is the Servo Controller power-on self test called by the Channel Program. Tests 41, 42, 43, and 44 are called by this driver. Test, Looping.

Test 58 -- This interactive test will provide a sequence of stimuli for the motors and the motor drive assembly. Pressing the Enter button will cause the Servo Controller to sequence to the next pattern. This test will continue until the Reset button is pressed. The tape drive door must be closed and a tape shouldn't be mounted to run this test. Local access, Utility.

Test 59 -- This interactive test will provide a sequence of scope loops for the servo system. Pressing the Enter button will cause the Servo Controller to sequence to the next pattern. This test will continue until the Reset button is pressed. The tape drive door must be closed and a tape shouldn't be mounted to run this test. Local access, Utility.

Secondary -- The Host to HP-IB loopback will be remotely initiated. The Host will send the data 255, 0, 1, 2, ..., 254 to the HP7978A. The HP 7978A puts the data, upon receipt, into the Data Buffer. The data is checked for correctness, and then sent back to the Host upon request. Remote access, Utility.

Secondary -- A diagnostic test not included in the built-in diagnostics may be sent to the HP 7978A from a Host and executed. This utility will receive the diagnostic as a data record in the Data Buffer, load it into RAM, and execute it. Test results are placed into the Data Buffer by the downloaded diagnostic and returned to the Host; assuming the downloaded test returns the drive to a known state. Remote access, Utility.

Secondary -- A firmware update may also be made remotely. The update information is sent to the tape drive as a data record from the Host. A version number is entered from the front panel and is compared to the version number included in the data record sent from the Host. If a match occurs, the firmware update is written into EEPROM. If a match doesn't occur, an error message is returned without updating the firmware. Remote access, Utility.

Secondary -- The firmware update area of EEPROM is sent to the Host as a single data record upon request. Remote access, Utility.

Secondary -- An image dump of the HP 7978A's status resident in RAM and EEPROM is sent as a data record to the Host upon request. Remote access, Utility.

Special Remote Diagnostics

NOTE

The following diagnostics are available to the Host via talk secondary and listen secondary protocol commands.

Listen 30 Send loopback data from the Host to HP-IB.
Talk 30 Return the loopback data from the HP-IB to the Host.
Listen 3 Download a diagnostic test to the HP 7978A.

Talk 4	Return the downloaded diagnostic results to the Host.
Listen 6	Remote Firmware Update.
Talk 6	Return the Firmware Update Data from EEPROM.
Talk 5	Return HP 7978A Status from EEPROM and RAM.

[3] MOTION CONTROL SYSTEM

3.1 SERVO CONTROLLER

HANDLING POSITIONS

The Servo Controller maintains, in real time, an unambiguous position for each spot on a reel of tape. That position is not directly available to the Master Controller. The Master Controller coordinates the use of these positions by telling the Servo Controller which positions he should store in his memory and whether or not to throw any of them away. Once the proper position is in the Servo Controller's memory, the Servo can move the tape to be up to speed at that position and tell the Master Controller precisely when that position is reached.

When the Servo Controller stores a position in its memory, it pushes it onto a two-deep stack. This process is called "Capturing". Two types of positions can be captured. The first is very precisely measured. It is the position of the tape when the read head enters a gap. The second is not as precise. It is the current position of the tape.

The Servo Controller modifies these positions by an offset just before storing them in its memory. This offset is a function of the speed at which the tape is moving. These "Capture Offsets" are provided only for gap positions.

Once a position has been captured, it may be thrown away by telling the Servo Controller to "pop" off the top of its position stack.

Only the top position on the stack may be used by the Master Controller. When the Servo Controller gets ready to move (called "repositioning") it looks at the top position on its stack and positions itself to be able to be up to speed by that position. When the Servo Controller begins moving the tape, it interrupts the Master Controller when it reaches that position.

An offset can also be specified for the position just before it is used. This offset will be added to the position on the top of the stack just before it is used but does not actually change what has been stored there. It is called an "In Position" Offset.

CONTROLLING TAPE MOTION

LOADING AND UNLOADING

The Servo Controller can load the tape and unload the tape. Loading is a trial and error process. Success is most likely with minimal slack in the tape. Unloading is accomplished by moving in reverse and shutting down the Motor Drivers when tension is lost.

MOVING AND STOPPING

The Servo Controller can move the tape at two read/write speeds. They are +-75.0 ips and +-73.73 ips. It can also rewind the tape at -250 ips. The Master Controller has direct control over the speed and whether the tape is to be moving or stopping.

REPOSITIONING

The Servo Controller is also able to guarantee that it is up to speed and settled by a given position on the tape. In order to do that it has to reposition itself before moving. The Servo Controller locks out the possibility of moving without repositioning first.

MONITORING SENSORS AND STATUS

The Servo Controller has access to the BOT and EOT sensors as well as to information that says whether its speed is within its specifications. All of this information is made available to the Master Controller in real time.

BOT AND EOT

The Servo Controller maintains two status bits for the BOT and EOT. The first indicates when the BOT marker is OVER the sensor. It is called "OVER_BOT". The second indicates whether or not the EOT marker has been PASSED in the forward or reverse direction. It is called "PAST_EOT".

SPEED CHECKING

When the Servo's speed should be meeting it specifications, the Servo Controller maintains a status bit that indicates whether or not it is being successful. This bit is maintained in real time. It is called "SPD_OUT_OF_SPEC". It is true ONLY when the speed should be within spec (i.e., after its settling time) but is not.

PROVIDING REAL-TIME INFORMATION

The Servo Controller can also provide internal information to the Master Controller whenever it is requested. One example of the information 5R$W,.6ast requuetted. This is used by the Master Controller for some special service-related purposes. Other uses are mainly for in the Lab.

RUNNING DIAGNOSTICS

The Servo Controller also contains extensive selftest capabilities. These are utilized both at power-on or after a reset command and whenever the Master Controller requests them.

POWER-ON SELFTEST

The Power On Self Test is automatically executed by the Servo Controller following power-on or a reset command and just preceding loading of the tape. It tests most of the Servo Controller Board and indicates any failures. If any failures are detected, it prevents servo operation.

SPECIFIC TESTS

Specific tests may also be run by the Servo Controller. The Master Controller individually requests and obtains results from each test.

HANDLING ERRORS

Two types of errors can be detected by the Servo Controller. Each of these is discussed below.

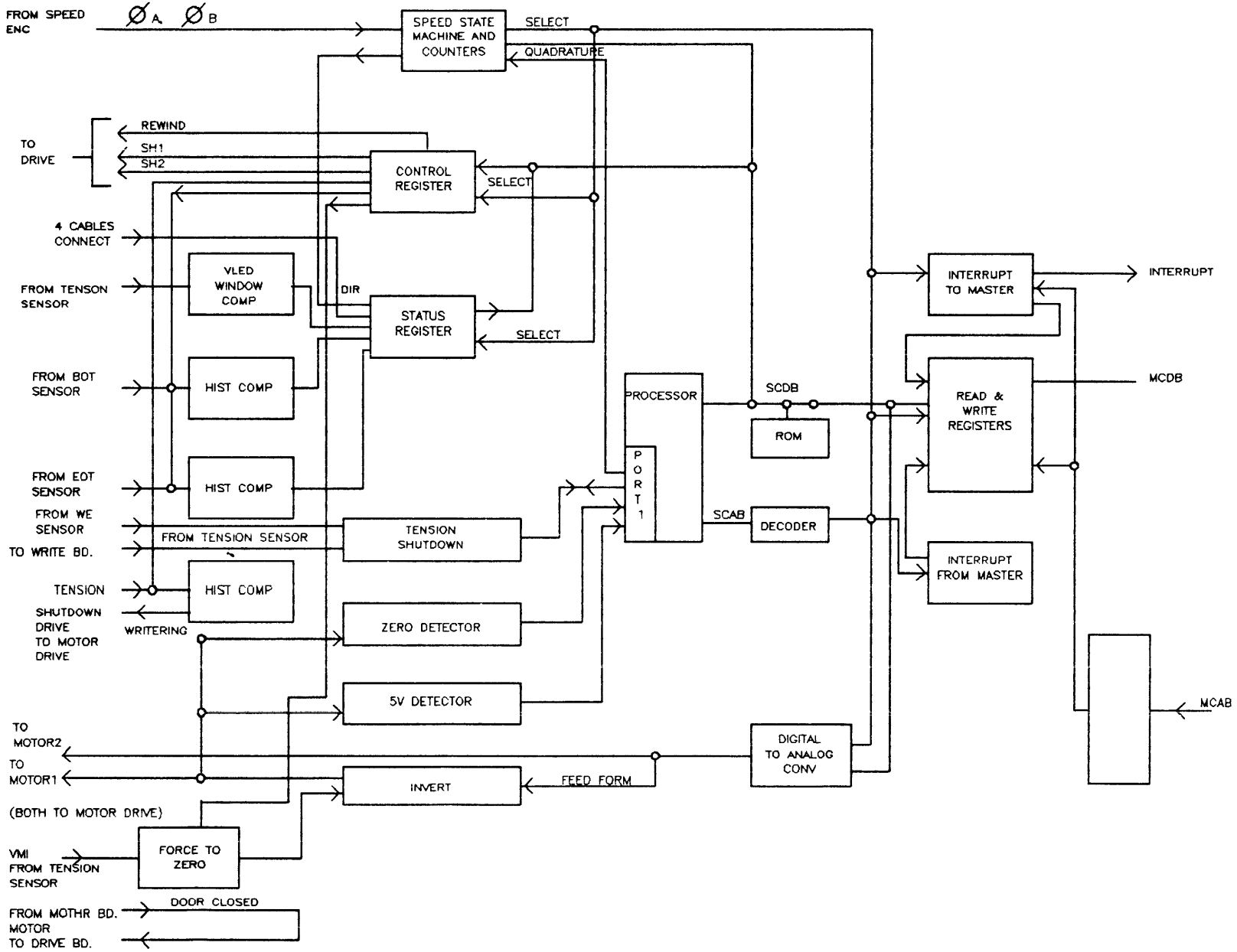
RECOVERABLE ERRORS

The first type is those errors that cannot hurt the tape. These include protocol errors (e.g., invalid parameters) as well as servo "errors" such as unsuccessful attempts at loading the tape. These cause the Servo Controller to ignore all commands until the Master Controller re-enables normal operation. These also have a specific code that tells the Master Controller what the problem is.

CATASTROPHIC ERRORS

The second type of errors is those that make the Servo Controller unable to handle tape safely or those that are are too difficult to recover from. Usually, these are failures of self-tests or unexpected loss of tension. The Servo Controller will not allow loading of the tape once one of these occur until it is re-initialized and selftest is re-run.

Figure (5) 3-1 Servo Controller Block Diagram



3.2 SPEED ENCODER

The speed encoder elecronics measures tape position as derived from the HEDS-6000 optical encoder.

The encoder assembly measures tape speed and direction and gives a rough estimation of tape position for feedback to the Servo Controller. The encoder shaft is attached to a flanged roller which provides critical tape guidance.

The roller rotates with no slippage relative to the tape. Its speed of rotation is therefore proportional to linear tape speed. The roller is rigidly attached to a shaft which in turn has a code wheel attached to it. The code wheel is made up of a repeating pattern of transparent and opaque sections. Light from two LED's is interrupted by the rotating code wheel. Photodetectors receive the modulated light and an electrical signal is generated. After the signals are amplified and passed through a comparator, two TTL-compatible square waves are produced. The square waves are 90 degrees out of phase and provide direction sensing. This phasing is a function of speed and temperature. Channel A will lead channel B for rotation in one direction and the opposite is true for rotation in the other direction.

From this information the servo processor is able to derive position of the tape, speed of the tape and direction of the tape.

The encoder channels A and B are brought into the state machine through schmitt triggers and a 4-to-1 multiplexer. They are filtered by a 3-bit digital filter. The input to the filter must be stationary for 3 clock cycles before the output is allowed to change.

The quadrature decode receives the two filtered shaft encoder signals from the digital filter and produces either a UP or DN pulse on each quadrature transition (see Figure (5) 3-2). If the state diagram is transversed in the clockwise direction, there will be an UP pulse for each state change. Similarly in the counterclockwise direction for DN pulses.

The digital filter was realized by three consecutive D flip flops connected in the form of a shift register. When one of the encoder channels changes, the data is "shifted" into the state machine by the next three consecutive clock pulses. If there is a "glitch" in the incoming encoder data, the filter will require three more clock cycles to qualify a valid input variable.

The state machine and combinational logic then operate on the four input variables to produce either UP or DN pulses. These pulses are fed into 74LS193 synchronous Up-Down counters to determine tape position. The 8051 Servo Controller can read the position through two 8-bit latches onto the data bus.

When the tape speed reaches 65 ips, the Servo Controller may latch quadrature. This must be done to guard against the loss of quadrature by the shaft encoder at high speeds. This is accomplished by pulling the line marked "QUADL" low. This latches in the present direction of tape and disables one of the encoder channels replacing it with a "dummy" channel. The counter frequency is maintained with half the resolution.

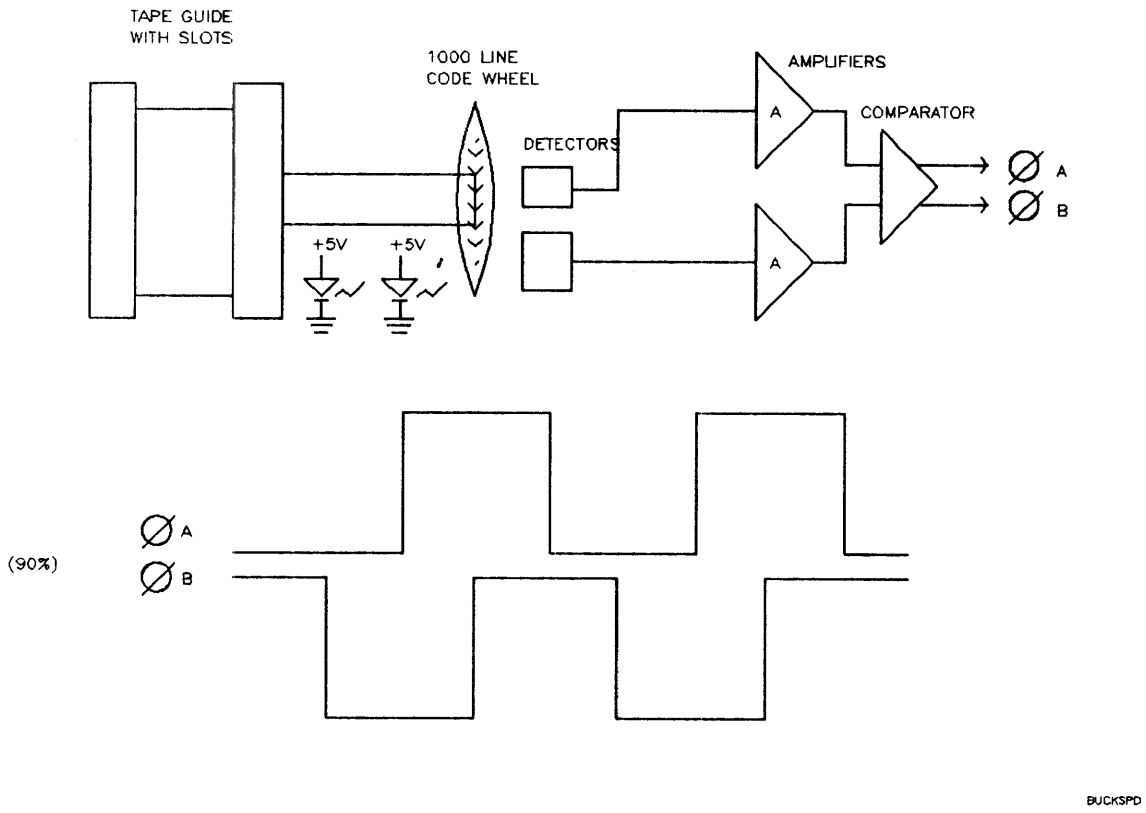


Figure (5) 3-2 Speed Encoder Block Diagrams

3.3 BUFFER ARM ASSEMBLY

The buffer arm electronics has two basic functions. The first is converting degrees to volts and the second is generating the feedback voltage for the buffer arm servo loop.

The conversion from degrees of angular rotation to volts is performed using an optical emitter and detector, a mask between them, circuitry to drive the emitter in such a way as to maintain calibration, and other circuitry to generate the voltage from the signals coming from the detector.

The emitter and detector are both hermetically sealed and use infrared light. The emitter is a flat lens LED. The detector has a flat lens also and consists of two rectangular phototransistors placed side by side. The detector is oriented such that the two elements lie along a line perpendicular to the surface of the board.

The reference voltage is provided to the electronics to provide a reliable buffer arm position voltage independently from allowable fluctuations in supply voltages. Any deviation in this voltage causes a proportional change in gain (Volts per degree of rotation).

The mask is mounted on the shaft of the buffer arm. It has a slot that provides the only path for light to travel through it. The slot is placed such that as the arm rotates, the exposed area of the detector shifts to include more of one element and less of the other.

A feedback circuit on the board insures that calibration is maintained by forcing the sum of the two output currents of the two detector elements and the reference voltage to zero. It drives the LED to whatever it needs to force that sum to zero.

The voltage that is proportional to the angular displacement of the buffer arm is derived from the difference of the two detector elements' currents.

The voltage to be fed back to the motor drive is derived from the voltage proportional to the angular displacement. That voltage is fed through a filter before leaving the board. The properties of the filter are such that the buffer arm servo is stable for all reel conditions and velocities.

The buffer arm electronics board provides three signals as outputs.

LED Drive Voltage (VLED)

The drive voltage of the LED is provided strictly as a check to see that the buffer arm is operating within its limits. If this voltage ever gets close to saturation, the feedback curcuit on the board is trying too hard to drive the LED to provide trustworthy signals. This could happen if the LED opens. In that case, the buffer arm position signal would equal zero (0-0=0) regardless of the arm's angular position.

This signal should be between 0 and -8 Volts for proper operation of the buffer arm electronics. Any voltage less than -8 Volts indicates operation beyond the design limitations of the board.

Buffer Arm Position Voltage (TENS)

The buffer arm position signal is provided solely for detection of over and under tension conditions. During closed loop operation of the buffer arm servo, this signal should stay between some reasonable limits. If it ever goes out of its limits, the loop should be shut down immediately.

This signal should stay between +7.0 volts and -7.0 volts during closed loop operation.

Motor 1 Servo Voltage (VM1)

The Servo Voltage is provided to be ultimately fed to the motor drive to the top motor. It is the buffer arm servo.

This voltage is the opposite sense from the position voltage. That is, increasing TENS should correspond to decreasing VM1. This signal is totally characterized by the needs of the buffer arm servo design.

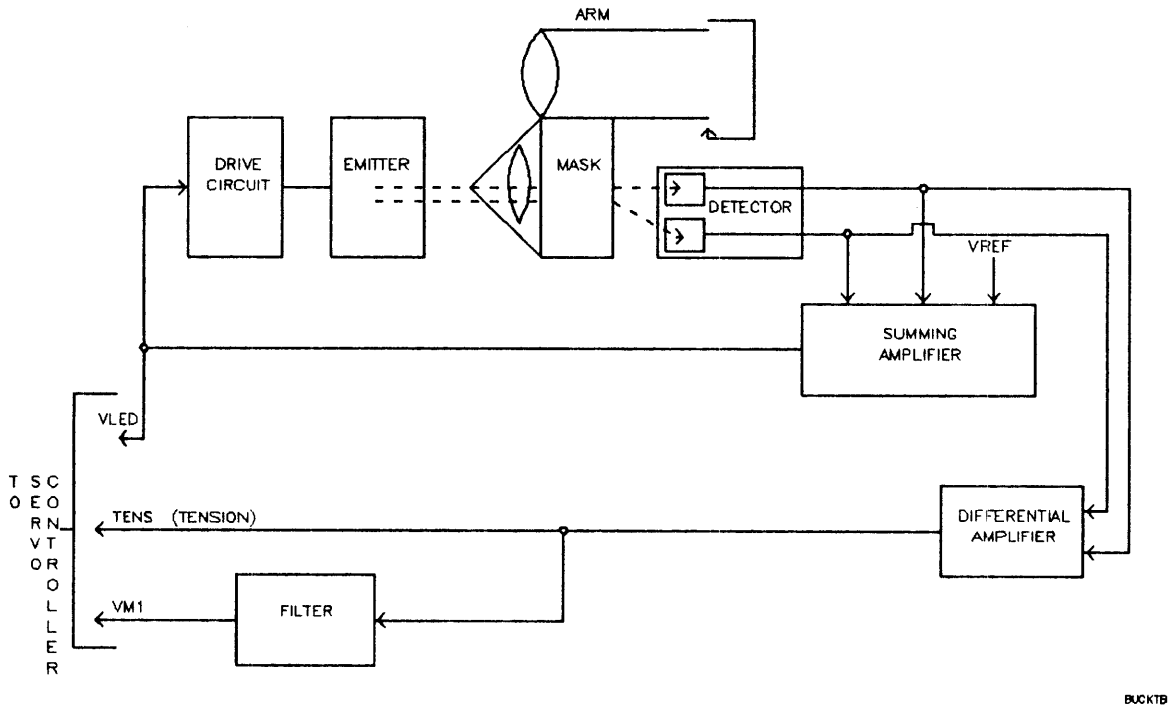


Figure (5) 3-3 Buffer Arm Assembly Block Diagram

3.4 MOTOR DRIVE BOARD

The function of the motor drive board (MDB) is to drive the supply and takeup motors of the HP 7978A. The MDB receives control signals from other boards in the HP 7978A. These signals are then used to determine the speed and position of the motors. The MDB also contains shutdown circuitry designed for motor control due to safety and firmware concerns.

The MDB consists of three main sections; the switching preregulator circuitry, the amplifier circuitry, and the shutdown circuitry. The function of the preregulator circuitry is to take the voltages from the transformer and regulate them to the proper DC level for the amplifier circuitry. The function of the amplifier circuitry is to take the motor control signals from the Servo Controller (SC) and amplify them so as to properly position the motors. The final section of the MDB is the shutdown circuitry. The function of this circuitry is to shut down the output to the motors whenever warranted by safety concerns as determined by Servo Controller firmware.

PREREGULATOR CIRCUITRY

The HP 7978A reads and writes at 75 inches per second (ips) and rewinds at 250 ips. At these speeds the required motor voltages are +26 volts and -26 volts for the read/write operations and +52 volts for the operation which rewinds the tape. The function of the preregulator is to provide these voltages as required. The preregulator consists of two voltage power supplies; one which provides +26/52 volts while the other provides -26 volts.

The reason for having the two selectable positive voltages for the positive supply and only one negative voltage for the negative supply is due to the 250 ips tape speed required for tape rewind. When the tape is rewinding, only the top positive half of the motor drive amplifiers are operating. The rewinding operation is accompanied by a rewind signal (REWIND). When REWIND is a logic high, the +52 volts is selected and subsequently used for rewinding the tape. When REWIND is logic low, the +26 volts is used.

Aside from the fact that the positive supply output voltage changes between +26 volts and +52 volts, the two preregulator circuits are virtually identical topographically. The basic preregulator design used for both power supplies is a switching design which employs an SCR as the switching element. The switching preregulator, which is switching at twice the line frequency, provides a coarse regulated voltage to the motor drive linear power amplifiers. The regulation is coarse because, due to the low switcing frequency, a large amount of ripple noise may be present at the output (e.g. 4 volts p-p) of the preregulator. Even though the preregulator voltage outputs may be very noisy, the motor drive linear power amplifiers, which receive their input power from the preregulators, will, due to their own feedback loops, reject virtually all of this periodic ripple noise in supplying a clean regulated voltage to their respective motors. Thus, the coarsely regulated low bandwidth voltage outputs of the preregulators are converted, via the linear motor drive amplifiers, to very precisely regulated high bandwidth voltages applied to the motors.

AMPLIFIER CIRCUITRY

The motor drive amplifier circuitry consist of two amplifier networks. Each is a power amplifier which consists of two 20A, 250W, 140V TO-3 push-pull transistors in it's output stage. One amplifier network is for the velocity motor, the other amplifier is for the tension motor. These amplifiers are fundamentally identical as implemented on the MDB. One amplifier is described here with the understanding that there are two amplifiers.

Each amplifier has two halves; a positive half and a negative half. The positive half uses the +26/52 preregulated voltage while the negative half uses the -26 preregulated voltage.

When the positive half of the amplifier is active, a positive current is being supplied by the MDA to the motor which, in turn, produces a torque in the counter-clockwise direction. When the negative half of the amplifier is active, a negative current is being supplied by the MDA which, in turn, produces a torque in the clockwise direction. Each half is virtually identical with the exception of the applied voltage as mentioned. Each amplifier consists of three internally nested feedback loops. The outermost feedback loop controls the dominant DC and AC characteristics. It sets the DC gain and bandwidth of the amplifier. This feedback loop also pushes the electrical pole of the motor out in frequency via lead compensation.

In addition, the amplifier must also be able to sink and source large currents (i.e. 10 amperes) at voltages between +52 volts and -26 volts.

The remaining feedback loops set the gain at ten within the outer loop and control the overall amplifier stability. The The most critical of all three loops is the innermost loop. This loop is a voltage-shunt feedback around a transresistance amplifier (a darlington configuration). That is, the feedback is voltage sensed from the output and approximately current (shunt) inserted into the input. The remaining feedback path is that of a voltage-series feedback. That is, the output is voltage-sampled and series-inserted with the input.

SHUTDOWN CIRCUITS

The amplifiers are required to be shut down under certain conditions. The shutdown circuits described below accomplish these shutdown functions.

PWRGD

The PWRGD signal indicates whether the +5 volts is within tolerance. This signal is generated by the power supply and sent to the MDB. This signal is logic high when the voltage is within +/- 5% of its set value. When PWRGD is logic high, the amplifiers of the MDB are able to drive the motors unless another shutdown is enabled.

SHDN*

This signal initiates a shutdown which disengages the relay of the MDB. By doing so, the output of the amplifiers are no longer connected to the motors. This shutdown is initiated by the Servo Controller. The purpose of this shutdown is to protect the tape. The SHDN signal is low when the tape loses tension or there is over tension.

SH1

The SH1 signal initiates a shutdown which does not allow a MOT1 signal, sent from the SC, to be amplified and applied to the tension motor The purpose of this shutdown is to allow the tape to be tensioned for a tape loading operation. That is, it forces the tension motor to have zero voltage (i.e. viscous braking) so the velocity motor can establish tension. SH1 is active at all times except during normal tape read/write/standby operations.

SH2*

The SH2* signal initiates a shutdown which disables both amplifiers in the MDB. This is accomplished by turning on and saturating a transistor in each amplifier input stage of the MDB. Hence, this forces the AMP1 and AMP2 outputs of both MDA's to ground. These outputs exhibit a very high impedance for applied voltages less than +/- 6 volts and therefore appear tristated. signals to ground. SH2* is active low and is used when the servo loop is not closed thus the tape is not tensioned.

DRCL*

The DRCL signal initiates a shutdown which disengages the relay of the MDB. This signal is activated when the door of the tape drive is opened. The motors will be disengaged from the amplifiers if:

a) the door is open for more than two seconds and
b) there is more than 6 volts (in magnitude) present on either motor and
c) the operator is not loading tape onto the tape drive.

This shutdown has been implemented to ensure that the operator will not be cut by moving tape.

INPUTS TO THE MOTOR DRIVE BOARD

Most of the inputs to the MDB have been discussed in previous sections. This section will describe the remaining inputs and also briefly review the previously discussed signals. PWRGD, SHDN, SH1, SH2*, AND DRCL, are shutdowns and are discussed in the previous section. REWIND is the signal which is used in conjunction with the system that rewinds the tape. This signal also

causes the MDB preregulator to switch from +26 volts to +52 volts. The +12, -12, +5 volts and ground are supplied to the MDB through the SC from the HP 7978A power supply.

The remaining input signals are MOT1 and MOT2. These signals are sent to the MDB from the SC. Both MOT1 and MOT2 signals range from +8 volts to -8 volts and represent, at any given instant, the necessary and correct voltage to be applied to the respective motor to maintain the proper tension and velocity for the tape as determined by the distributed (but integrated) servo of the tape drive. Both signals are amplified by a factor of seven, at low frequencies, by the MDB and sent to the motors. This amplification and transfer to the motors are subject to the shutdowns as described in "SHUTDOWN CIRCUITS".

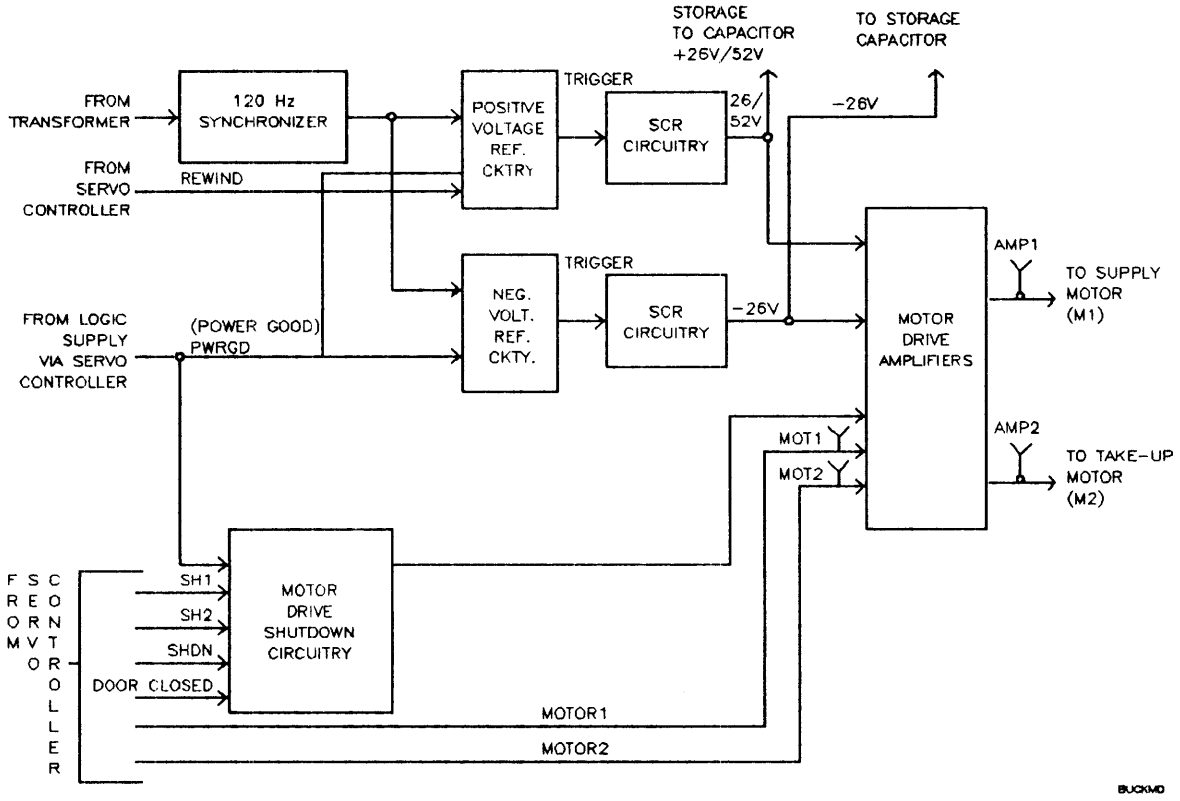


Figure (5) 3-4 Motor Drive Assembly Block Diagram

3.5 SUPPLY REEL MOTOR AND HUB

The hub and motor assembly allows the user to easily attach (detach) tape reels to the motor. The reel is aligned with the rest of the tape path by three rollers which force it into contact with the hub turntable before it is locked in place. A slight push of the hub lever causes it to snap closed, locking the reel in place. The lever must be pulled open to allow the reel to be removed. The motor operates under servo control to maintain proper tape speed and tension. The motor also brings the tape to a stop at power failure.

A chrome plated cylinder, which is free to move along the axis of the motor, is attached to the hub and may not rotate relative to the hub. The cyclinder is spring loaded so that it will extend into the groove of the reel when the write enable ring is removed. When the write enable ring is in place, this cylinder translates along the motor axis. A reflective sensor mounted on the main casting is pointed in a radial direction to the cylinder. When the write enable ring is installed, the sensor views the reflective cyclinder and writing on the tape is permitted.

3.6 TAKEUP REEL MOTOR AND HUB

The take-up reel and motor assembly stores tape as it is runs past the head. The reel is aligned to the rest of the tape path for proper tape transportation. The motor operates under servo control to maintain proper tape speed and tension. The motor also brings the tape to a stop in the case of power failure.

The reel is rigidly attached to the motor. The reel has three cutouts in its flanges to allow the operator to wind tape on to it. The reel is held in place by a cover that compresses an o-ring between itself and the reel. The cover is attached to an aluminum turntable by three screws that are accessible from the front of the drive.

3.7 TAPE PATH

The Head Plate assembly includes the tape head, the tape cleaner, the two fixed guides, the head plate with the skew adjustment apparatus and the end-of-tape and beginning-of-tape sensors and mounting.

The tape path essentially guides the magnetic tape to and over the tape head in a precise manner. For the tape head to function properly, the wrap angles to and from the head and the location of the tape with respect to the gaps on the head must be held accurately. In addition, the tape must have a uniform stress profile across its width without any shear stresses, as this adversely affects the skew.

The tape cleaner cleans the tape of any loose particles and debris which can cause read/write errors (dropouts) as the tape passes over the head. The cleaner scrapes the particles off the tape with sharp-edged hard surfaces made of aluminum oxide.

Two fixed guides with their ceramic (A12O3) washers determine where the tape is positioned with respect to the gaps on the head and therefore determine any off-track error.

These components are all mounted on the head plate which has a precision flat surface and therefore locates these components accurately in the vertical dimension with respect to each other. The head plate also has skew adjustment apparatus. This apparatus adjusts the angle of the head (azimuth) with respect to the rest of the tape path and hence, the tape.

The tape path must allow the head assembly to read and write on one-half inch magnetic tape in 1600 PE and 6250 GCR formats. The tape path supports a tape speed of 75 ips and a tape tension of between 2.1 and 3.5 newtons (7.5 to 12.5 ozf). In addition, the tape path must be able to have a minimum of 500 tape passes of a good section of tape without having a hard dropout or hard data error induced in the tape by the tape path.

The placement of the head with respect to the two fixed guides forms approximately a 2:1 ratio. This helps our drive be compatible with other tape drives in terms of skew.

The wear surfaces of the tape cleaner, edge guides (washers), and the tape head all have a hard ceramic coating. In the case of the tape cleaner and the edge guide washers, the ceramic is aluminum oxide. These ceramics will enable the life of the tape path to exceed 8000 hours of continuous operation. The bearings of the rollers are sealed and well lubricated, so that they should meet the 8000-hour specification unless abused by improper cleaning techinques. The fixed guide posts are made of stainless steel and will last over 8000 hours.

The tape guide roller barrels are made of stainless steel and have hard chromed stainless steel flanges for a long lifetime of tape guiding without edge damage to the tape. Thes roller barrels may require degaussing if exposed to excessive magnetic fields. They are factory degaussed to 2 gauss.

To remove the tape head assembly requires only the removal of three screws and the use of a standard posi-drive screwdriver. To remove the EOT/BOT sensor housing requires a hex key and removal of one screw.

The tape path is gentle on the tape and allows at least 500 passes of a good section of tape without inducing a hard data error on the tape. In addition, the tape cleaner reduces the amount of soft errors (i.e. read/write retries) to an acceptable level. Gentle handling of the tape is accomplished by the low pressure placed on the tape edge by the edge guides (ceramic washers) and by providing a large radius on the fixed guides to lower stress on the tape. The tape cleaner is also fairly gentle on the tape. Rather than having sharp blades to scrape the oxide surface of the tape, it consists of a series of 90-degree vertical traps which capture any tape debris.

A nominal tape tension of 2.8 newtons (10 ozf) was decided upon for the following reasons. At the higher tape speeds, more tension reduces the flying height of the tape over the head. The HP 7976 also has a nominal tension of 2.8 newtons at the head. Therefore, tension changes would be minimized between tapes written on the HP 7976 and the HP 7978A. The higher tension also allows interchange between the HP 7978A and the higher speed (200 ips GCR) machines of other manufacturers. Lower tensions on the tape present the possibility of tape cinching or slipping in the reels on these higher speed machines.

[4] POWER DISTRIBUTION SYSTEM

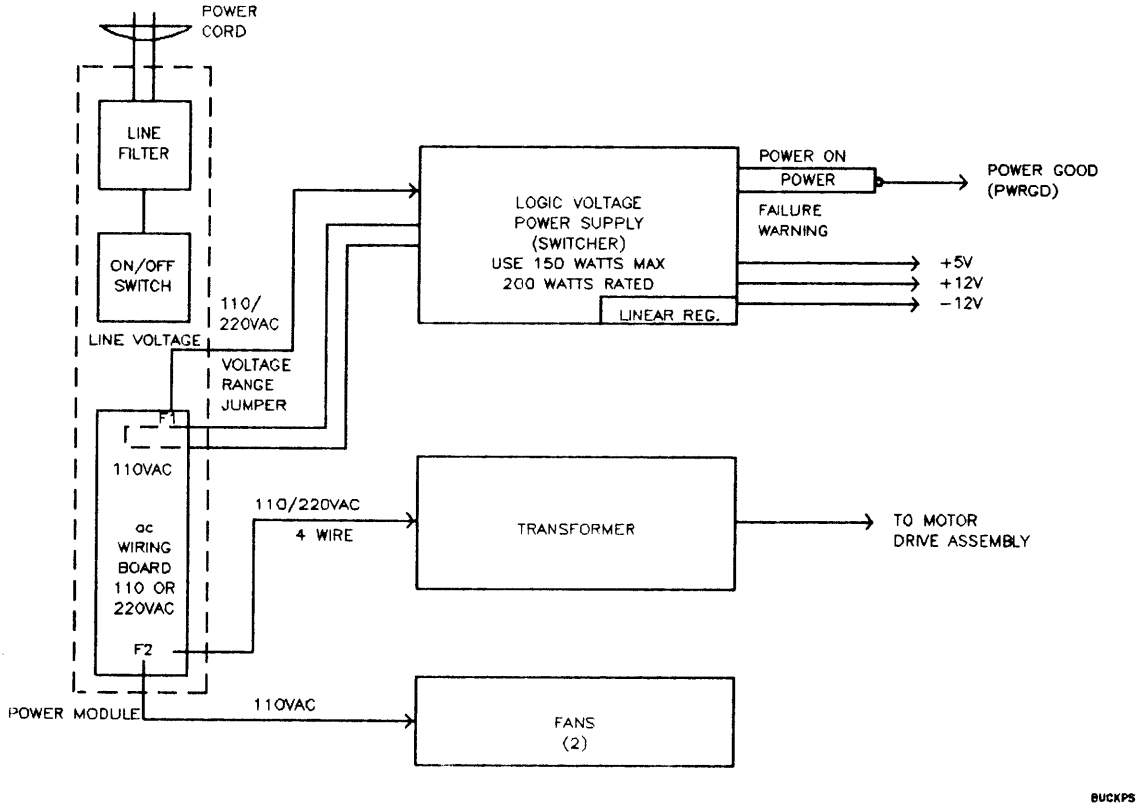


Figure (5) 4-1 Power Distribution

4.1 LINE FILTER

4.2 AC BOARD

4.3 POWER SUPPLY

(The following is a brief overview of the power supply. No troubleshooting will be done within the Power Module which includes the power supply- this is for general information only).

The AC line passes through an RFI filter intended to keep switcher noise from being transmkitted back out the AC line. The input voltage is rectified and the resulting DC energy is stored in the input capacitor(s). These capacitors provide both filtering of the pulsating DC from the rectifier and the "holdup" (short-term energy source) for the supply in the event of line failure.

The transistor switch chops the DC input from the capacitor into a pulse train. The pulse width is modulated by the feedback loop to maintain one output at a constant voltage. The pulse train is then filtered by the primary inductor to provide a smooth DC output. The primary inductor is the main energy storage element in this two-stage design.

The filtered DC voltage from the primary inductor drives the inverter. Boschert, the manufacturer of this power supply, uses two types of inverters, push-pull and half-bridge. Both use a saturating reactor to determine their frequency, which is about 20 KHZ. Each type is used for different manufacturability reasons. However, their operation and purpose is virtually the same. The free-running inverter transforms the high DC input voltage to the various output voltages via the output transformer. A push-pull type is shown in Figure (5) 4-2.

The outputs of the transformer are full-wave rectified and filtered using IC circuits.

A feedback loop, which uses an opto-isolator to isolate the primary (which floats at line potential) and secondary, regulates one output. The +5V output is regulated.

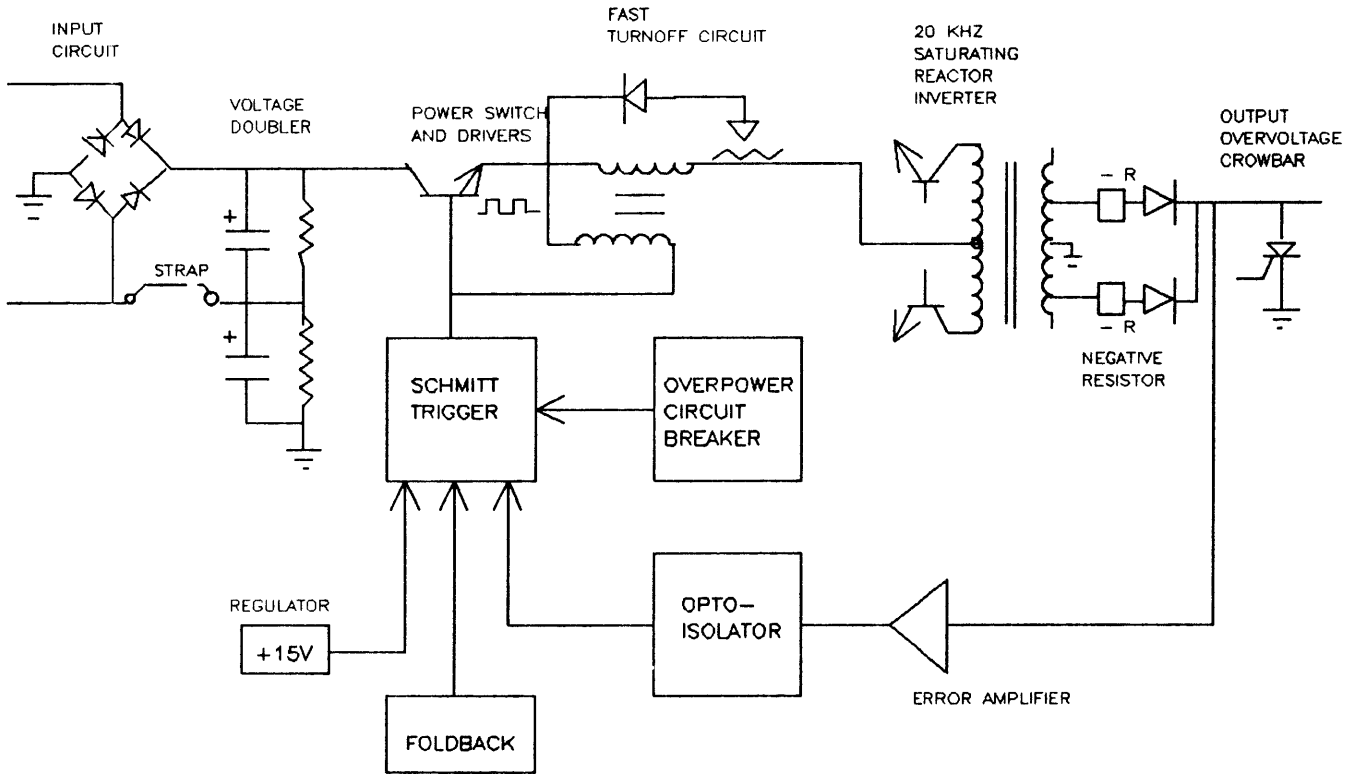


Figure (5) 4-2 Two-Stage Power Supply (Push-Pull or Half-Bridge)

[5] FRONT PANEL

The front panel provides an interface between the operator and the HP 7978A. Interaction is through 6 operator input buttons and 15 individually-controllable LED displays.

The front panel board also contains a Hall Effect device which uses a magnet mounted in the door to sense whether the tape path door is open or not.

Besides interfacing mechanically and optically with the operator, the front panel board interfaces electrically with two other HP 7978A assemblies; the Master Controller assembly and the motor driver assembly. Normally, communication of the front panel to other assemblies is done through the Master Controller assembly. Operator safety is maintained by a hardwired line to the motor driver assembly which enables the front panel DOOR OPEN signal to deactivate the reel motors when the tape door is opened and either drive motor is turning. This signal is also sent to the Master Controller assembly but motor shutdown does not depend on the Master Controller.

The Master Controller assembly microprocessor regards the four write registers and one read register of the front panel as locations in its own external read/write memory space.

To determine if a button is pressed, or if the tape path door is open, the Master Controller reads from the front panel "memory". To turn on any combination of the various front panel LED's, the Master Controller writes to the front panel "memory".

Of the 15 LED displays, two are 7-segment hexadecimal displays and one is a tri-color display capable of displaying red, green, or yellow. All displays can be blanked out.

The 6 entry buttons are highly reliable membrane switches which are sandwiched directly onto the front panel board. To add more reliablility, two switches per entry button are used in a parallel fashion. All the buttons except for the RESET button are debounced via Master Controller software. The RESET button, because of its critical importance, is latched by an R-S flip flop on the front panel board so that the Master Controller can be assured of never missing a possible momentary activation by the operator (the front panel never interrupts the Master Controller, but merely waits to be serviced). The Master Controller can then clear this R-S flip flop, via a front panel write register, once it has been set.

The Master Controller assembly can verify the front panel is present during selftest diagnostics by writing and then reading back a "diagnostic bit".

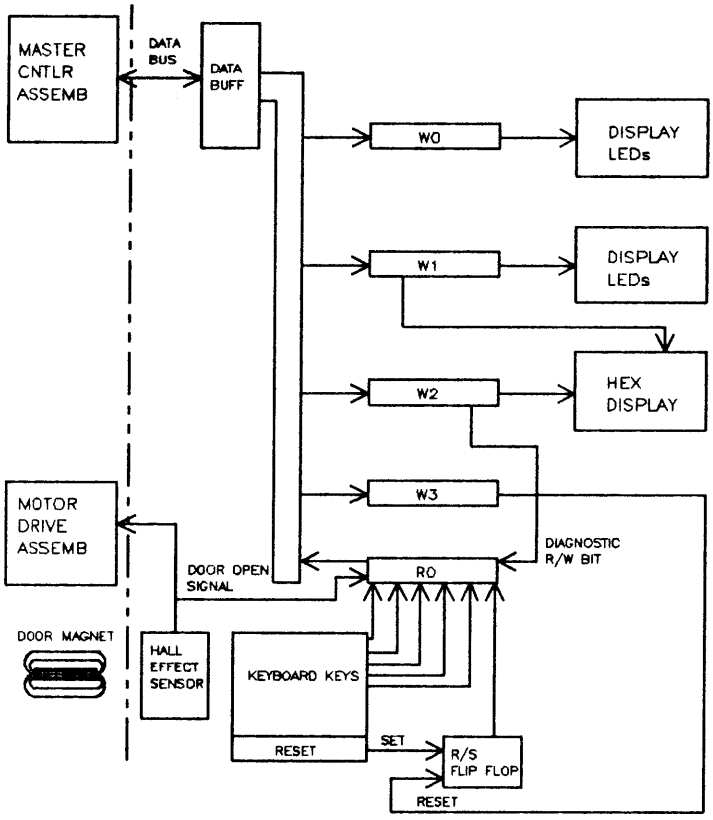


Figure (5) 4-3 Front Panel Block Diagram

VI REMOVAL AND REPLACEMENT

[1] CASTING

1.1 ACCESS

1. Grasp the lower decorative panel by the lower edge and pull. Panel is held on by insertion-fit connectors.

3. Use flat-blade screwdriver to rotate casting access screw counterclockwise 1/2 turn to release casting.

4. Swing casting out.

1.2 SUPPLY REEL MOTOR AND HUB

REMOVAL

1. Take off tape reel if one is mounted.

2. Cut the tie wrap around the power cable.

3. Disconnect power cable from Motor Driver Assembly (A2). The cable is mounted to the vertical connector on the right side of the front of the board. Squeeze connector tabs to unlock.

4. Use a ratchet or adjustable crescent wrench to loosen four M8x25 bolts holding motor mount onto casting.

CAUTION

Use care when rotating the adjustable wrench in the vicinity of the Buffer Assembly PC board, which is to the right of the supply reel motor.

5. Use 13 mm nutdriver to remove bottom two bolts.

WARNING

Support the motor to prevent it from falling from the casting during the next step.

5. Remove upper two bolts.

6. Rotate the motor assembly clockwise enough to clear the Tension Sensor PC board.

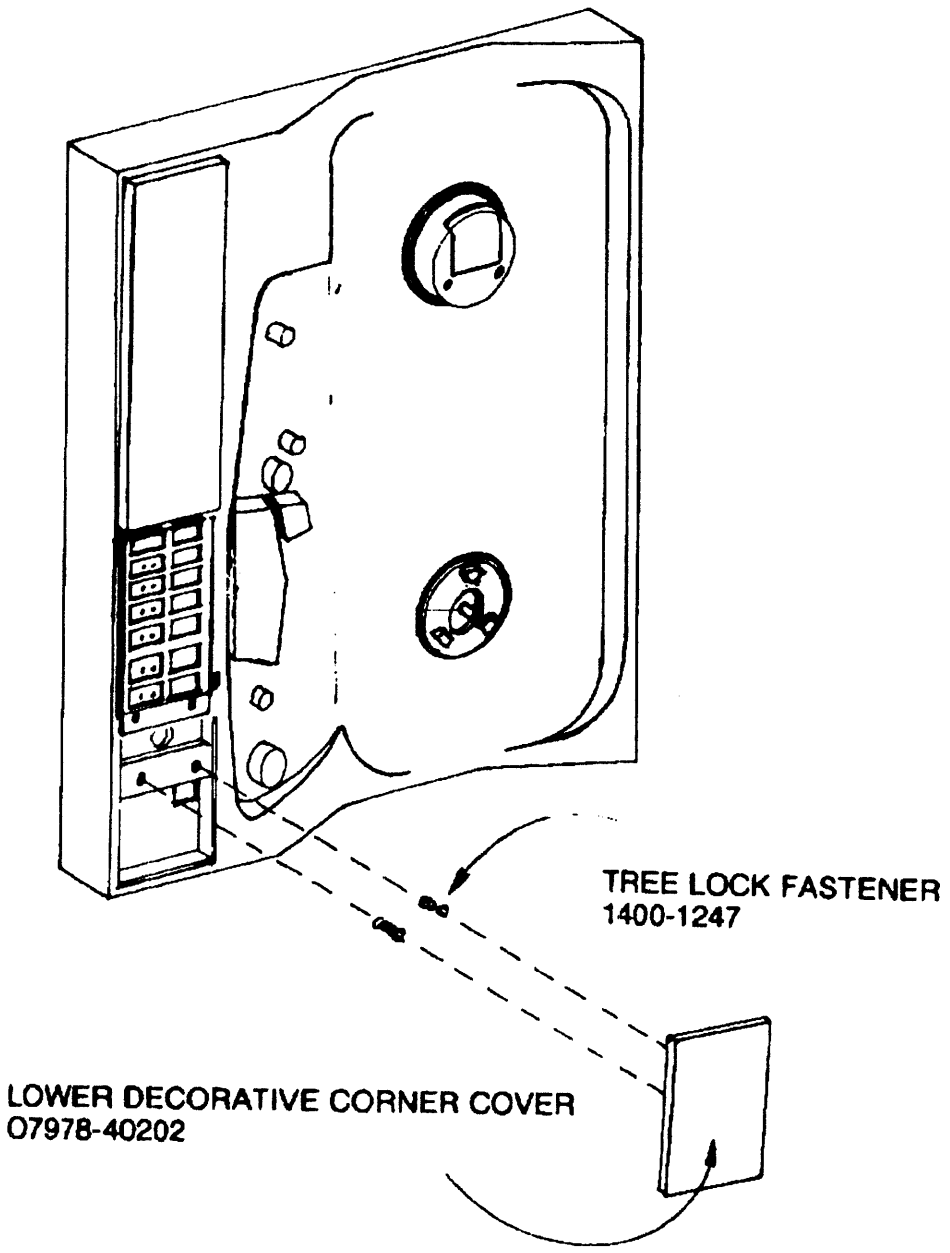


Figure (6) 1-1 Casting Access

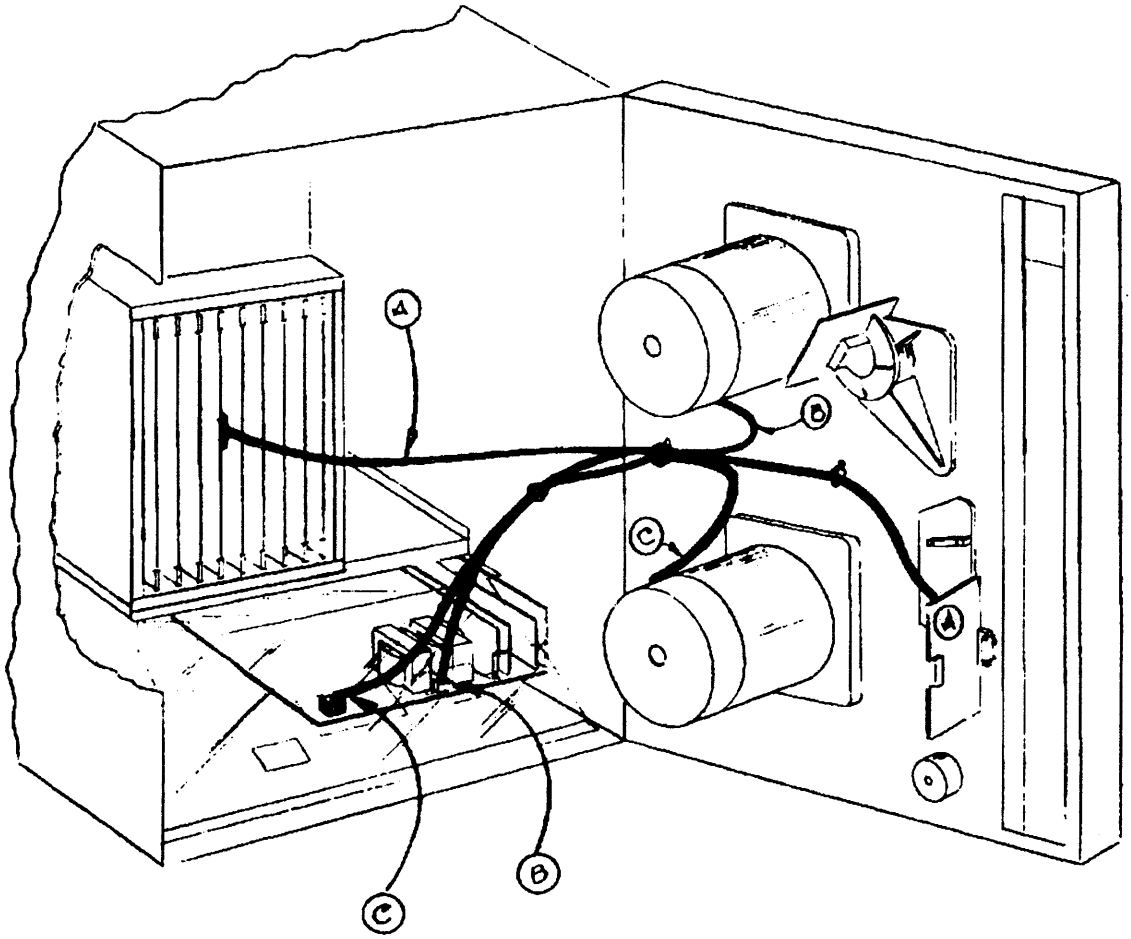


Figure (6) 1-2 Motor Cables

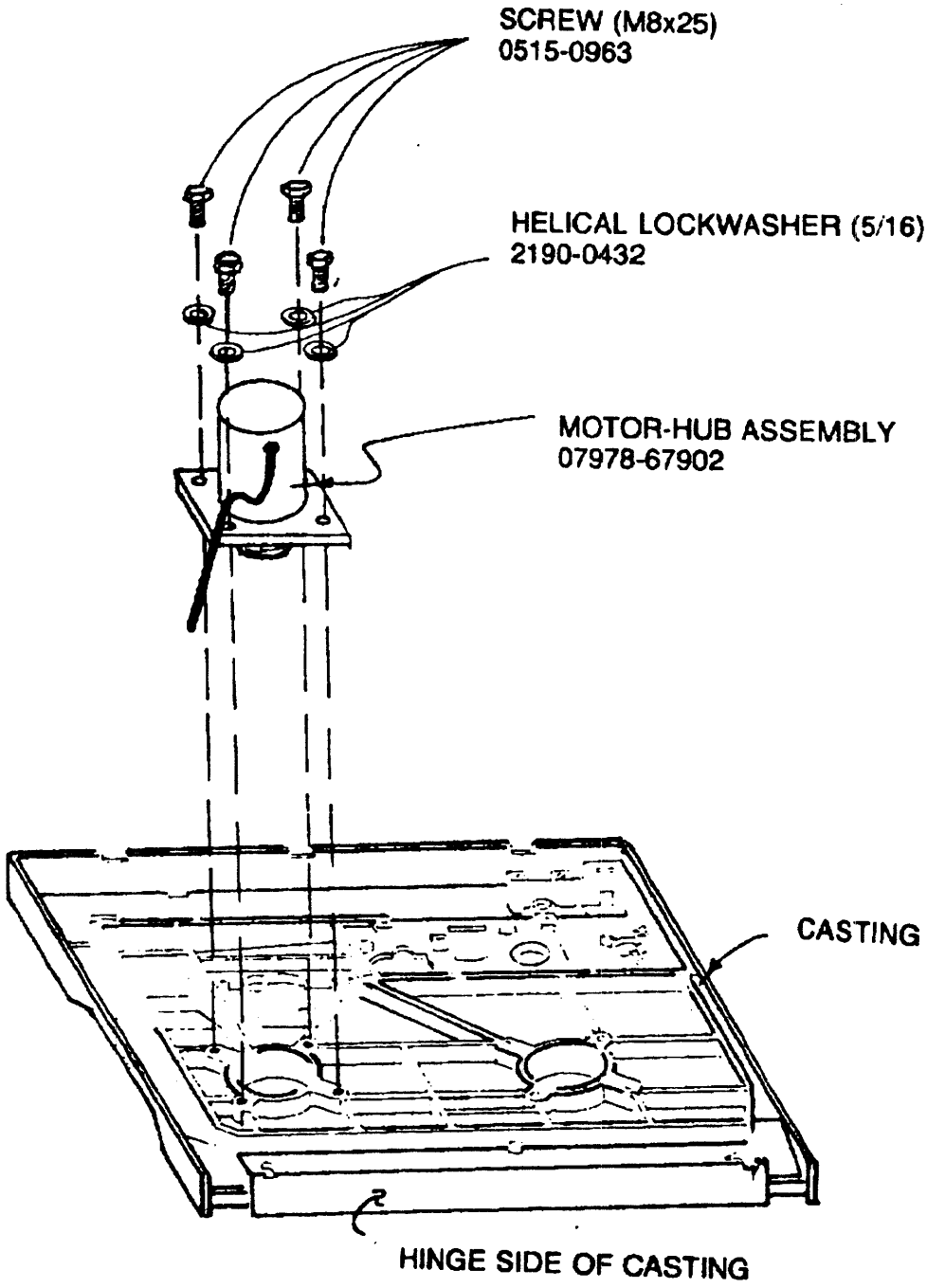


Figure (6) 1-3 Supply Motor

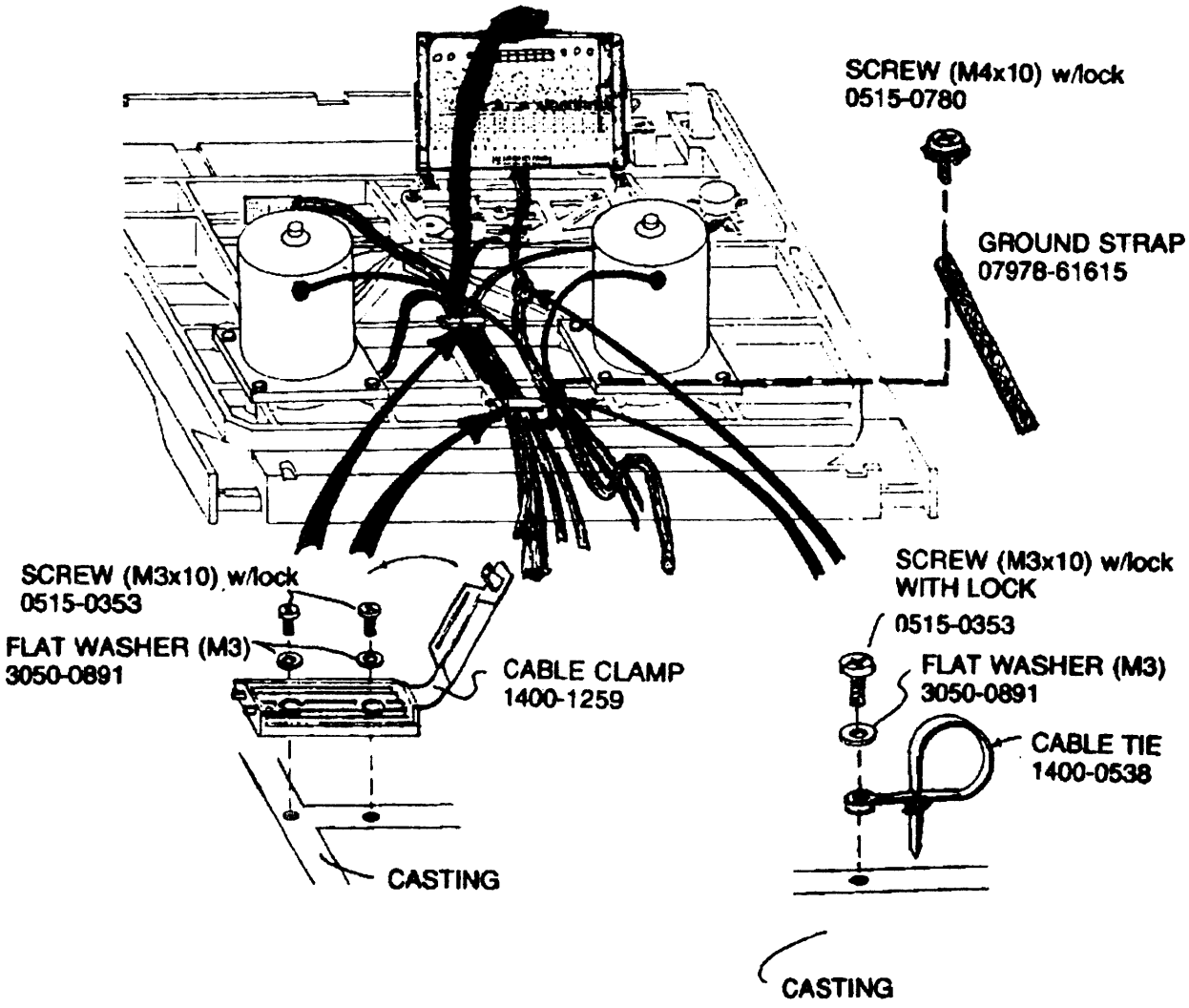


Figure (6) 1-4 Cable Clamping

REPLACEMENT

1. Rotate motor/turntable assembly as needed to pass assembly past Tension Sensor PC board. Align mounting holes. Ensure that the motor power cord is on top of the motor when the motor is placed into position.

2. Insert and finger-tighten top two M8x25 bolts and 5/16" helical washers.

3. Insert and finger-tighten bottom two M8x25 bolts and 5/16" helical washers.

4. Use a ratchet or adjustable wrench to firmly tighten all four motor mount bolts.

5. Connect motor power cable to Motor Driver Assembly (A2) (vertical connector on the right side).

6. Route motor power cable to left tie-wrap point on the back of the casting (see drawing) and tie-wrap cable to the takeup motor power cable and Tape Head Assembly cable. Screw tie wrap to casting with M3x10 lockscrew and flatwasher.

7. Rotate hub by hand to check for free operation.

8. Mount a reel of tape. See Section II for tape mounting instructions, if needed.

1.3 TAKEUP REEL MOTOR AND TURNTABLE

REMOVAL

1. Remove three M4x8 Allen screws and lockwashers holding the fixed reel cover to the hub.

2. Remove the fixed reel cover, O-ring, and tape reel.

3. Cut the tie wrap holding the motor power cable at the rear of the casting.

4. Disconnect motor power cable connection to Motor Driver Assembly (A2) (vertical connector on the left). Squeeze to unlock.

5. Use adjustable crescent wrench to loosen four M8x25 bolts holding motor mount onto casting.

6. Use a 13 mm nutdriver to remove bottom two bolts.

WARNING

Support the motor to prevent it from falling from the casting during the next step.

7. Remove upper two bolts.

8. Withdraw motor and turntable assembly from casting.

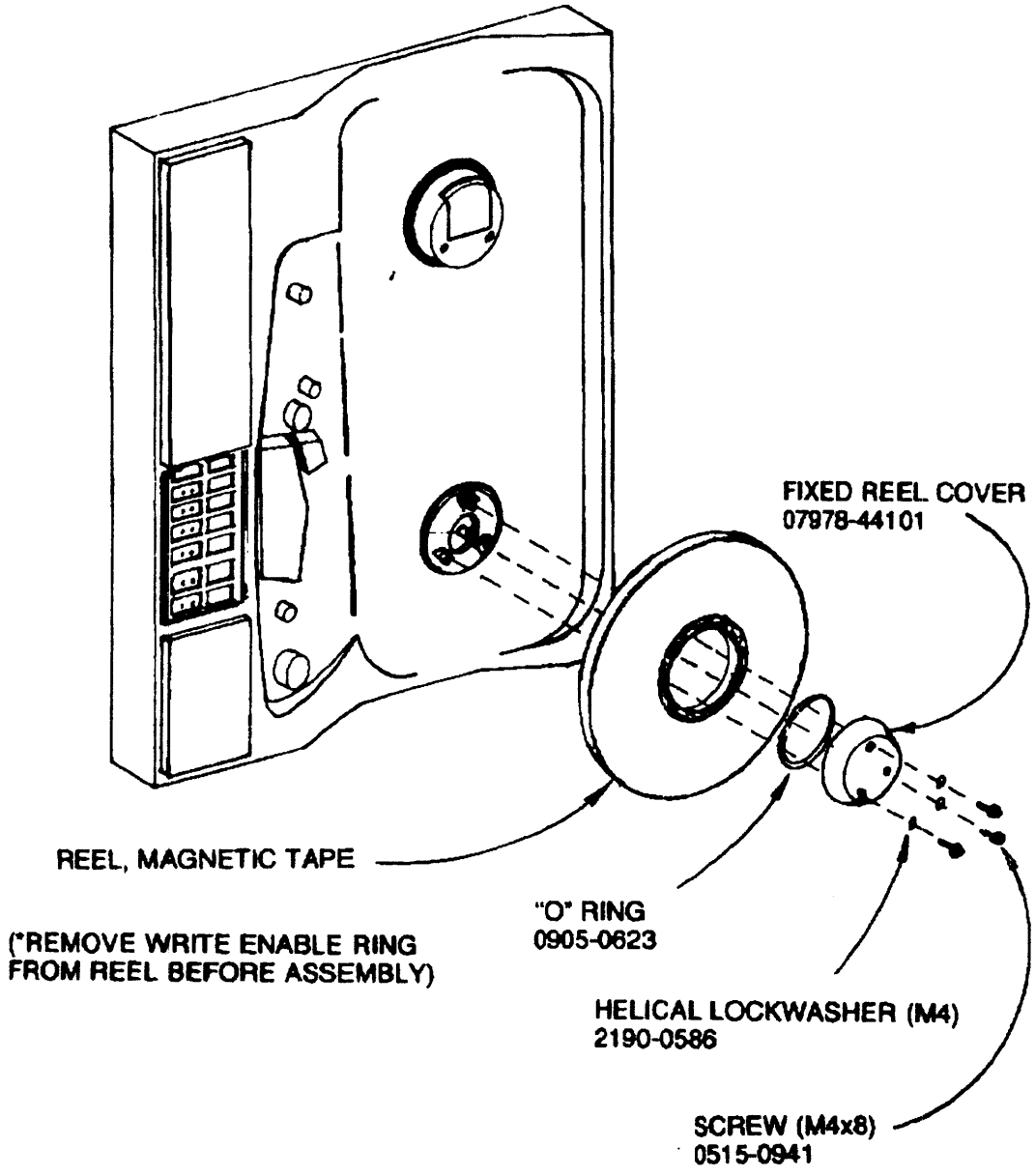


Figure (6) 1-5 Takeup Reel

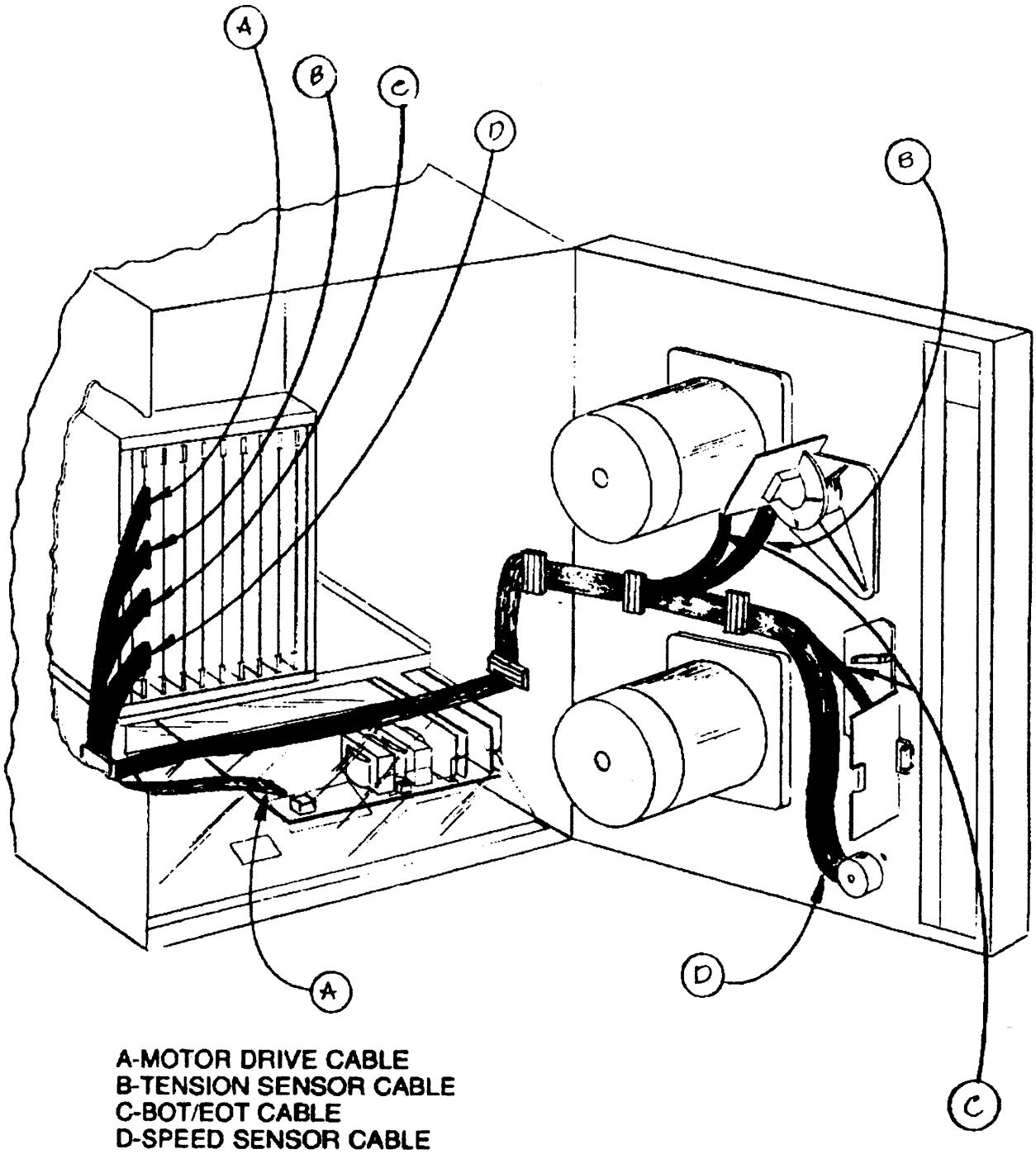


Figure (6) 1-6 Control Cables

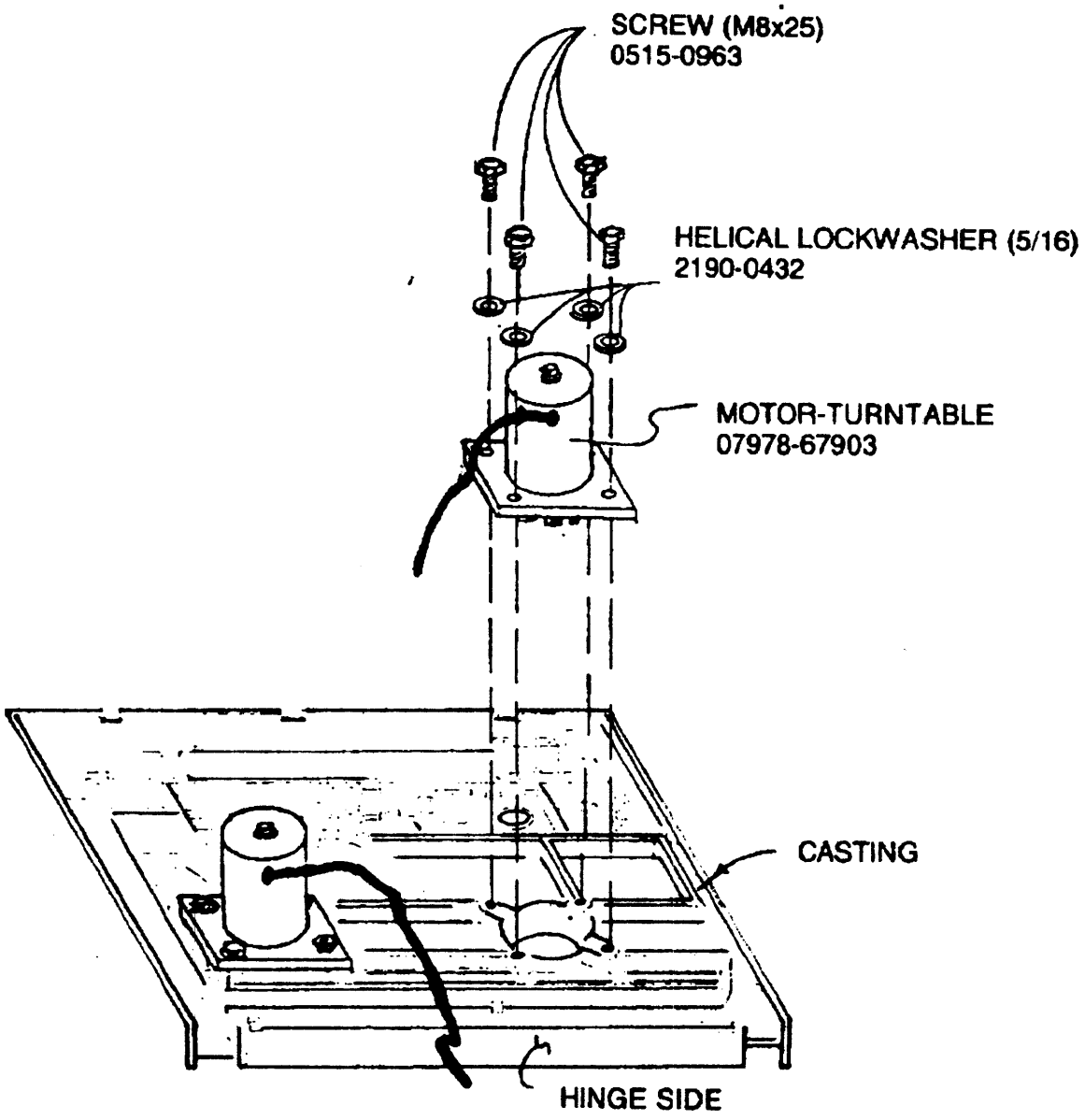


Figure (6) 1-7 Takeup Motor

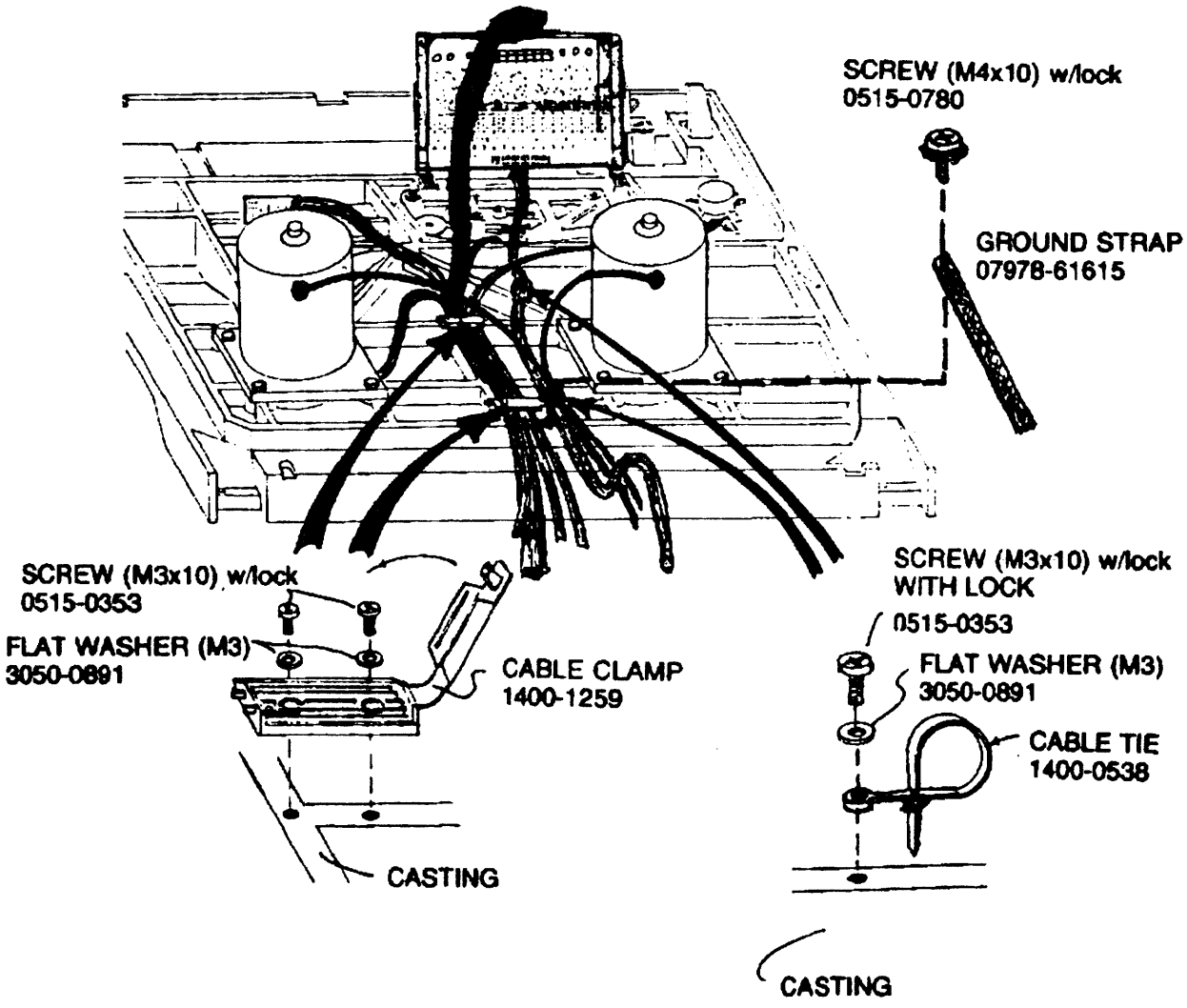


Figure (6) 1-8 Cable Clamping

REPLACEMENT

1. Insert takeup reel hub through casting. Align motor mount holes. Motor power cable must be on top when motor/takeup reel assembly is placed into position.

2. While supporting motor, insert top two M8x25 bolts and 5/16" helical washers. Finger tighten.

3. Insert bottom two M8x25 bolts and 5/16" helical washers. Finger tighten.

4. Use adjustable wrench to firmly tighten all four motor mount bolts.

5. Install power cable connection on left upright connector on Motor Driver Assembly (A2).

6. Route power cable to left tie-wrap point on the back of the casting (see drawing) and tie wrap cable to the supply motor power cable and the Tape Head Assembly cable. Screw tie-wrap to casting with M3x10 lockwasher and flatwasher.

NOTE

If replacing the plastic takeup reel, remove the write enable ring from new assembly before installing.

7. Install takeup reel with clear plastic side facing out.

8. Ensure "O" ring is in groove on the back of the fixed reel cover. Install fixed reel cover with 3 M4x8 Allen screws and lockwashers.

1.4 BUFFER ASSEMBLY

REMOVAL

1. Open the two ribbon cable clamps on the back of the casting, the two clamps on the right front side of the chassis, and the one clamp on the lower left front of the chassis.

CAUTION

Use the extractor tabs to release edge connectors from the edge connector receptacles. When the tabs are spread, the edge connector is released and partially raised. To fully remove the connector, grasp the body of the connector, *not the wires*, and pull.

2. Remove the ribbon cable connector from the receptacle third from the bottom on the Servo Controller Assembly (A1).

3. Use #2 Posidriv to remove three screws which hold the Buffer Assembly casting to the main, tape path casting. *Do not loosen or remove the screws holding the sensor housing and PC board to the Buffer Assembly casting.*

WARNING

The Buffer Assembly could catch on the ribbon cable coming from the Preamplifier PC board and be pulled from your hand. Be sure this cable is cleared when withdrawing the assembly from the casting.

CAUTION

Use care when removing the Buffer Assembly (A13). The tape guides are easily caught on the edge of the hole in the casting and could be thrown out of alignment.

4. Withdraw Buffer Assembly from the casting.

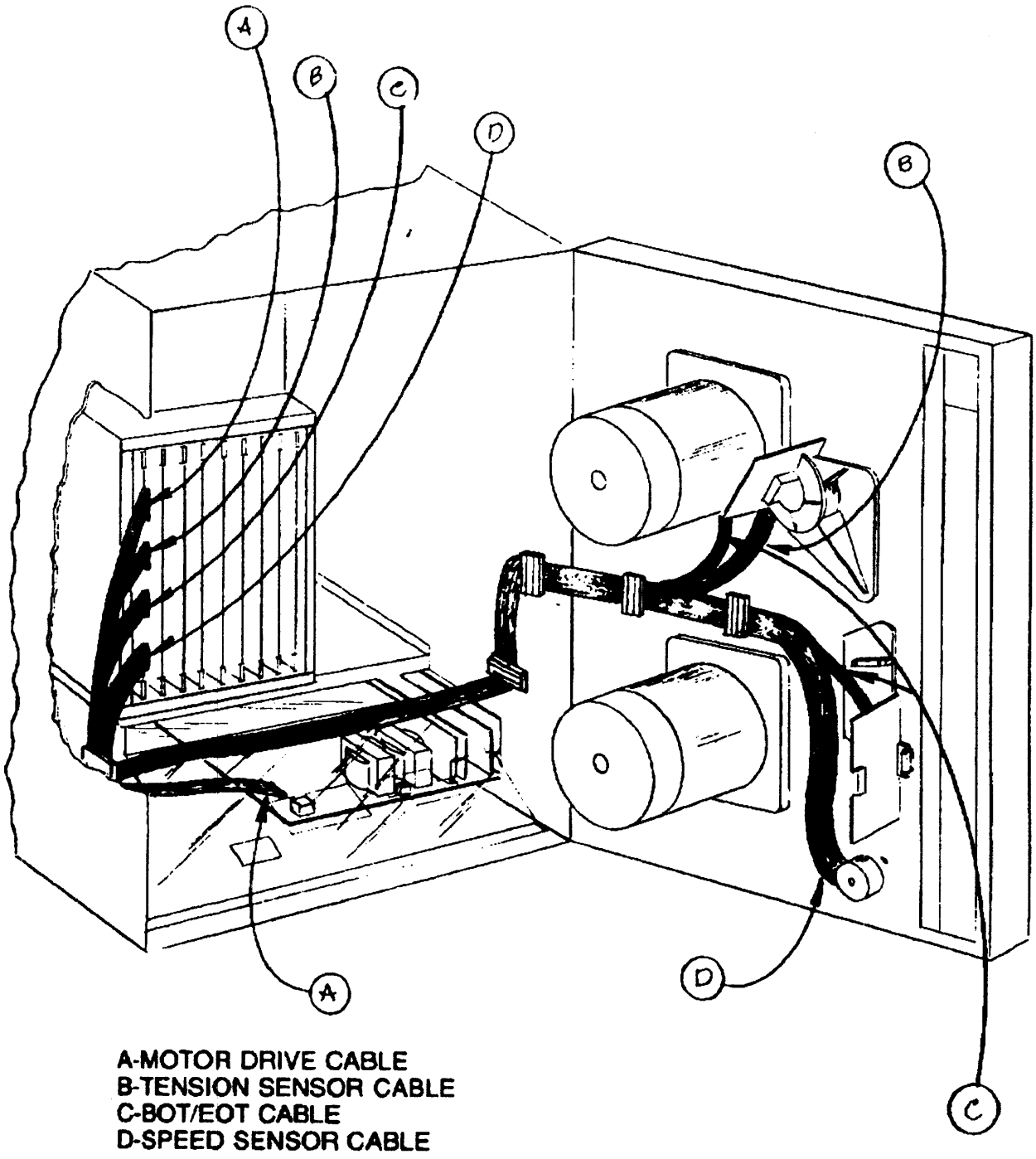


Figure (6) 1-9 Control Cables

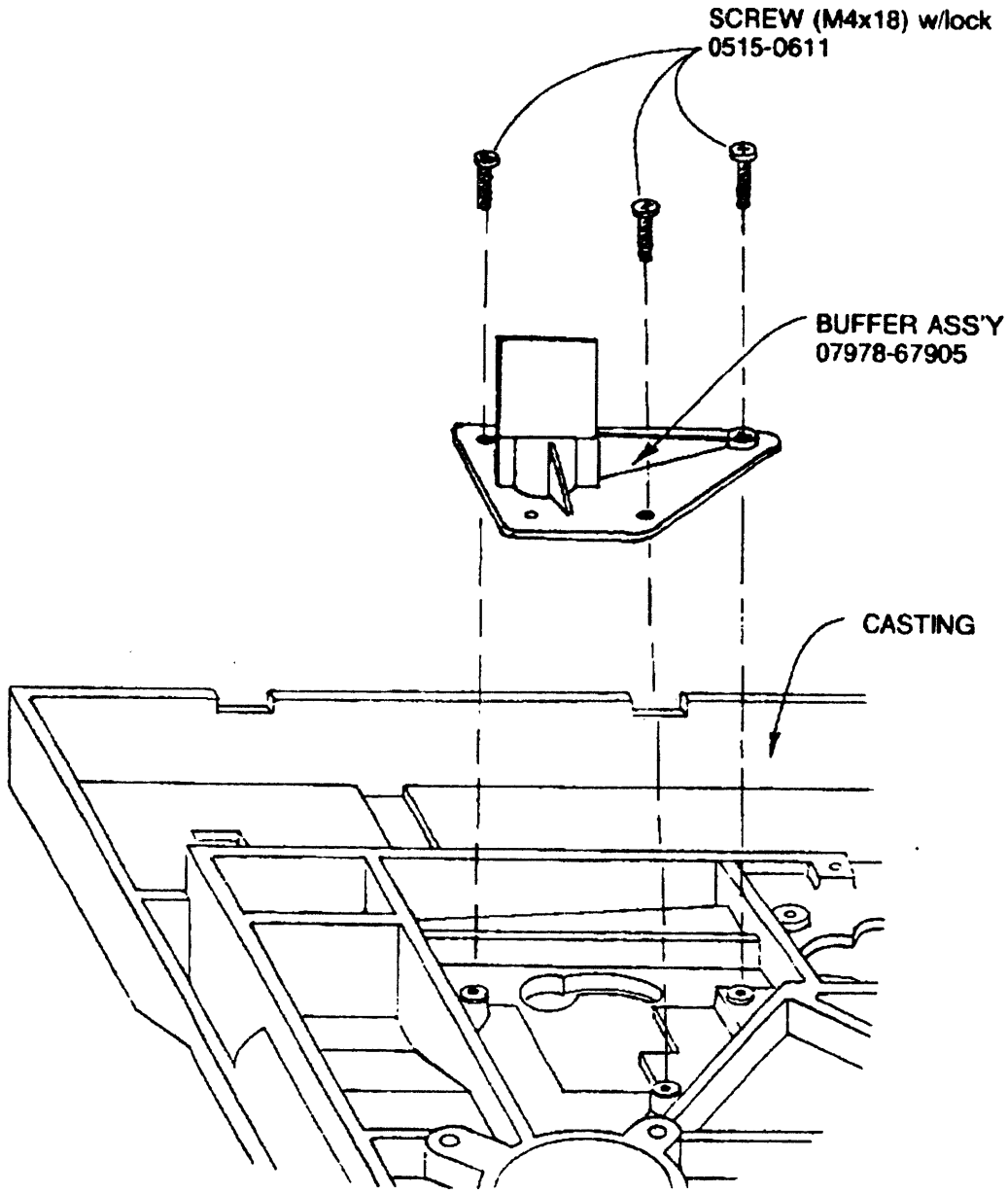


Figure (6) 1-10 Tension Sensor Assembly

REPLACEMENT

1. Insert the tape guides into the holes in the main casting and align mounting holes.

CAUTION

Be sure that the ribbon cable that comes from the Front Panel is not caught behind the the Tension Sensor casting.

2. Insert three mounting screws with #2 Posidriv. Tighten screws.

3. Move the Buffer arm by hand and check that the arm moves freely from limit to limit.

4. Route edge connector behind the Supply Motor power cable.

5. Bring ribbon cable directly down to the right cable clamp on the back of the casting. Clamp the cable.

6. Lay the cable over to the left cable clamp on the back of the casting. Clamp the cable.

7. Route the cable off the casting over to the top cable clamp on the right front side of the chassis. Swing casting all the way open to assure that cable has enough play, and clamp cable.

8. Route cable down to bottom clamp. Clamp cable.

9. Route cable across top of plastic shield over Motor Driver Assembly. Clamp cable in clamp on left side of chassis.

10. Connect cable to edge connector third from the bottom on the Servo Controller Assembly (A1).

1.5 SPEED ENCODER

REMOVAL

1. Open the two ribbon cable clamps on the back of the casting, the two clamps on the right front side of the chassis, and the one clamp on the lower left front of the chassis.

2. Remove the ribbon cable connector from the receptacle in the bottom position on the Servo Controller Assembly (A 1).

3. Loosen the three screws on the three holddown lugs. Use a #2 Posidriv.

4. While holding the Speed Encoder, rotate the three holddown lugs out of the groove around the circumference of the encoder case.

CAUTION

Use care when pulling the Speed Encoder roller through the casting.

5. Withdraw the Speed Encoder from the casting.

6. Carefully pull Speed Encoder ribbon cable from among the other cables until cable is completely free of chassis.

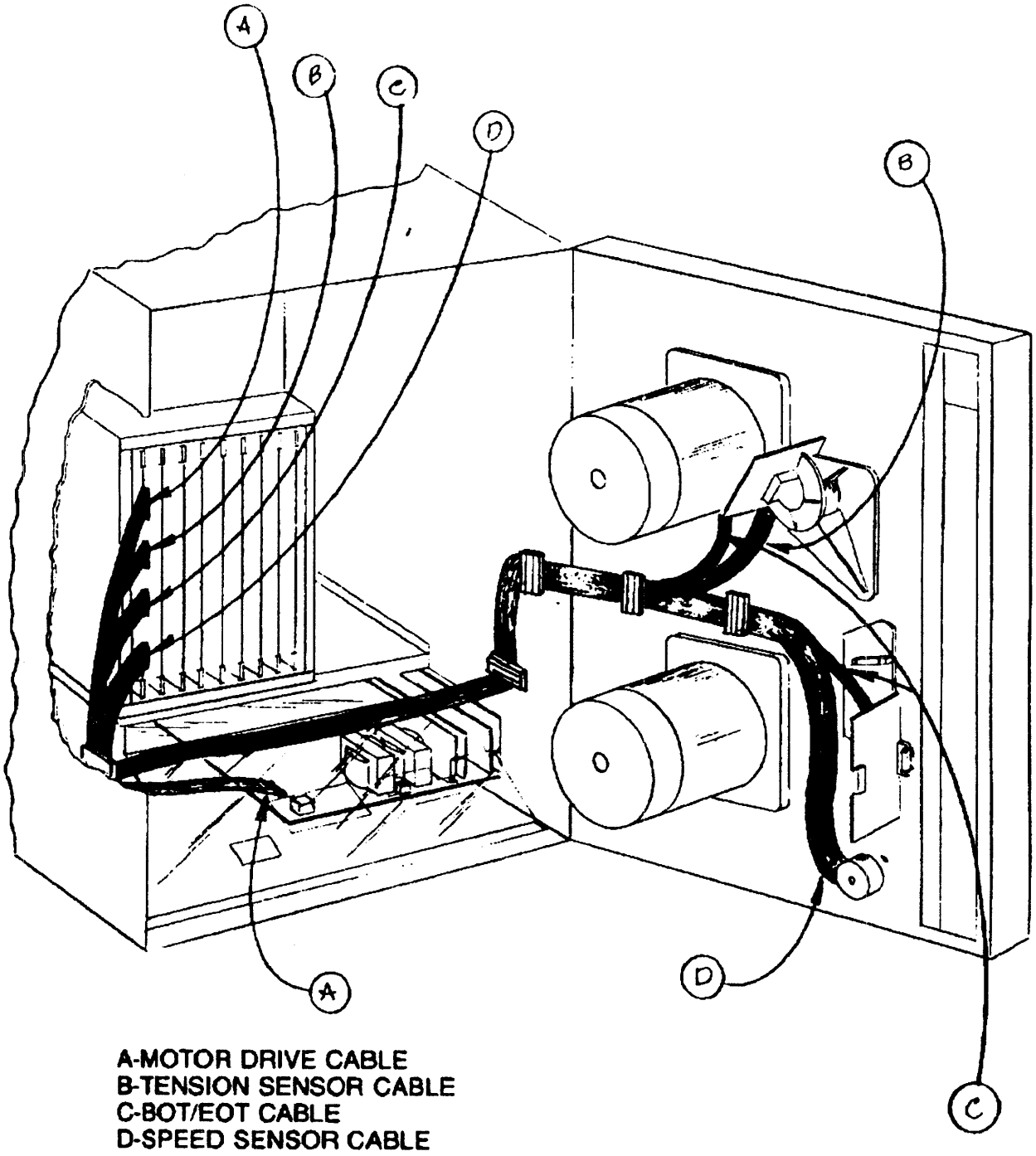


Figure (6) 1-11 Control Cables

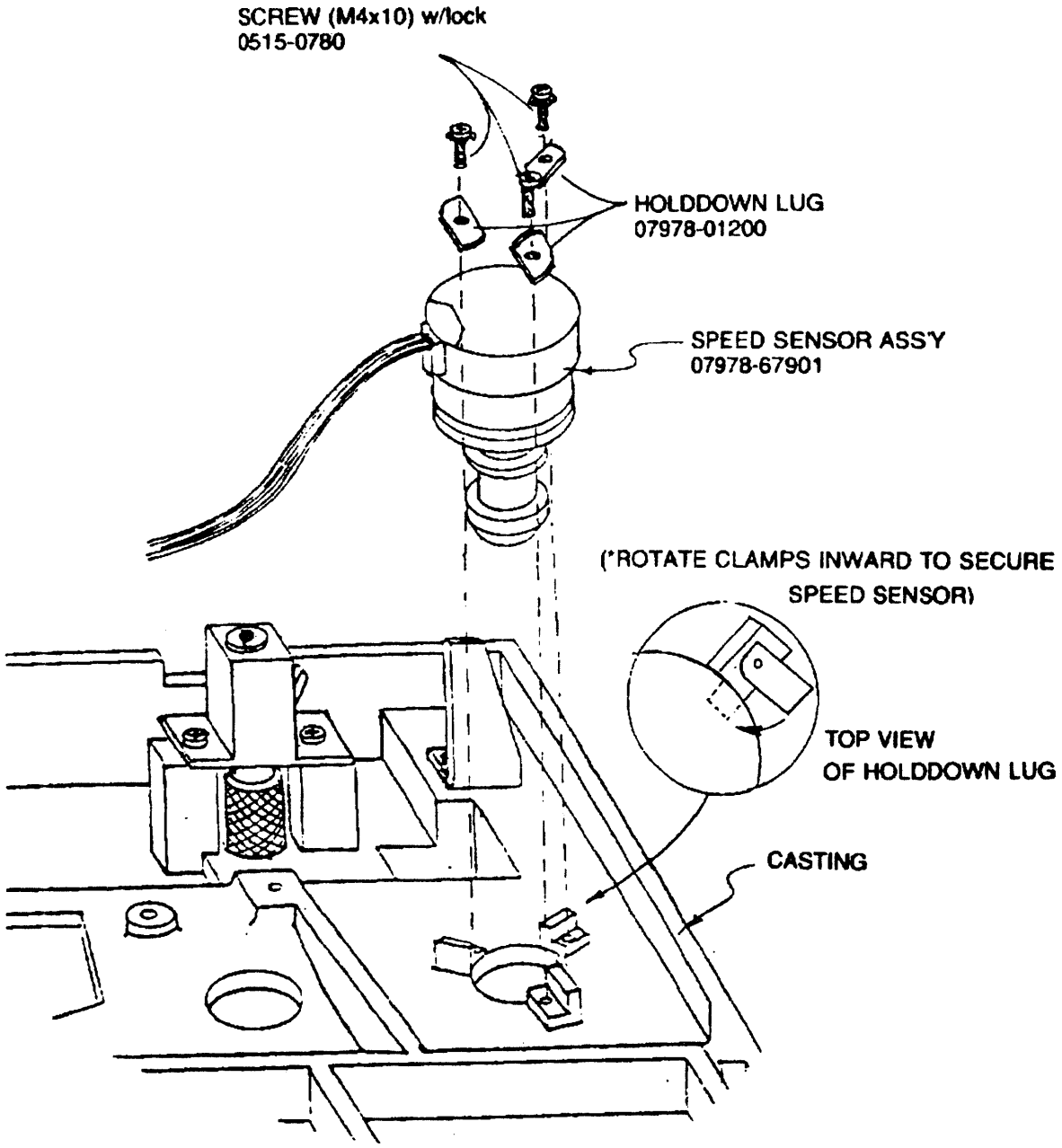


Figure (6) 1-12 Speed Sensor Assembly

REPLACEMENT

CAUTION

Use care when pushing the Speed Encoder roller through the casting.

1. Insert Speed Encoder in the casting. Ribbon cable from the case should exit from the left at about the 11 c'clock position.

2. Rotate the three holddown lugs into the groove around the circumference of the encoder case. Tighten the lugs in place with a #2 Posidriv.

3. Manually rotate the Speed Encoder roller. There should be no binding.

4. Route edge connector behind the Supply Motor power cable.

5. Bring ribbon cable directly down to the right cable clamp on the back of the casting. Clamp the cable.

6. Lay the cable over to the left cable clamp on the back of the casting. Clamp the cable.

7. Route the cable off the casting over to the top cable clamp on the right front side of the chassis. Swing casting all the way open to assure that cable has enough play, and clamp cable.

8. Route cable down to bottom clamp. Clamp cable.

9. Route cable across top of plastic shield over Motor Driver Assembly. Clamp cable in clamp on left side of chassis.

10. Attach ribbon cable to bottom connector on the Servo Controller Assembly (A1).

1.6 PREAMPLIFIER ASSEMBLY (A12)

REMOVAL

1. Remove ribbon edge connector from the outboard edge connector on the Preamplfier PC board.

2. Remove the cable going to the Tape Head Assembly (A11).

3. Use M3 nut driver to remove the four nuts holding the preamplifier PC board to the mounting brackets. Support the PC board when removing the nuts. Remove PC board, M3x10 lockscrews, and M3 washers.

REPLACEMENT

1. Hold the Tape Head Assembly cable against the casting behind the control panel so that when the PC board is moved into position on the mounting bracket, the connector is on the right (IC) side of the board.

2. Position the Preamplifier PC board on the left side of the bracket. The IC side of the board faces to the right. The Tape Head Assembly cable should be on the right (IC) side of the PC board (from Step 1).

3. Insert four M3x10 lockscrews with washers through the PC board and the brackets from the bracket side. Apply and tighten the nuts starting with the top bracket.

4. Connect ribbon cable to outboard edge connector (farthest from the casting).

5. Connect the Tape Head Assembly cable to inboard connector (nearest the casting).

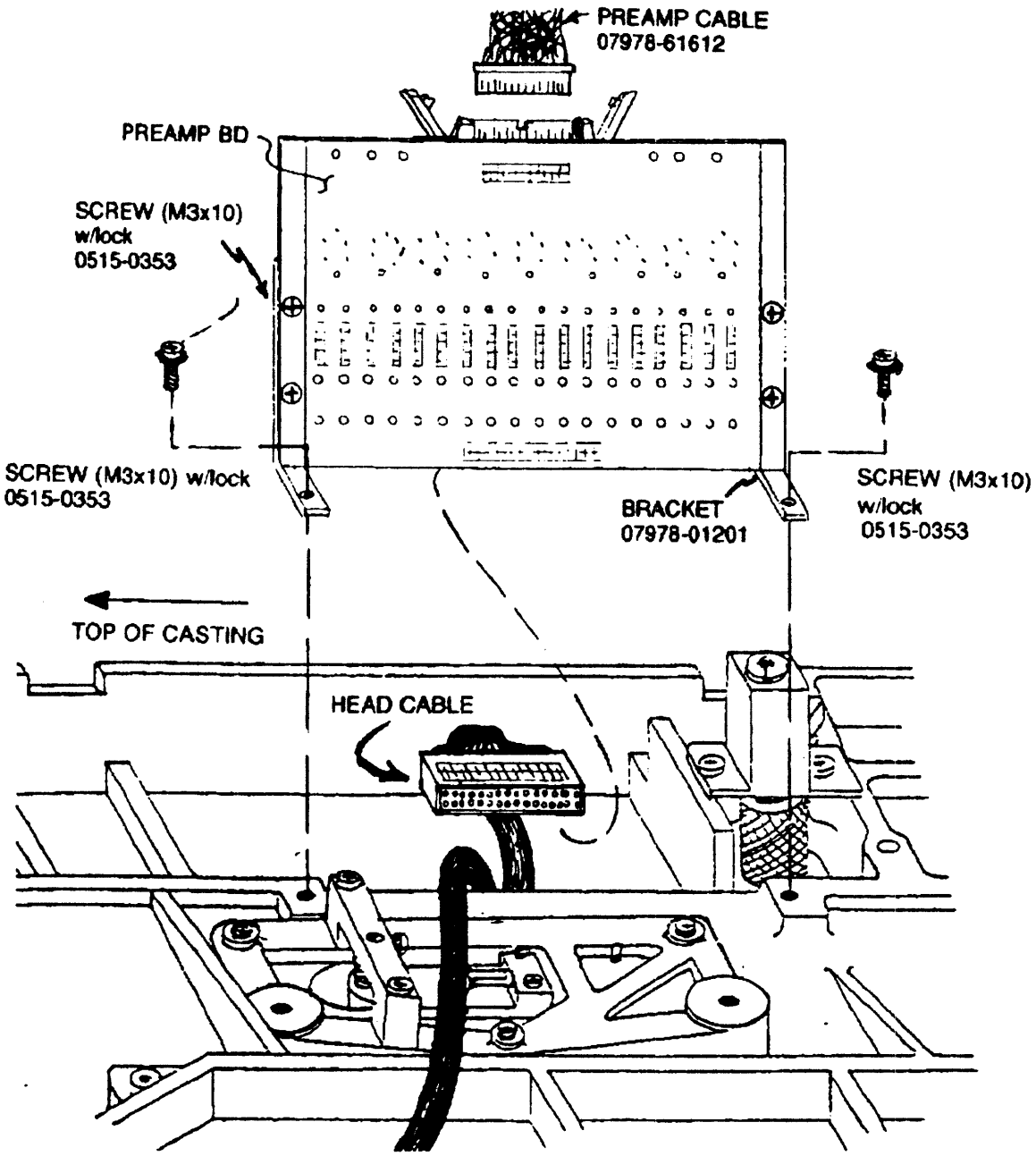


Figure (6) 1-13 Preamplifier Assembly

1.7 TAPE HEAD ASSEMBLY

REMOVAL

1. Remove braided ribbon cable from the Preamplifier PC board (A12) outboard connector (farthest from casting).

2. Remove the Tape Head Assembly cable from the Preamplifier PC board (A12) inboard connector (nearest the casting).

3. Remove Tape Head Assembly cable from connector on Write Assembly (A7). (Round cable).

CAUTION

If casting is swung towards the closed position to remove the BOT/EOT sensor as called for in the next step, be careful that the Tape Head Assembly cable just released does not get caught between the casting and the lower edge of the chassis.

4. Use an Allen wrench to remove M4x40 screw and lockwasher holding BOT/EOT sensor to the front of the Tape Head Assembly (A11).

5. Use a #2 Posidriv to remove the three screws on the back of the Tape Head Assembly.

6. Carefully withdraw the Tape Head Assembly (A11) from the casting. Leave the BOT/EOT sensor assembly hanging on the front of the casting. Manueuver the assembly away from the casting so that no damage is done to the cabling, tape head, or guides.

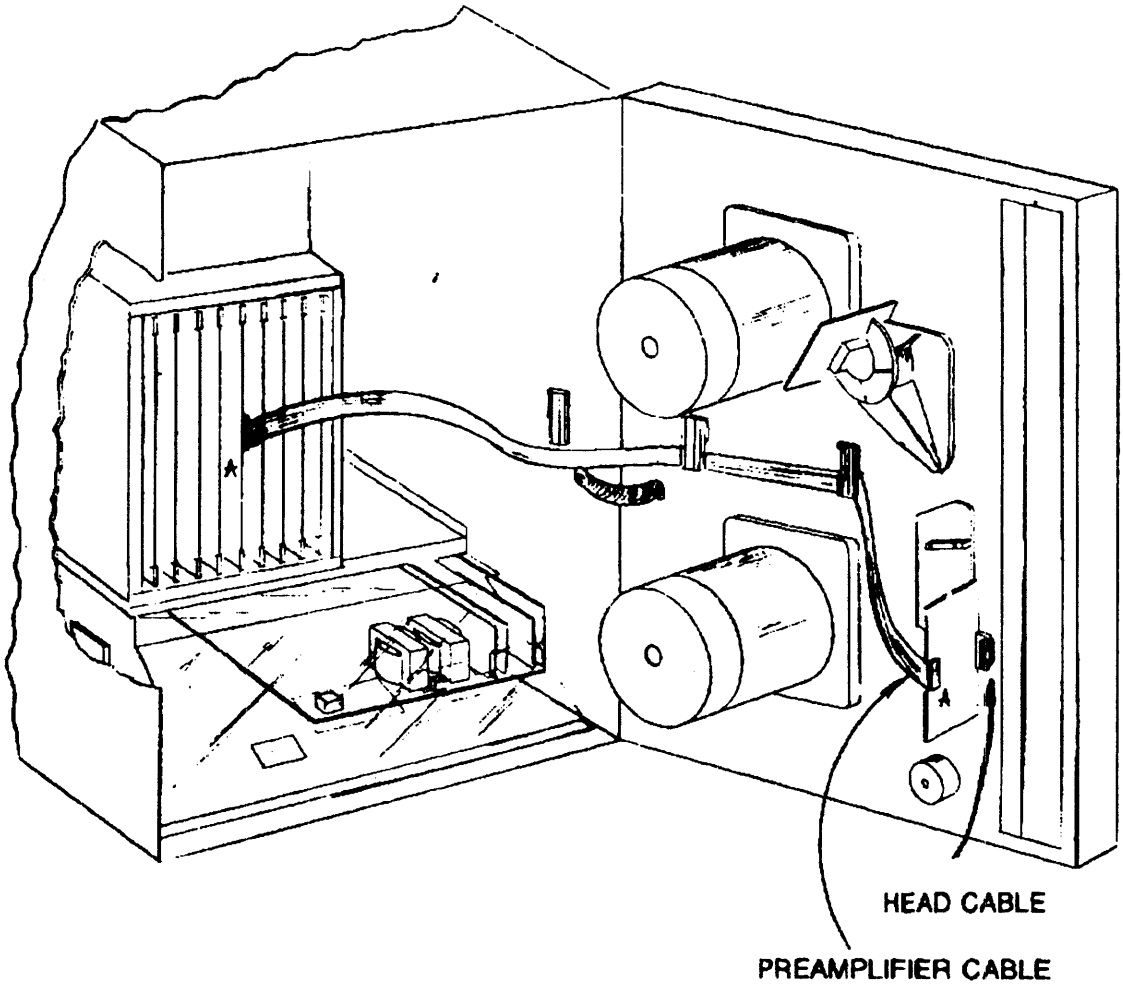


Figure (6) 1-14 Preamplifier Cable

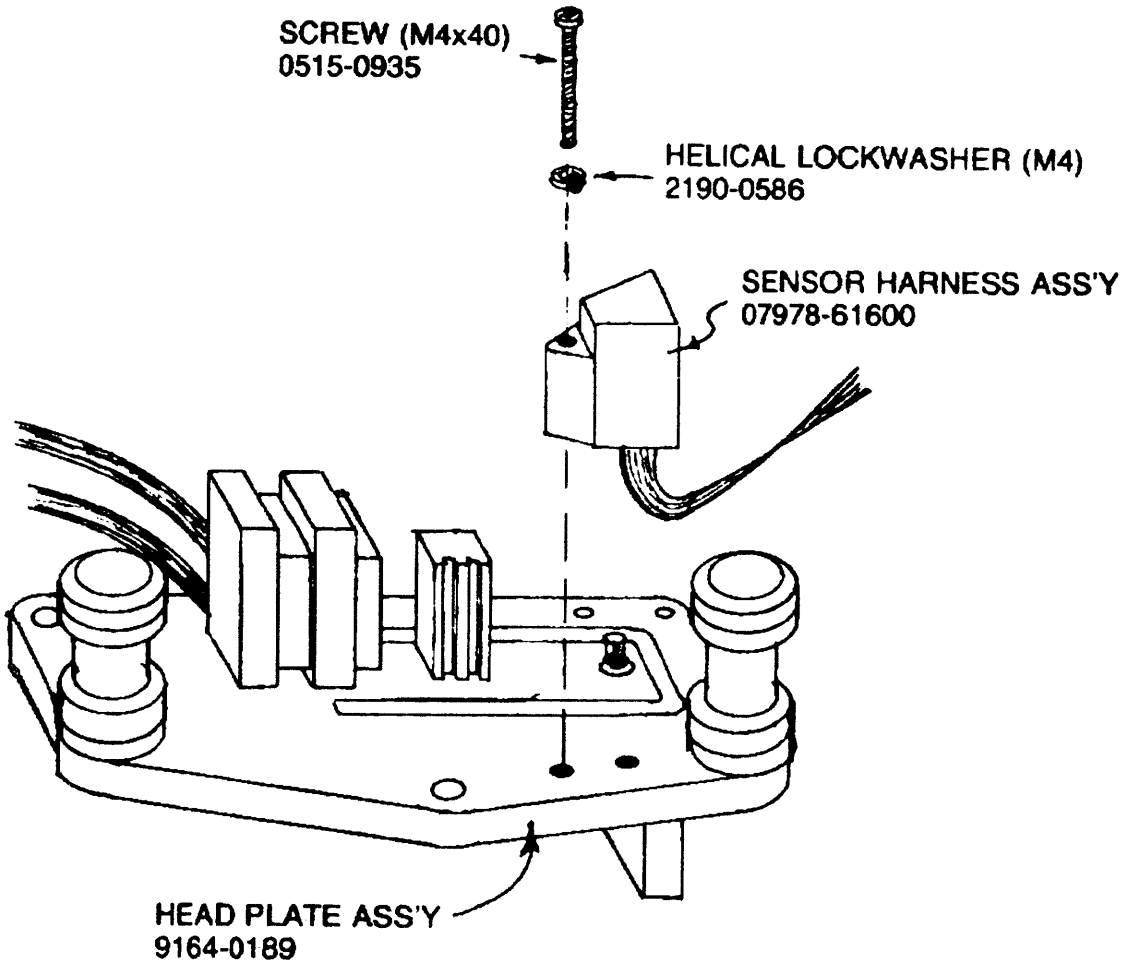


Figure (6) 1-15 Sensor Harness Assembly

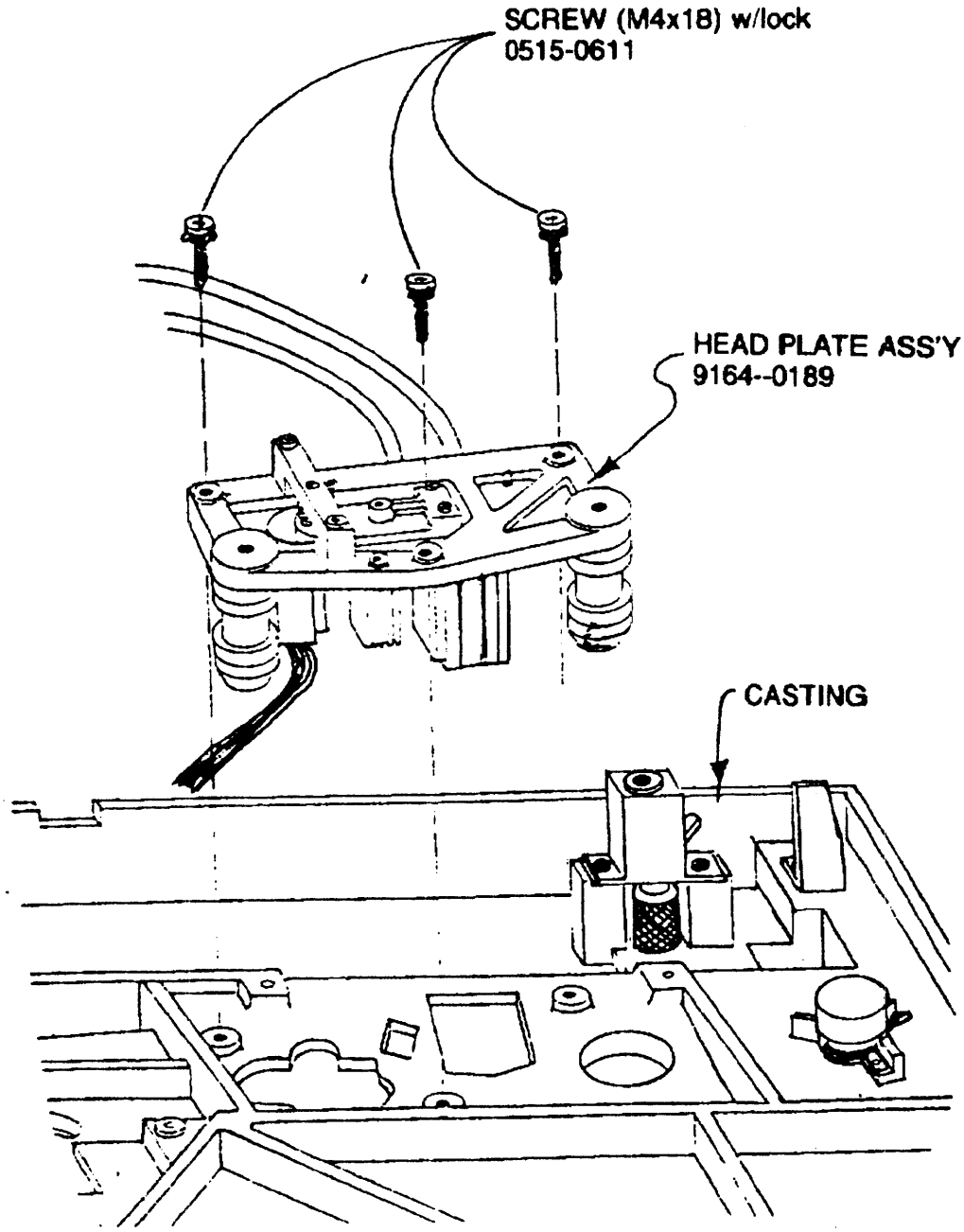


Figure (6) 1-16 Head Plate Assembly

REPLACEMENT

1. As Tape Head Assembly is brought close to the casting, route the short Tape Head cable from the assembly through the space between the Preamplifier PC board and the casting. Bring the Tape Head Assembly into position over the mounting holes.

2. Insert and use #2 Posidriv to tighten the three screws that hold the Tape Head Assembly to the casting.

3. Connect the Tape Head Assembly cable to the inboard connector (closest to the casting) on the Preamplifier PC board.

4. Lay the write cable against the back of the casting and attach the cable with a tie-wrap to the tie point on the right middle of the casting with a M3x10 lockscrew and flatwasher.

5. Route the write cable over to the left tie wrap point behind the casting. Combine the write cable with the two motor power cables, tie wrap and attach to the left tie wrap point with a M3x10 lockscrew and flatwasher.

6. Connect the the write cable to the edge connector on the Write Assembly board (A7).

7. Slowly swing casting to full open position and check that the write cable does not exert any pulling pressure on the Write Assembly (A7).

8. Connect braided ribbon cable to Preamplifier PC board outboard edge connector (farthest from the casting).

9. Use M4x40 Allen screw to fasten BOT/EOT sensor assembly to front of Tape Head Assembly.

1.8 SENSOR HARNESS ASSEMBLY

REMOVAL

1. Remove the M3x10 Allen screw and washers on the write enable ring sensor underneath the Supply Motor. Dismount the write enable ring sensor.

NOTE

If the sensor screw is tight, it may be necessary to remove the Supply Motor to remove the sensor. See removal procedures for "SUPPLY REEL MOTOR AND HUB", this Section.

2. Open the two cable clamps on the rear of the casting, the two cable clamps on the right front side of the chassis, and the cable clamp on the left front side of the chassis.

3. Remove the ribbon cable connector located second from the bottom on the edge of the Servo Controller Assembly (A1).

4. Unthread the ribbon cable from the cables in the rear of the casting.

5. Remove the M4x40 Allen screw from the front of the BOT/EOT Sensor Assembly.

6. Withdraw Sensor Assembly from the front of the casting; pulling the ribbon cable and connector through the casting.

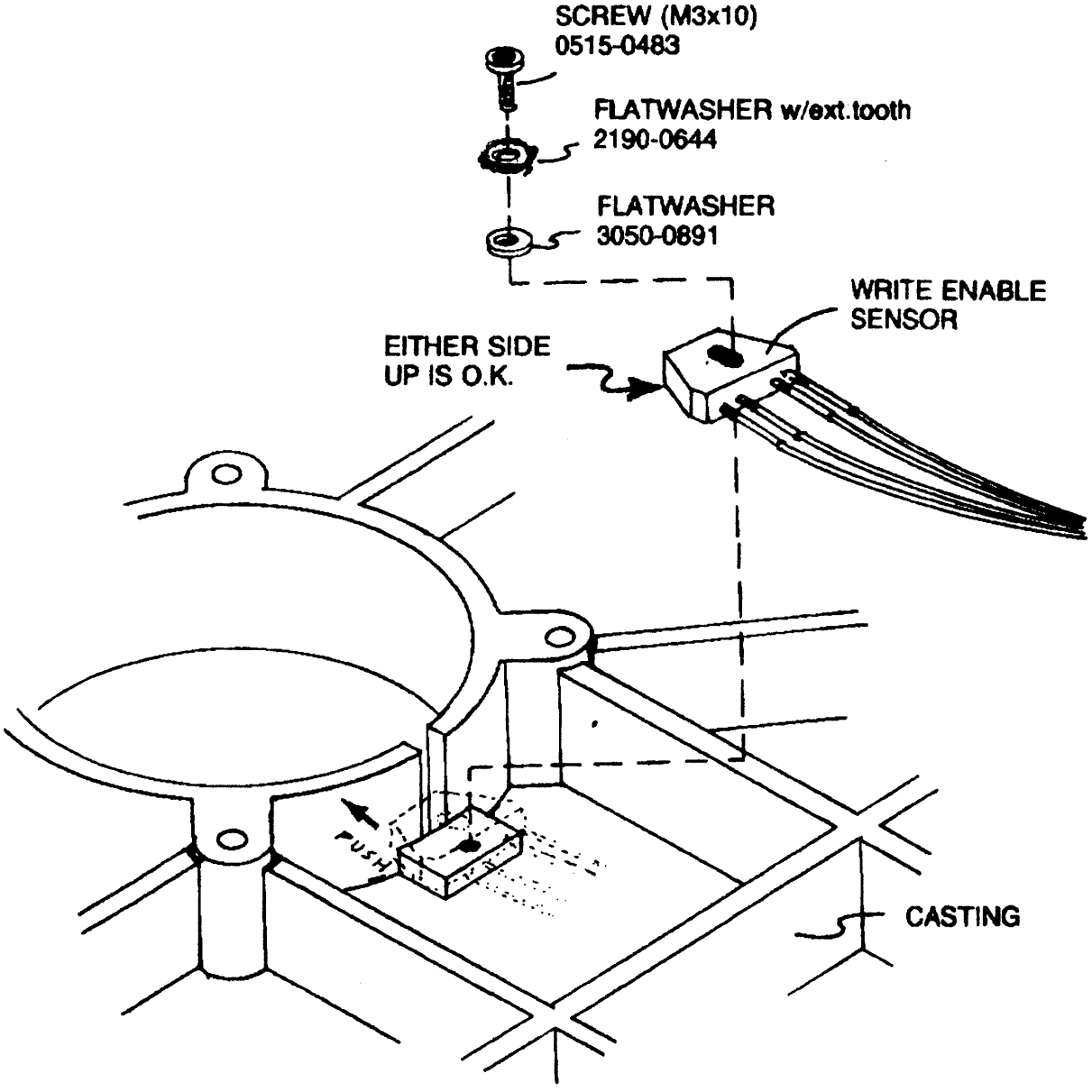


Figure (6) 1-17 Write Enable Sensor

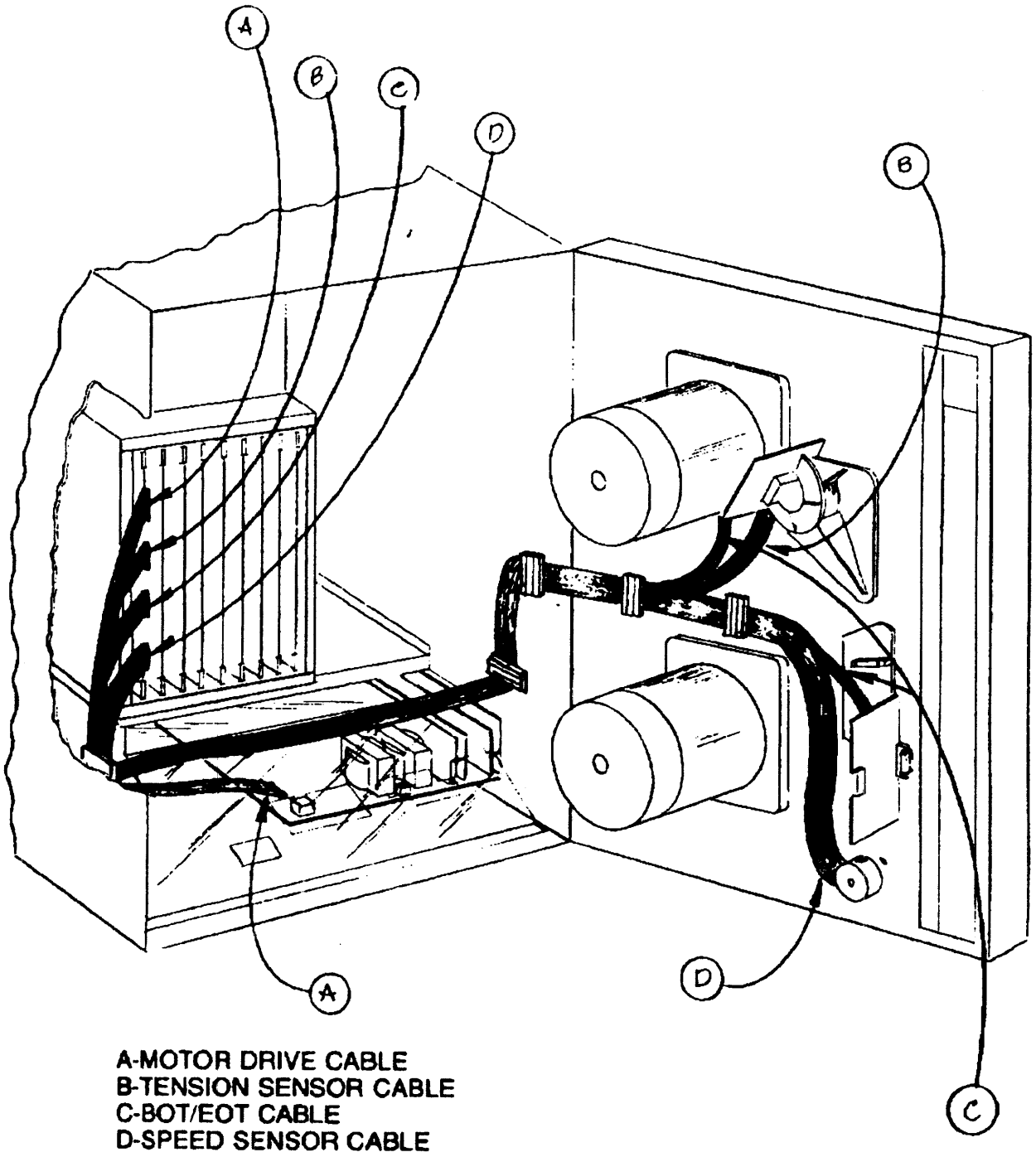


Figure (6) 1-18 Control Cables

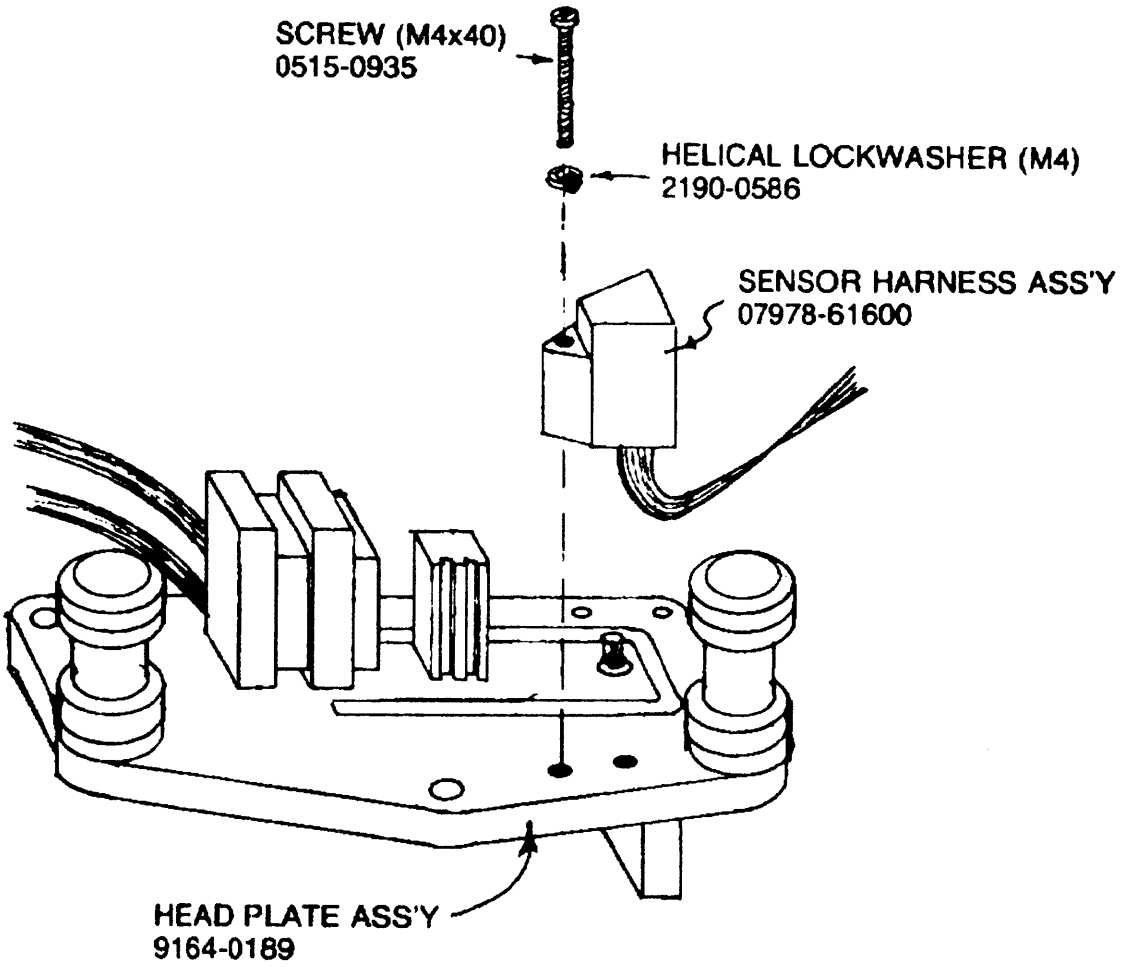


Figure (6) 1-19 Sensor Harness Assembly

REPLACEMENT

CAUTION

Be careful of the write enable ring sensor as the ribbon cable is threaded through the casting in the next step.

1. Thread the edge connector and ribbon cable through the casting from the front.

2. Secure the BOT/EOT Assembly with the M4x40 Allen screw and lockwasher. The plastic pin on the middle bottom of the assembly will help position the assembly against the head plate assembly. The pin will slip into a hole just above the hole where the Allen screw goes in.

3. Route the ribbon cable through the right cable clamp on the back of the casting. Clamp the cable.

4. Route the ribbon cable behind the Supply Motor power cable and through the left cable clamp on the back of the casting. Remove slack and clamp the cable.

5. Use M3x10 Allen screw and washer to attach the write enable ring sensor underneath the Supply Motor. Push the sensor in a radial direction against the machined stop in the casting while tightening the screw.

6. Route the ribbon cable from the left clamp on the back of the casting to the top clamp on the right front side of the chassis. Swing the casting to its full open position, lay the cable straight across to the clamp and fasten the clamp. When the casting is in the open position, there should be no pulling force on the ribbon cable.

7. Route ribbon cable down to the lower clamp on the right side of the chassis. Clamp the cable.

8. Route ribbon cable across the top of the plastic shield over the Motor Driver Assembly (A2) to the cable clamp on the lower left side of the chassis. Clamp the cable.

9. Route ribbon cable up to the edge connector which is second from the bottom on the Servo Controller Assembly (A1). Connect cable.

1.9 FRONT PANEL

REMOVAL

1. Use a #1 Posidriv to remove the lower two, then the upper two, M3x20 screws and washers holding the upper decorative panel. Hold the panel when removing the last screw to prevent the panel from falling to the floor.

2. Remove the bottom M3x10 screws from the Front Panel Assembly PC board just below the control buttons. Remove the same type screw from the middle of the PC board just above the control buttons.

3. Unhook the Front Panel cable from the Front Panel PC Assembly by pressing down on the release ears on the connector.

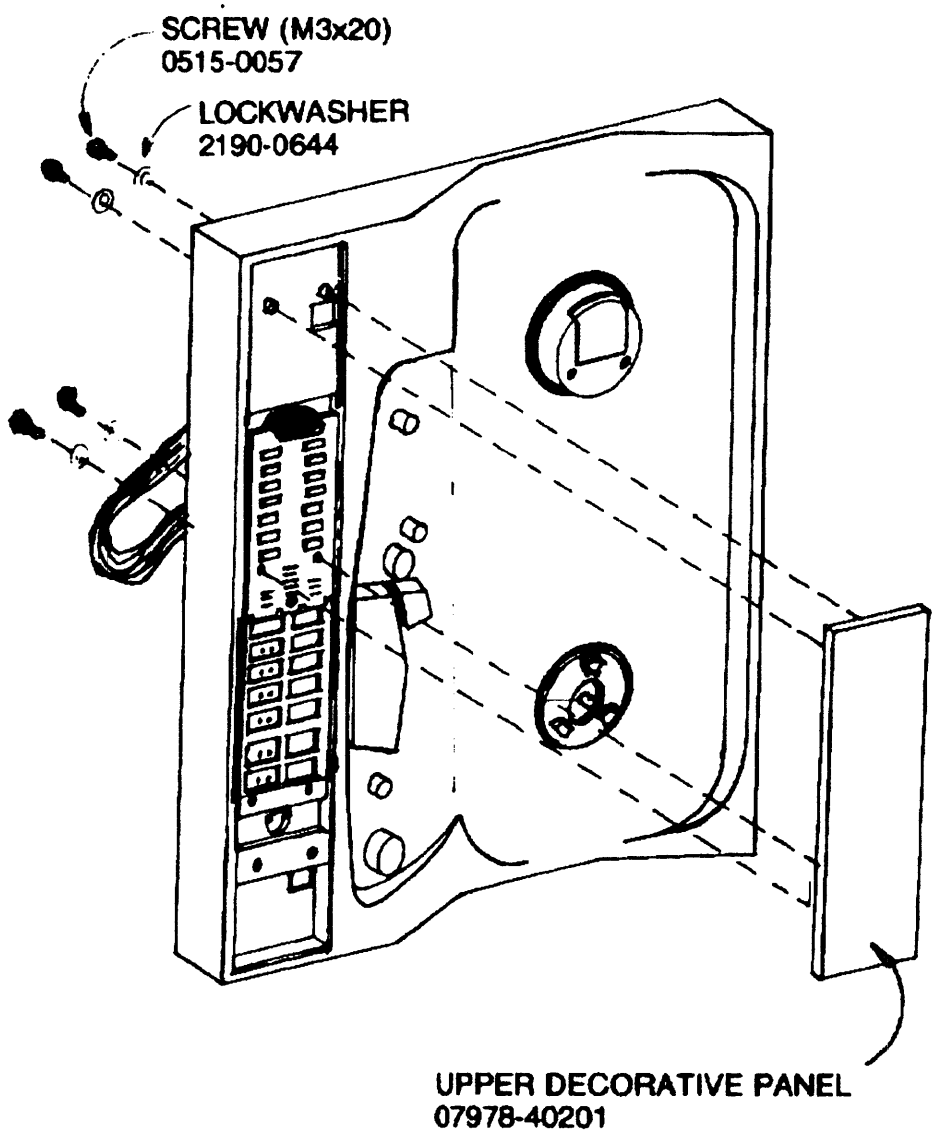


Figure (6) 1-20 Front Panel Access

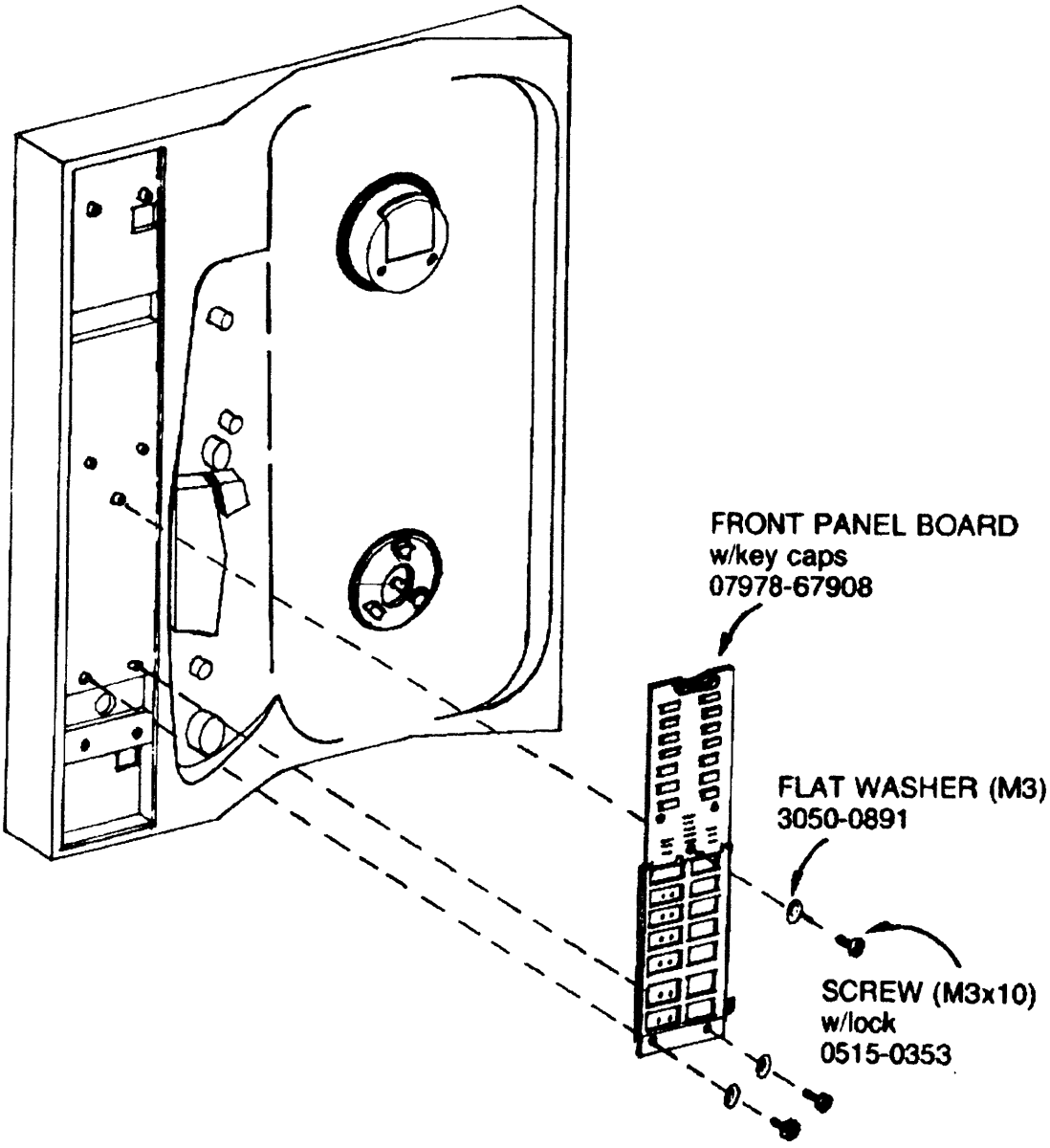


Figure (6) 1-21 Front Panel PC Board

REPLACEMENT

1. Position Front Panel PC board over mounting holes and insert M3x10 screw and flatwasher in the middle mounting hole just above the control buttons. Start the screw but do not tighten.

2. Insert two M3x10mm screws and washers in the bottom mounting holes (below the buttons).

3. Tighten the three screws.

4. Pull connector through the hole in the casting and connect to the Front Panel PC board by pushing down into the header until the connector ears snap into place.

5. Position the top decorative panel (logo on the top) and start the top two M3x20 screws and washers.

6. Start the two bottom M3x20 screws and washers holding the panel.

7. Tighten the four screws.

1.10 MISCELLANEOUS- CASTING

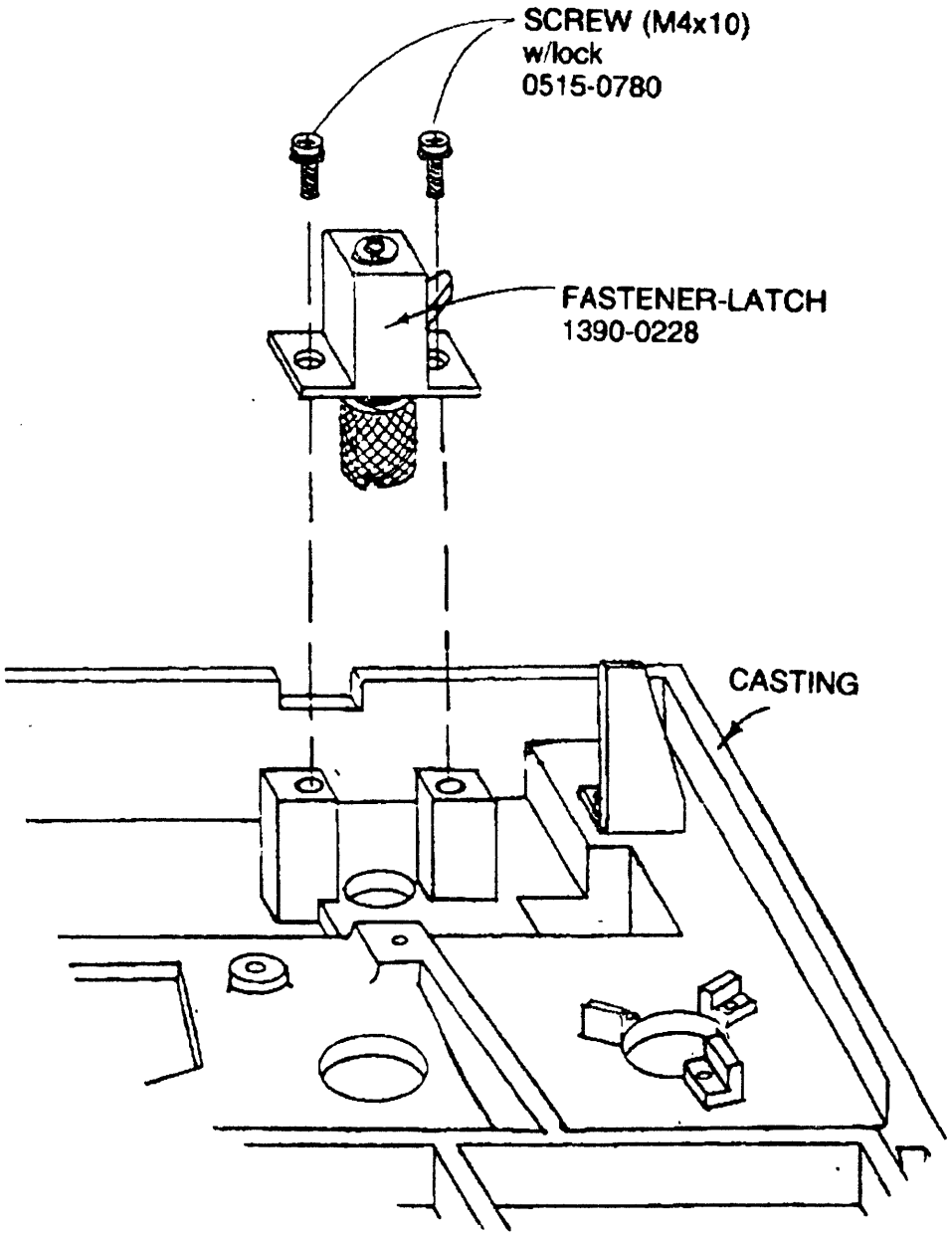


Figure (6) 1-22 Casting Fastener-Latch

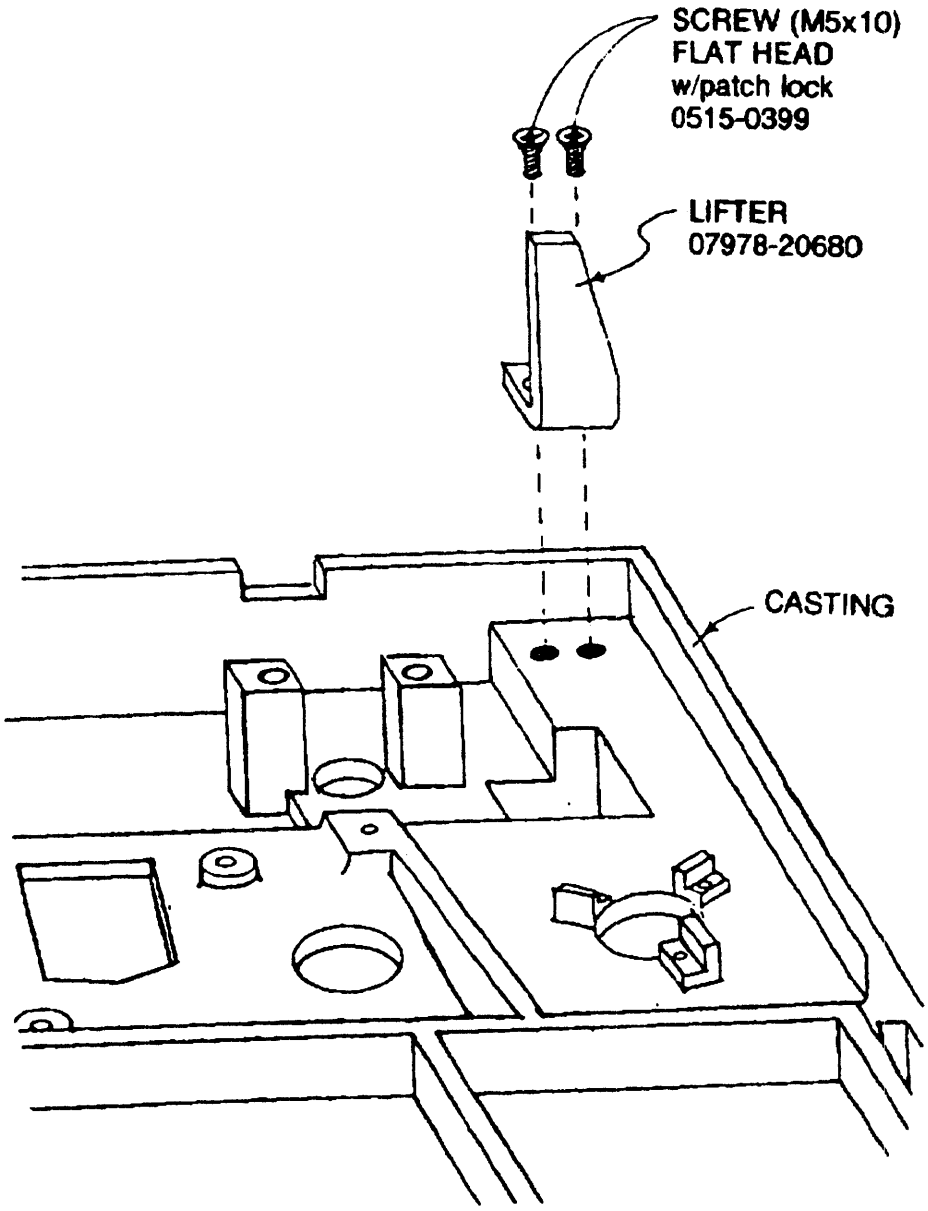


Figure (6) 1-23 Casting Lifter

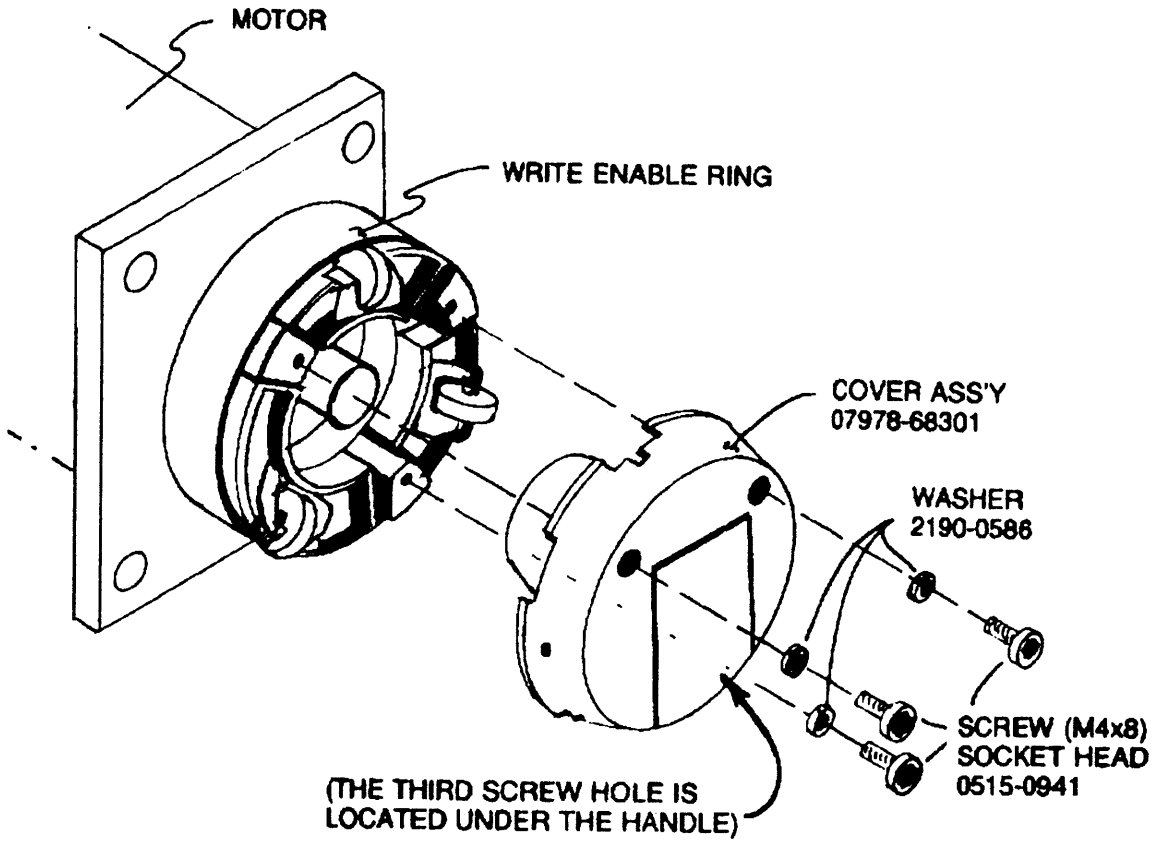


Figure (6) 1-24 Supply Reel Hub (Internal-1)

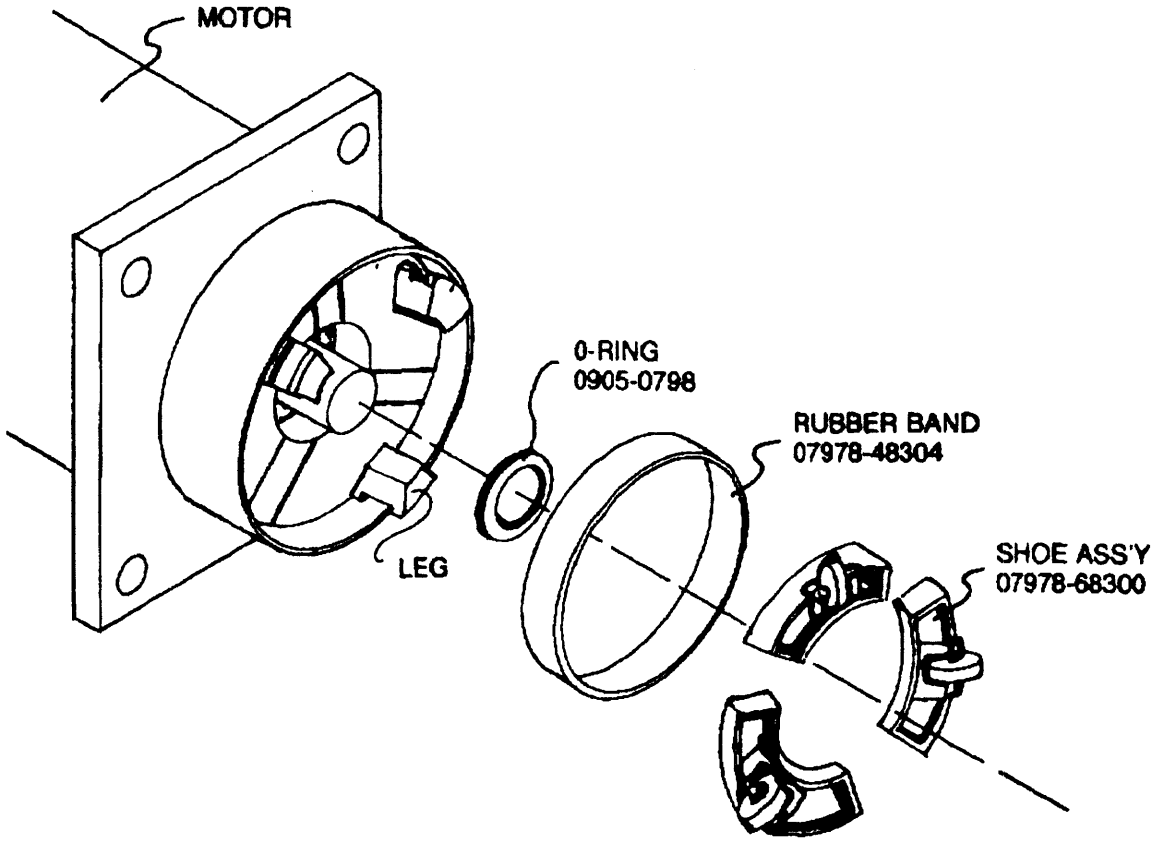


Figure (6) 1-25 Supply Reel Hub (Internal-2)

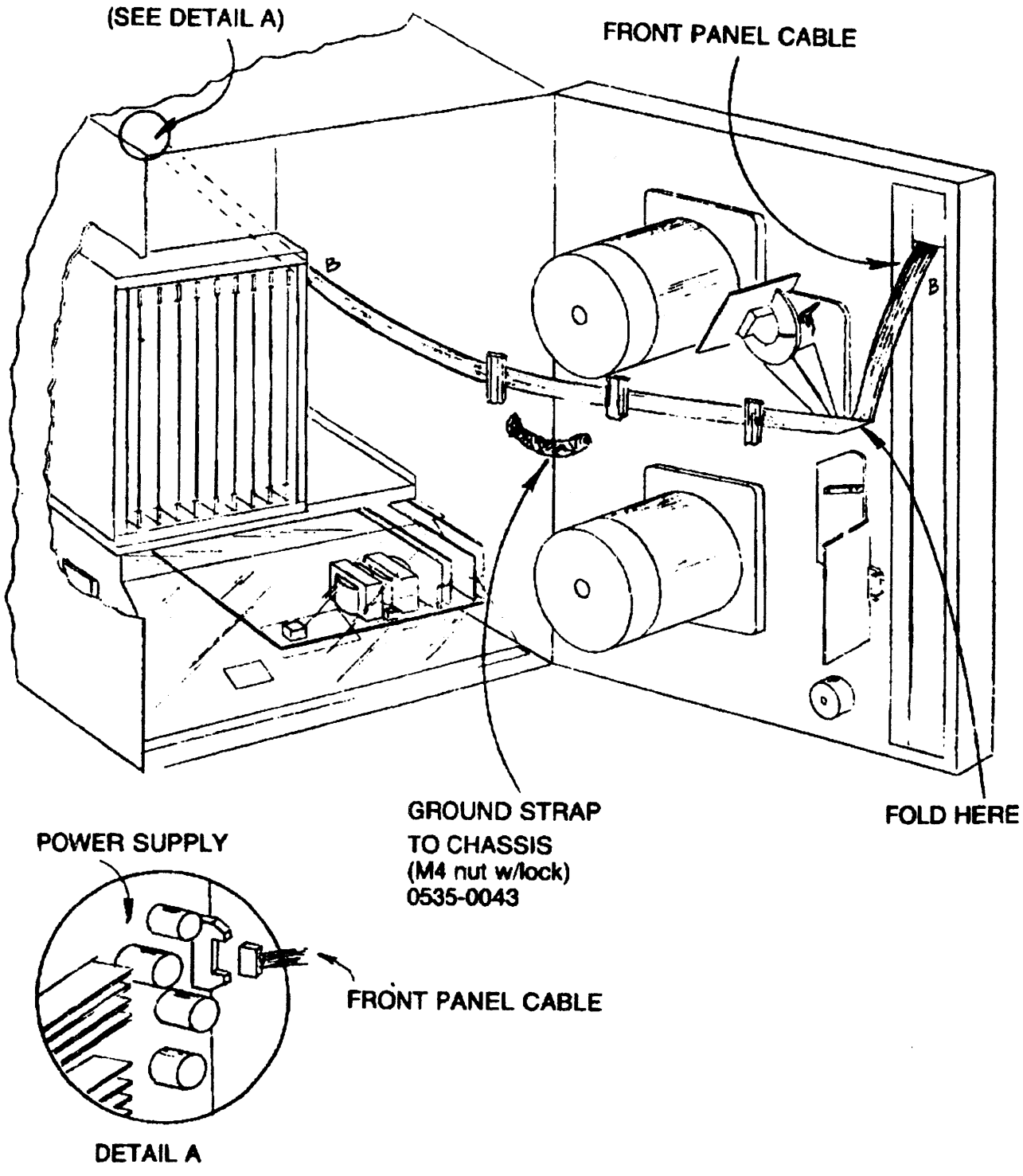


Figure (6) 1-26 Front Panel Cable

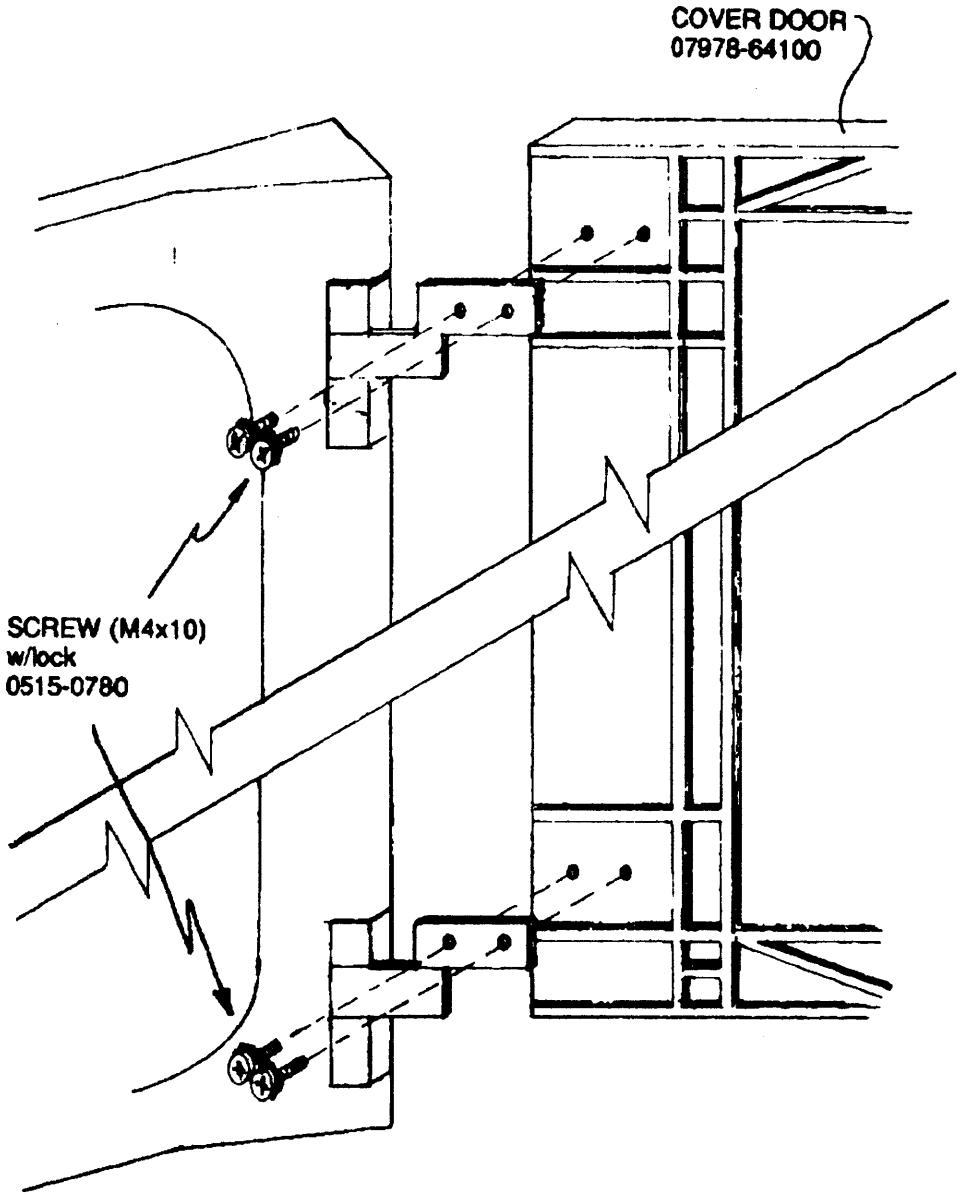


Figure (6) 1-27 Tape Path Door

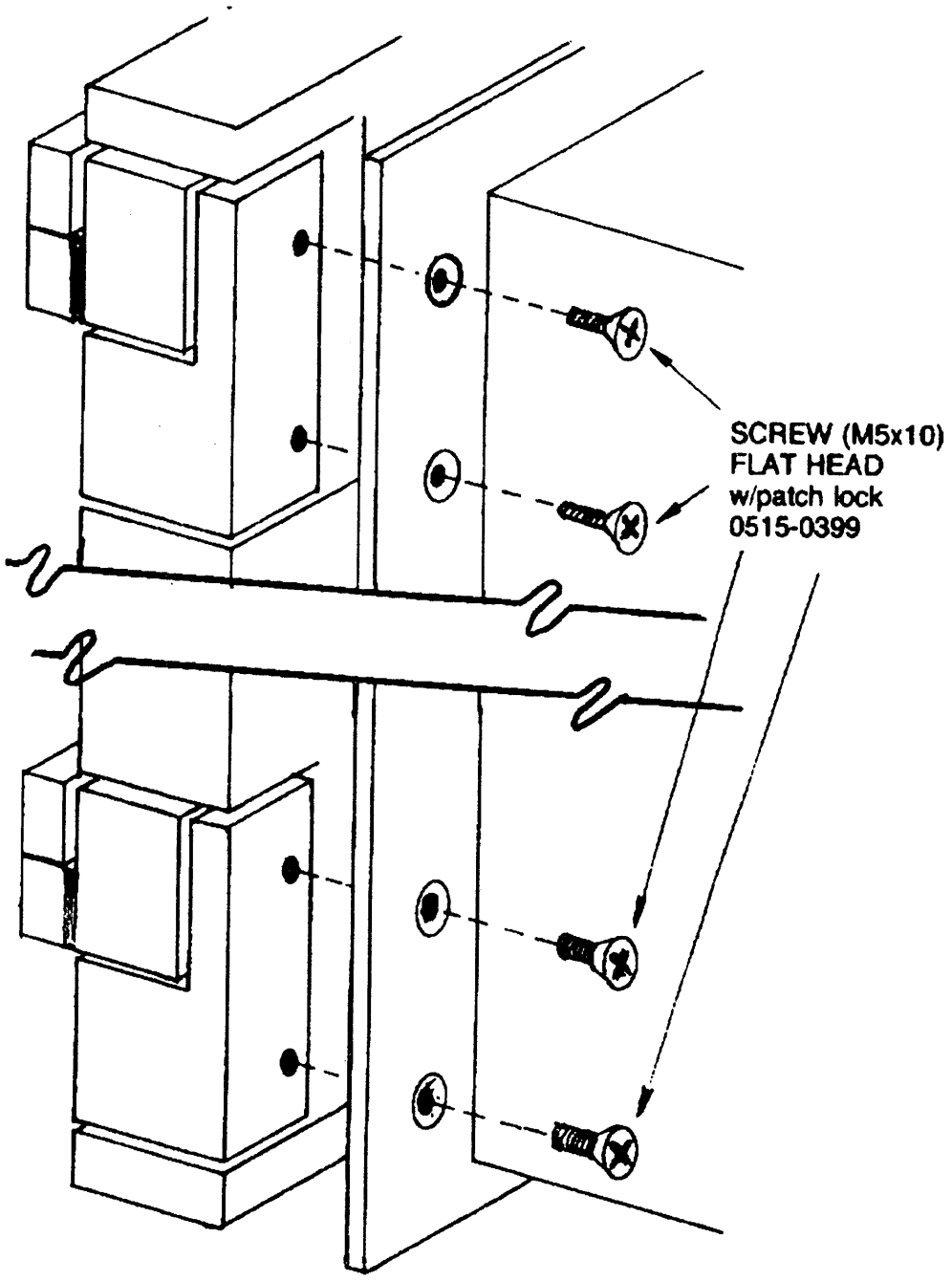


Figure (6) 1-28 Casting Screws

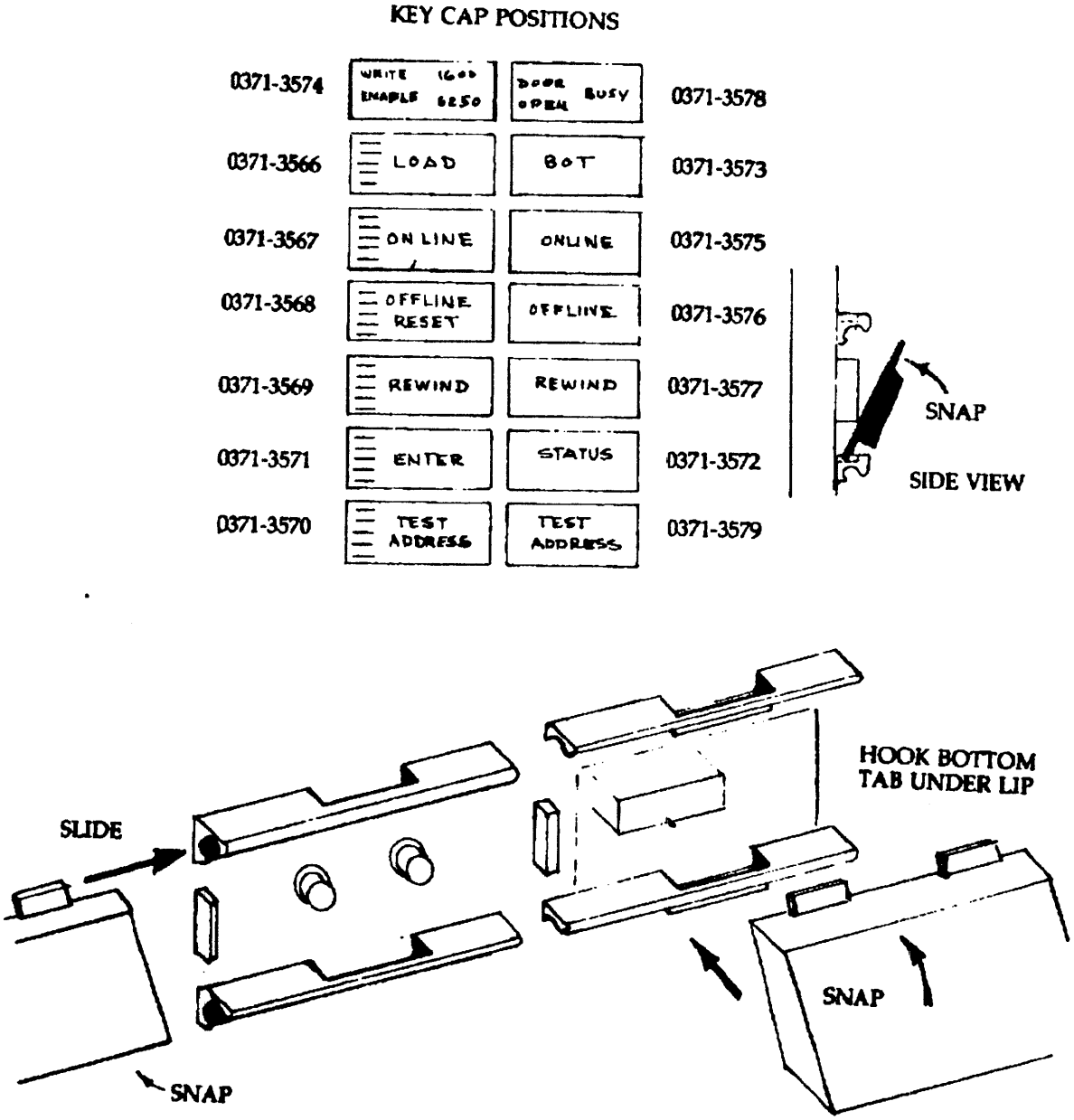


Figure (6) 1-29 Control Panel Key Caps

[2] CHASSIS

2.1 ACCESS

1. Grasp the lower decorative panel by the lower edge and pull. Panel is held on by insertion-fit connectors.

3. Use flat-blade screwdriver to rotate casting access screw counterclockwise 1/2 turn to release casting.

4. Swing casting out.

5. Use a flat-bladed screwdriver to loosen the two captive screws on the card restraint.

NOTE

Right-handed people will probably find it easiest to loosen the left fastener first.

To Access:

WRITE ASSEMBLY	(A7)
READ ASSEMBLY	(A8)
PHASE-LOCK LOOP ASSEMBLY	(A9)
FORMATTER ASSEMBLY	(A5)
MASTER CONTROLLER ASSEMBLY	(A4)
HP-IB ASSEMBLY	(A6)
POWER SUPPLY ASSEMBLY	(A10)

Disconnect:

- round cable between the Write Assembly (A7) and the Tape Head Assembly (A11).

- ribbon cable between the Read Assembly (A8) and the Preamplifier Assembly (A12).

2.2 HP-IB ASSEMBLY (A6)

REMOVAL

CAUTION

Use the extractor tabs to release the PC boards. When the tabs are spread, the board is released and partially extracted.

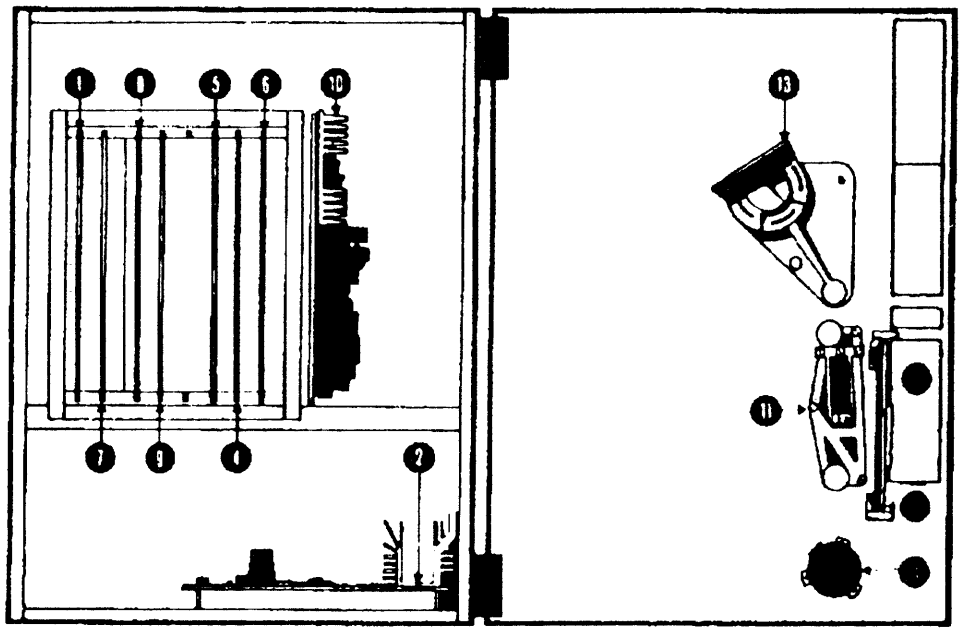
1. Remove PC board from card cage.

2. Use a #1 Posidriv to remove the three screws holding the PC board to the extender board.

REPLACEMENT

1. Align HP-IB PC board with metal extender board. As viewed from the top, the rear of the HP-IB PC board should be on the left side of the metal extender board and the two boards should form one plane. Insert screws and tighten with a #1 Posidriv.

2. Insert PC board/extender board into the card cage with the IC side of the HP-IB board to the right.



MAJOR COMPONENTS

1. SERVO CONTROLLER
2. MOTOR DRIVE
3. FRONT PANEL
4. MASTER CONTROLLER
5. FORMATTER
6. HP-IB ASSEMBLY
7. WRITE ASSEMBLY
8. READ ASSEMBLY
9. PHASE LOCK LOOP ASSEMBLY
10. POWER SUPPLY
11. TAPE HEAD ASSEMBLY
12. PREAMP ASSEMBLY
13. TAPE BUFFER ASSEMBLY
14. SPEED ENCODER

Figure (6) 2-1 Major Components

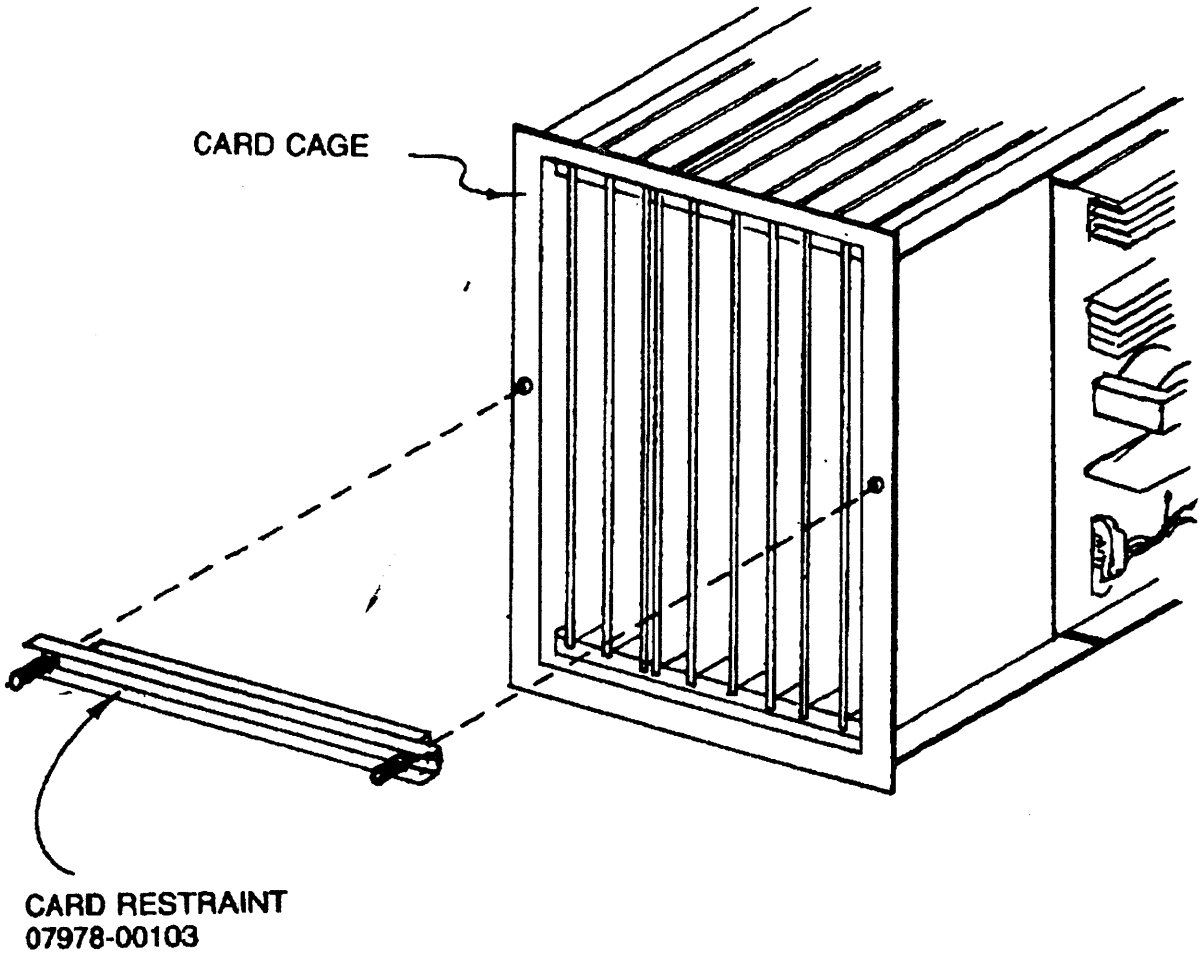


Figure (6) 2-2 Horizontal Card Restraint

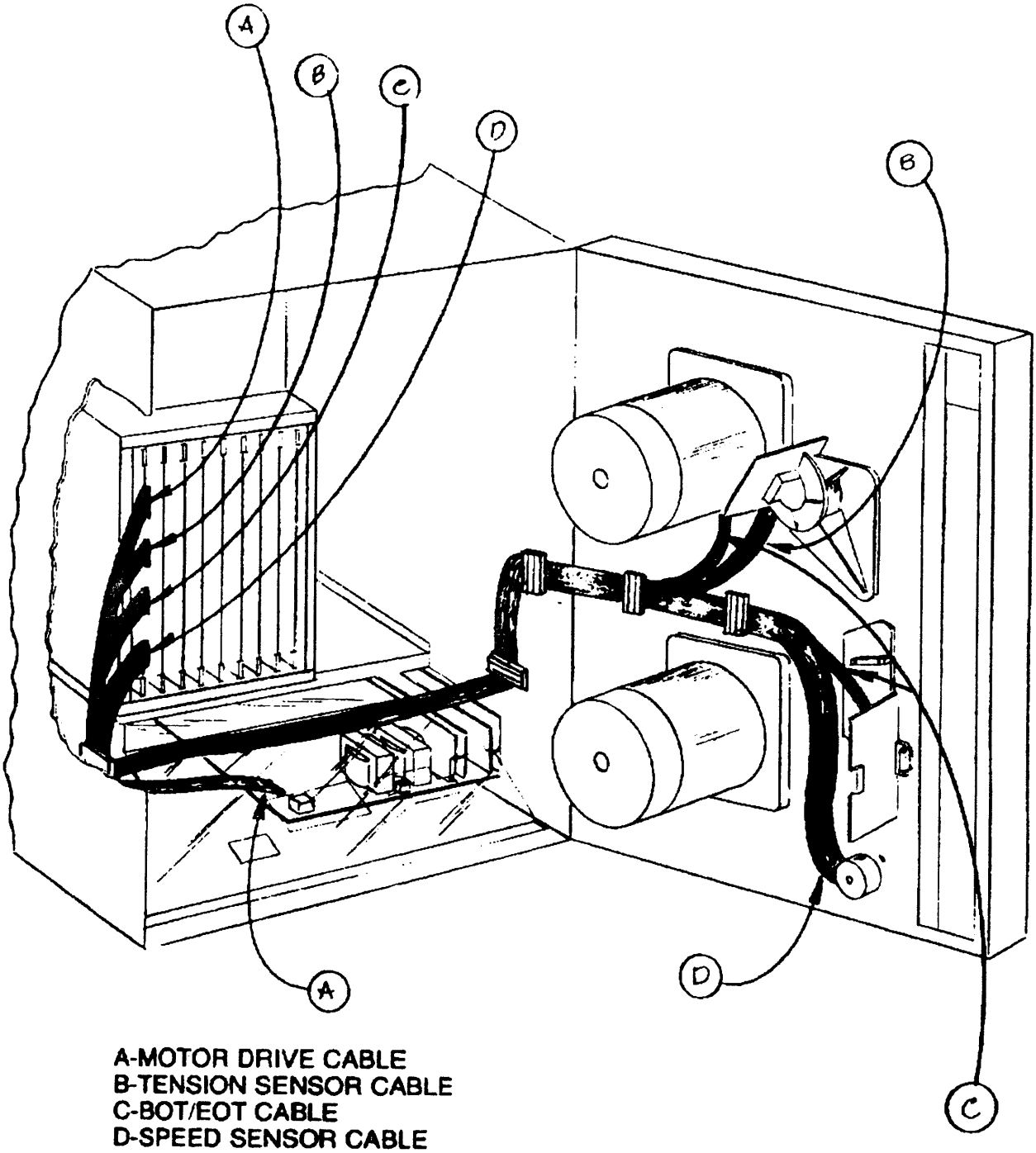


Figure (6) 2-3 Control Cables

2.3 SERVO CONTROLLER ASSEMBLY (A1)

REMOVAL

1. Remove four ribbon cable connectors from edge of PC board.

2. Remove PC board.

REPLACEMENT

1. Insert PC board into card cage with the IC side of the Servo Controller board to the right.

2. Connect four ribbon cables to edge connectors. Starting from the top of the edge connectors on the PC board, the progression is: the top has 20 connectors , the next 14, the next 16, and the bottom connector has 10.

After inserting any PC board within the card cage (except the Servo Controller Assembly) replace:

- round cable from the Tape Head Assembly (A11) to the Write Assembly (A7).

- braided ribbon cable from the Preamplifier Assembly (A12) to the Read Assembly (A10).

- Card Restrainer horizontally across card cage; use flat-bladed screwdriver.

2.4 MOTOR DRIVER ASSEMBLY (A2)

REMOVAL

1. Remove the power cable that goes to the supply reel motor (vertical connector on the right side of the Motor Drive Board). Squeeze tabs to unlock connector.

2. Remove the power cable that goes to the takeup reel motor (vertical connector on the left side of the Motor Drive Board). Squeeze tabs to unlock connector.

3. Remove the cable from the Preamplifier Assembly (A12) to the Read Assembly (A8).

4. Remove the cable that goes from the Tape Head Assembly (A11) to the Write Assembly (A7).

5. Use a flat-bladed screwdriver to loosen the two captive screws on the card restraint across the front of the card cage. Remove the card restraint to allow removal of all edge connectors.

NOTE

Right-handed people will probably find it easiest to loosen the left fastener first.

5. Remove the four cables to the Servo Controller Assembly (A1).

6. Open the cable clamps on the left and right front walls of the chassis.

7. Lay all cables out of the way to the right. The ribbon cable from the Servo Controller (A1) down to the Motor Drive Assembly (A2) will remain on the left until access is gained to the Motor Drive Assembly in the next step.

8. Remove the plastic safety shield over the Motor Drive Assembly by hooking fingers through holes in the face of the shield or around its edges and firmly, and slowly, pulling. The plastic push-in rivets should release with a moderate amount of upward and outward pressure on the shield.

9. Remove the motor driver board power supply connector from the center of the PC board, next to the relay. Squeeze tabs to unlock connector. Fold cables and connector out of the way to the left.

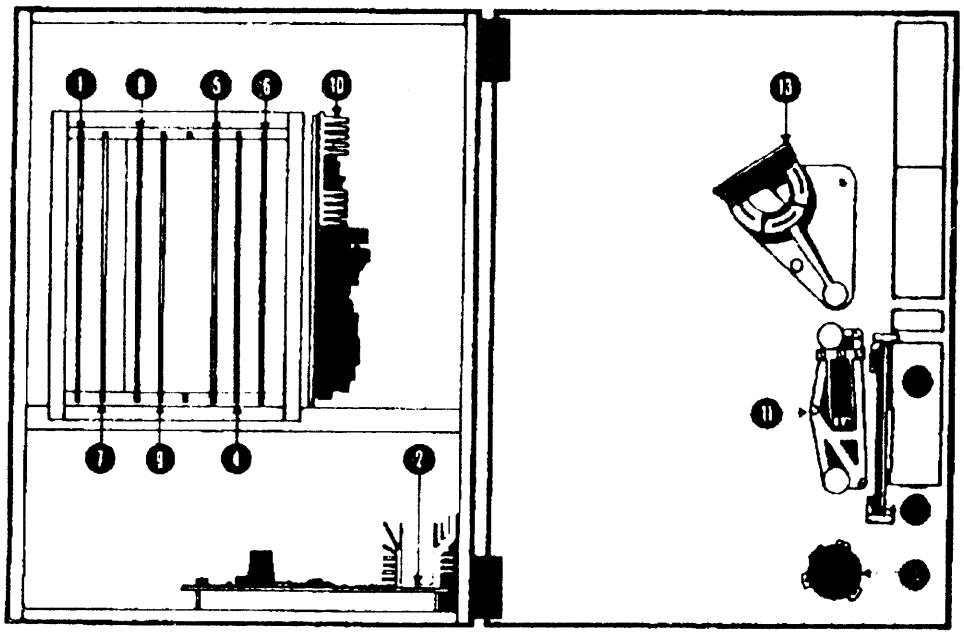
CAUTION

Keep track of all washers associated with the screws taken out of the Motor Drive Assembly PC board. Do not let the washers get lost on the board.

10. Remove 9 M3x10 screws holding the Motor Drive Assembly PC board to the bottom of the chassis.

11. Remove 4 M3 nuts holding the heat sink to the chassis wall.

12. Maneuver Motor Drive Assembly PC board up and out of the chassis.



MAJOR COMPONENTS

1. SERVO CONTROLLER
2. MOTOR DRIVE
3. FRONT PANEL
4. MASTER CONTROLLER
5. FORMATTER
6. HP-IB ASSEMBLY
7. WRITE ASSEMBLY
8. READ ASSEMBLY
9. PHASE LOCK LOOP ASSEMBLY
10. POWER SUPPLY
11. TAPE HEAD ASSEMBLY
12. PREAMP ASSEMBLY
13. TAPE BUFFER ASSEMBLY
14. SPEED ENCODER

Figure (6) 2-4 Major Components

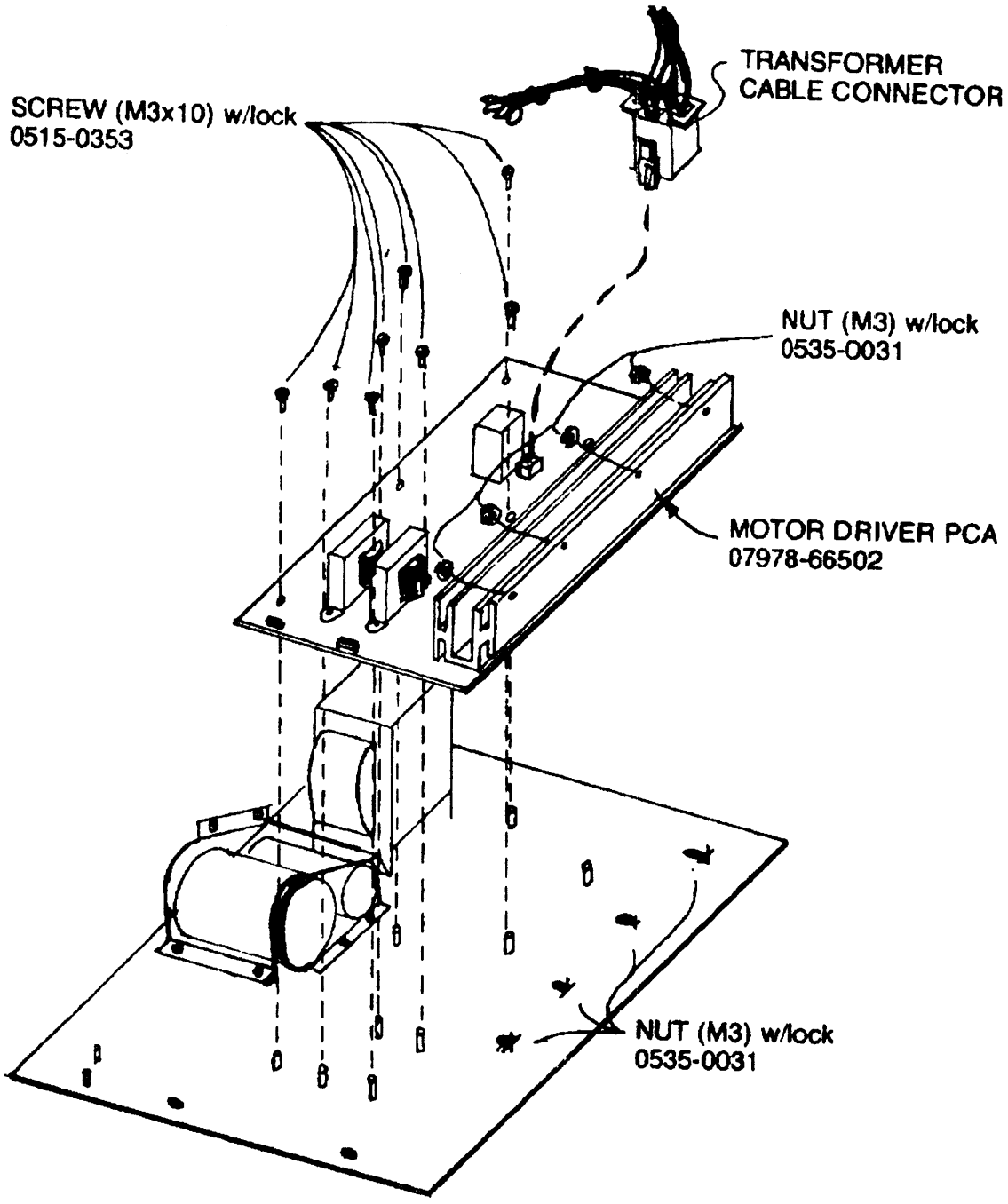


Figure (6) 2-5 Motor Driver Board

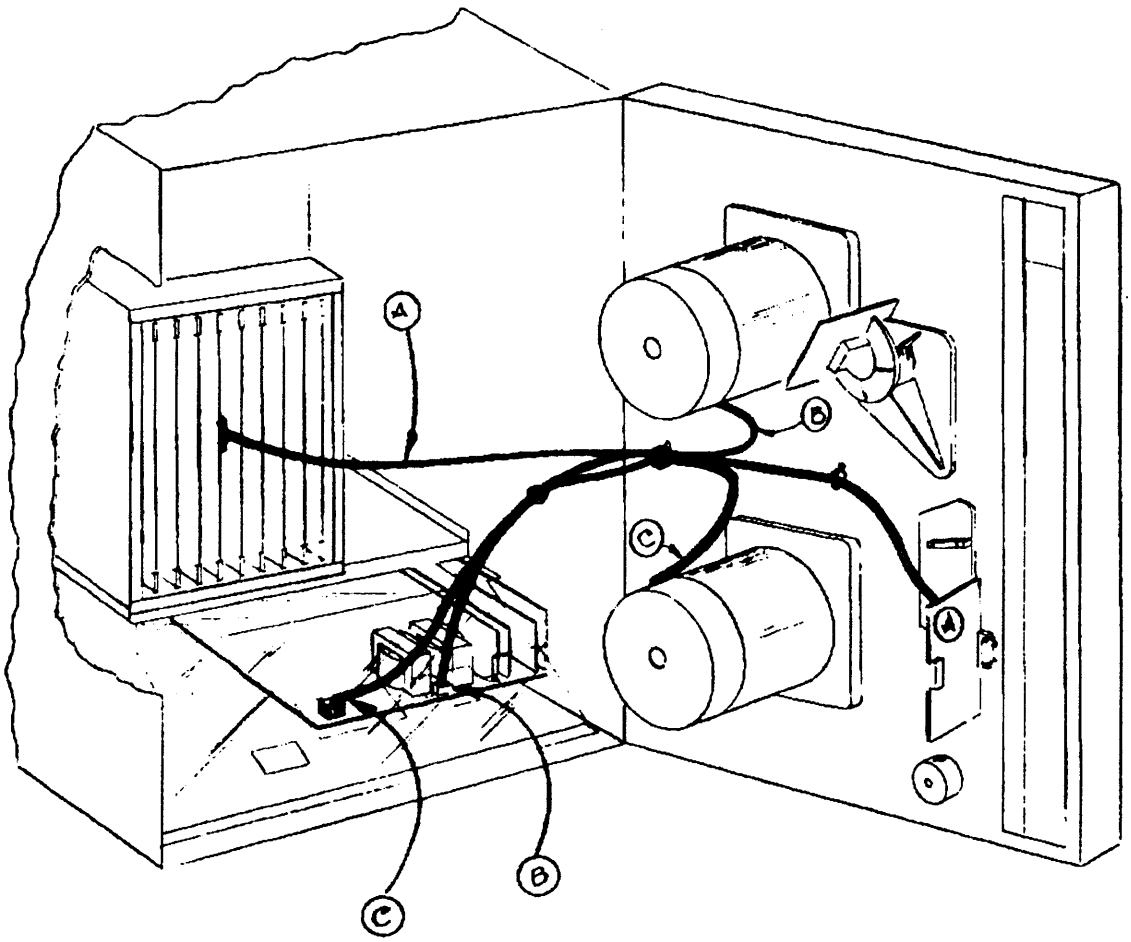


Figure (6) 2-6 Motor Cables

REPLACEMENT

1. Maneuver PC board into electronic chassis and positioned over the mounting pedestals. Heat sink goes on the right.

2. Align the heat sink holes with the four studs on the right side of the chassis. Attach the nuts, but do not tighten them yet.

3. Insert all nine screws that hold down the PC board. Do not tighten.

4. Tighten the four nuts through the heat sink.

5. Tighten the nine screws holding down the PC board.

6. Attach the connector from the motor driver power supply transformer and capacitors to the receptacle next to the relay on the PC board.

7. Route ribbon cable to cable clamp on the left front side of the chassis. Clamp cable.

8. Attach edge connector of the ribbon cable to the top connector on the Servo Controller Assembly (A1).

9. Attach the plastic guard panel over the Motor Driver Assembly (A2). Press in the top two plastic rivets, then the bottom two.

10. Retrieve the bundle of cables previously stored behind the casting. Route the three *flat* ribbon cables to the upper right cable clamp on the front of the chassis. Swing the casting to its full open position and lay the cables through the clamp. Clamp the cables. When the casting is full open, there should be no pulling force on the clamped cables.

11. Route the three cables to the lower clamp on the right front side of the chassis. Clamp the cables.

12. Route the cables across the plastic shield over the Motor Driver Assembly (A2) to the cable clamp on the lower left side of the chassis. Clamp the cables.

13. Connect the cables to the edge of the Servo Controller Assembly (A1) as follows: the 14-pin connector to receptacle which is second from the top on the PC board, the 16-pin connector to the receptacle which is third from the top, and the 10-pin conncector goes to the bottom receptacle.

14. Connect the braided ribbon cable from the Preamplifier Assembly (A12) to the Read Assembly (A8).

15. Connect the round cable from the Tape Head Assembly to the Write Assembly (A7).

16. Attach the supply reel power cable to the vertical connector on the right front of the Motor Driver PC board.

17. Attach the takeup reel power cable to the vertical connector on the left front.

2.5 MOTOR DRIVER PC BOARD POWER SUPPLY

ACCESSING THE AREA

1. Remove the power cable that goes to the supply reel motor (vertical connector on the right side of the Motor Drive Board, (A2)). Squeeze tabs to unlock connector.

2. Remove the power cable that goes to the takeup reel motor (vertical connector on the left side of the Motor Drive Board, (A2)). Squeeze tabs to unlock connector.

3. Remove the cable from the Preamplifier Assembly (A12) to the Read Assembly (A8).

4. Remove the cable that goes from the Tape Head Assembly (A11) to the Write Assembly (A7).

Capacitors

REMOVAL

WARNING

The capacitors in the Motor Driver PC board power supply are large and may retain a charge. Uncover them with care. Discharge them as soon as they are accessible.

1. Remove the power supply connector from the center of the Motor Driver PC board near the relay (if not already disconnected).

2. Remove the two M4 nuts and lockwasher from the upright screws holding the capacitor cover down.

NOTE

If the nuts are only loosened, and not removed, the capacitor cover can not be pulled away from the screw shafts far enough to raise it.

3. Insert screwdriver shaft under the front of the cover. Slide the screwdriver forward, leveraging the cover up and off the screw shafts.

4. See WARNING above. Pull capacitors forward and out from under the plastic cover.

5. Remove the cables connected to capacitors.

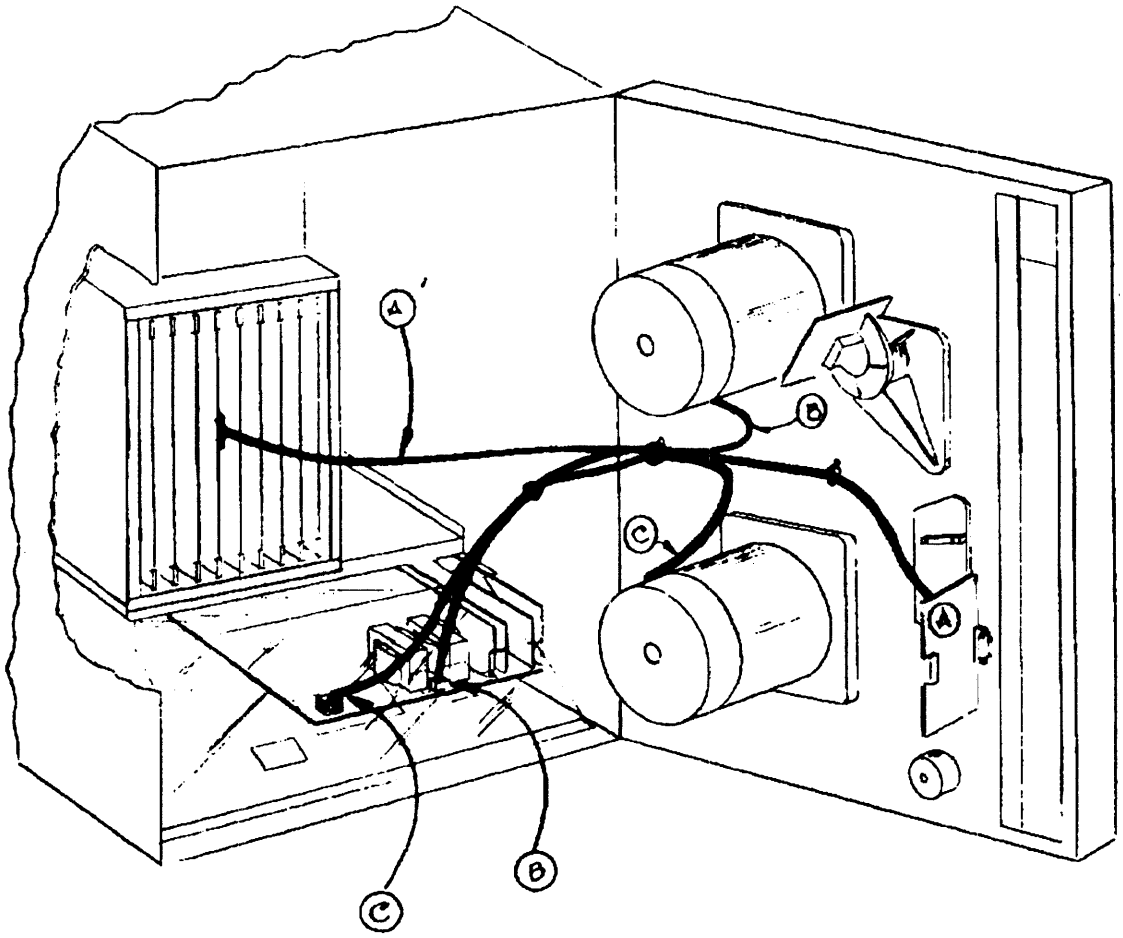


Figure (6) 2-7 Motor Cables

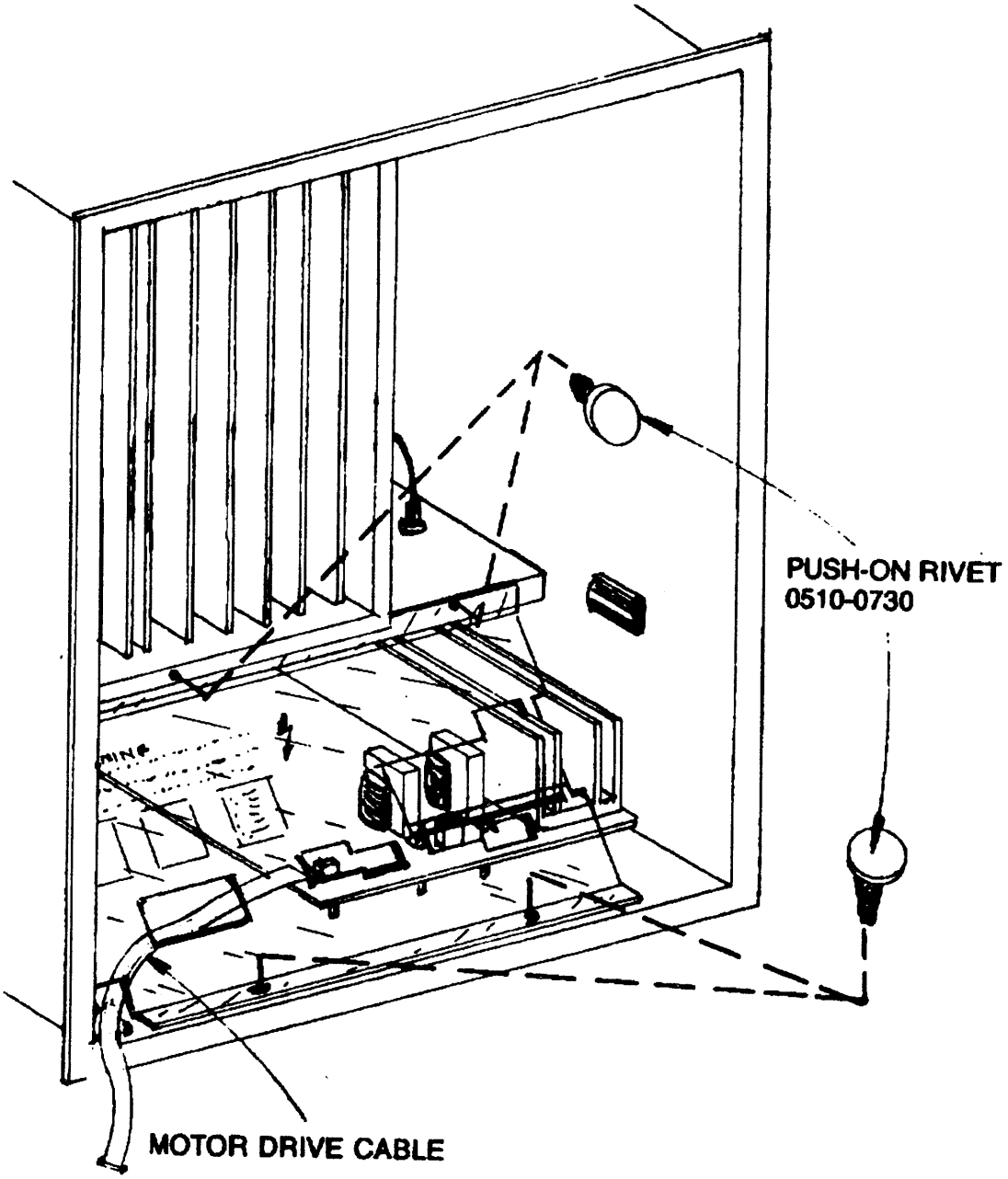


Figure (6) 2-8 Safety Shield Rivets

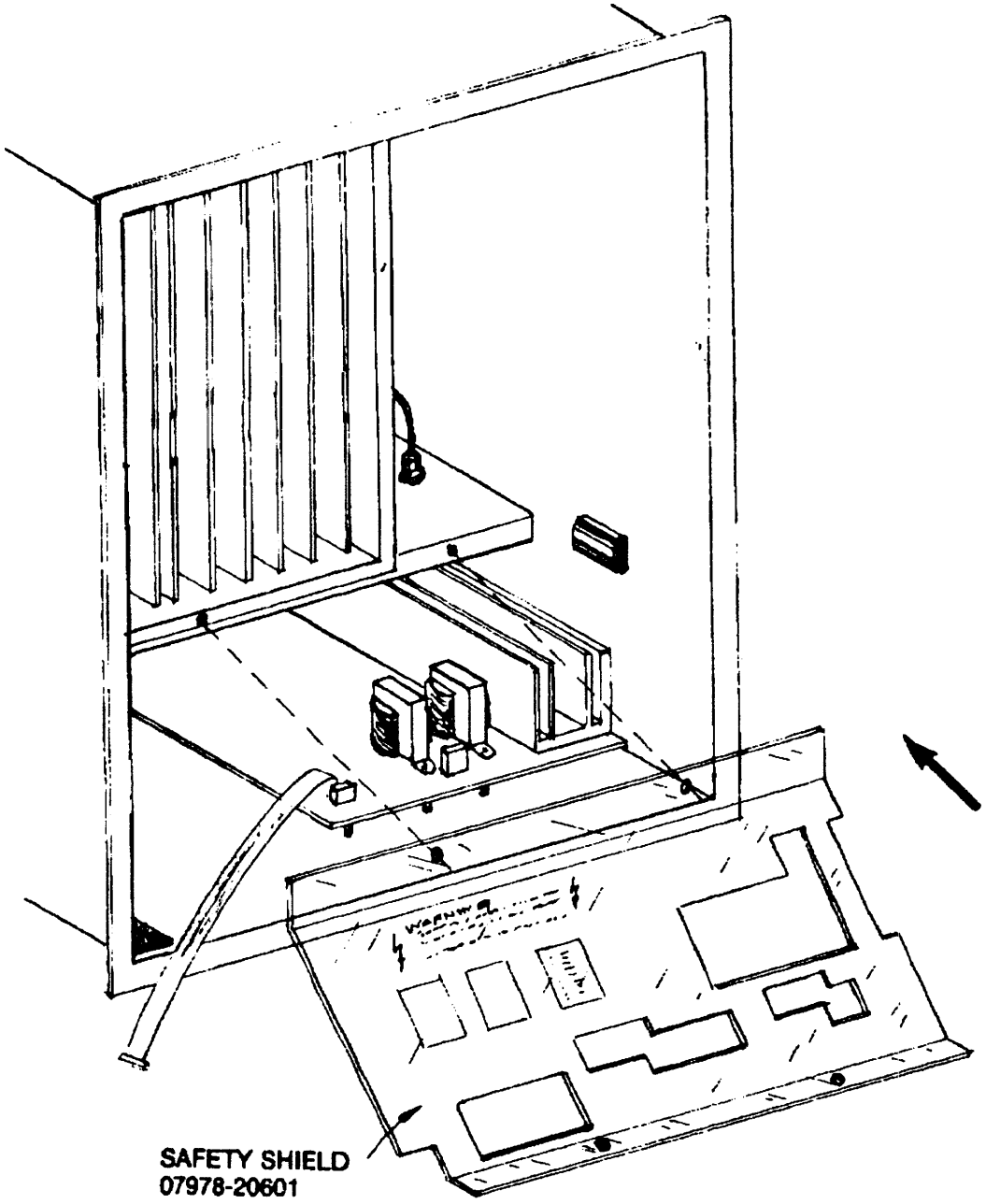


Figure (6) 2-9 Safety Shield

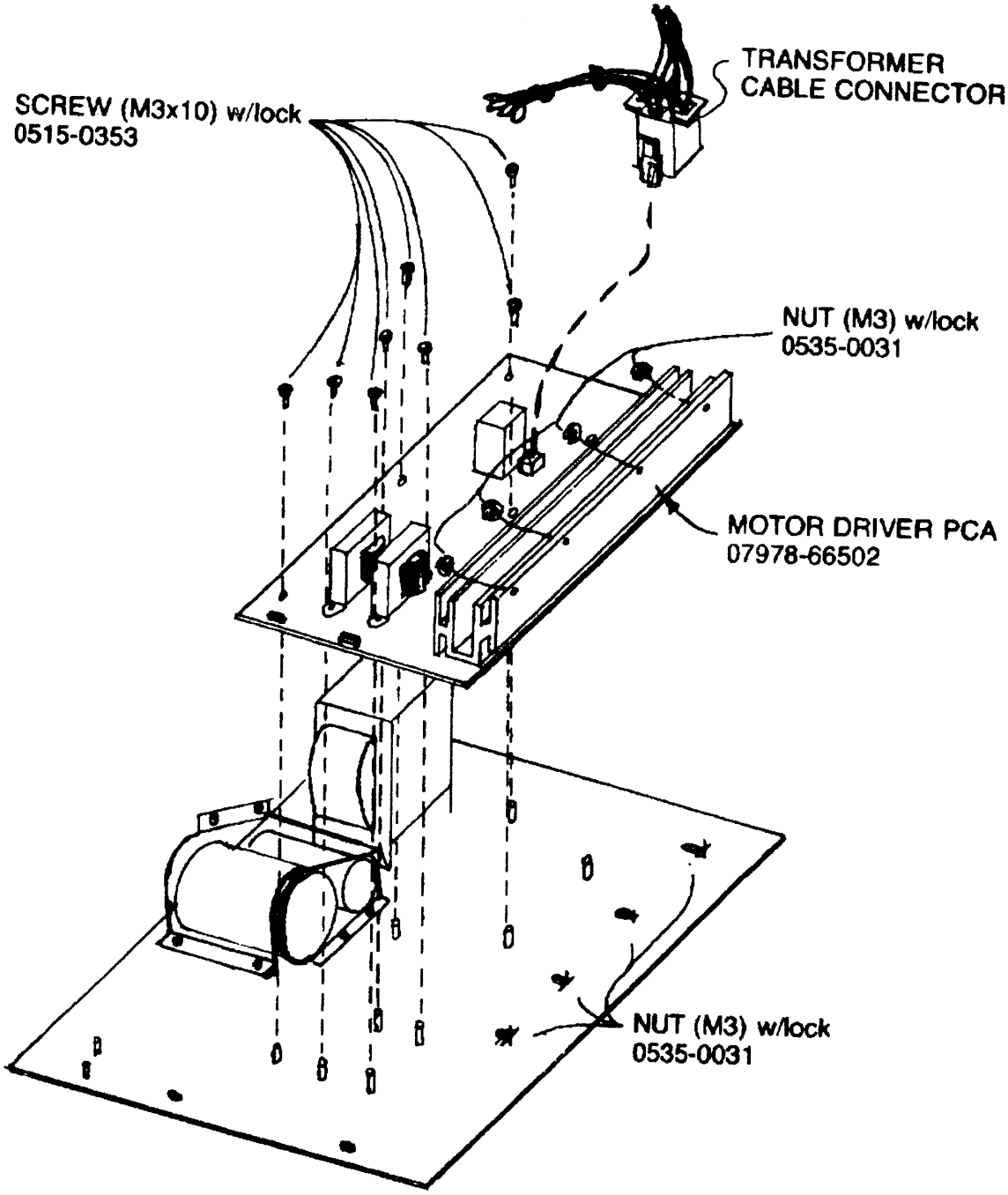


Figure (6) 2-10 Motor Driver Board

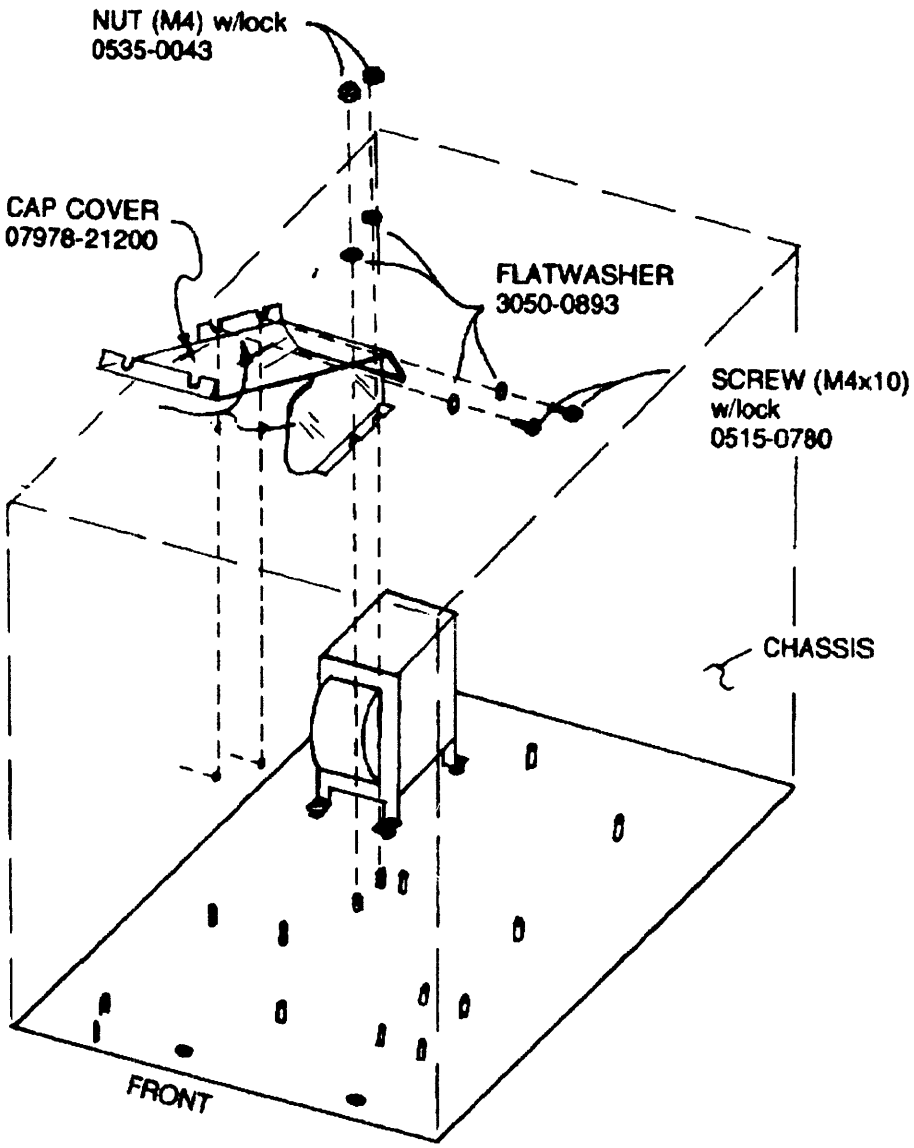


Figure (6) 2-11 Motor Driver Capacitors Cover

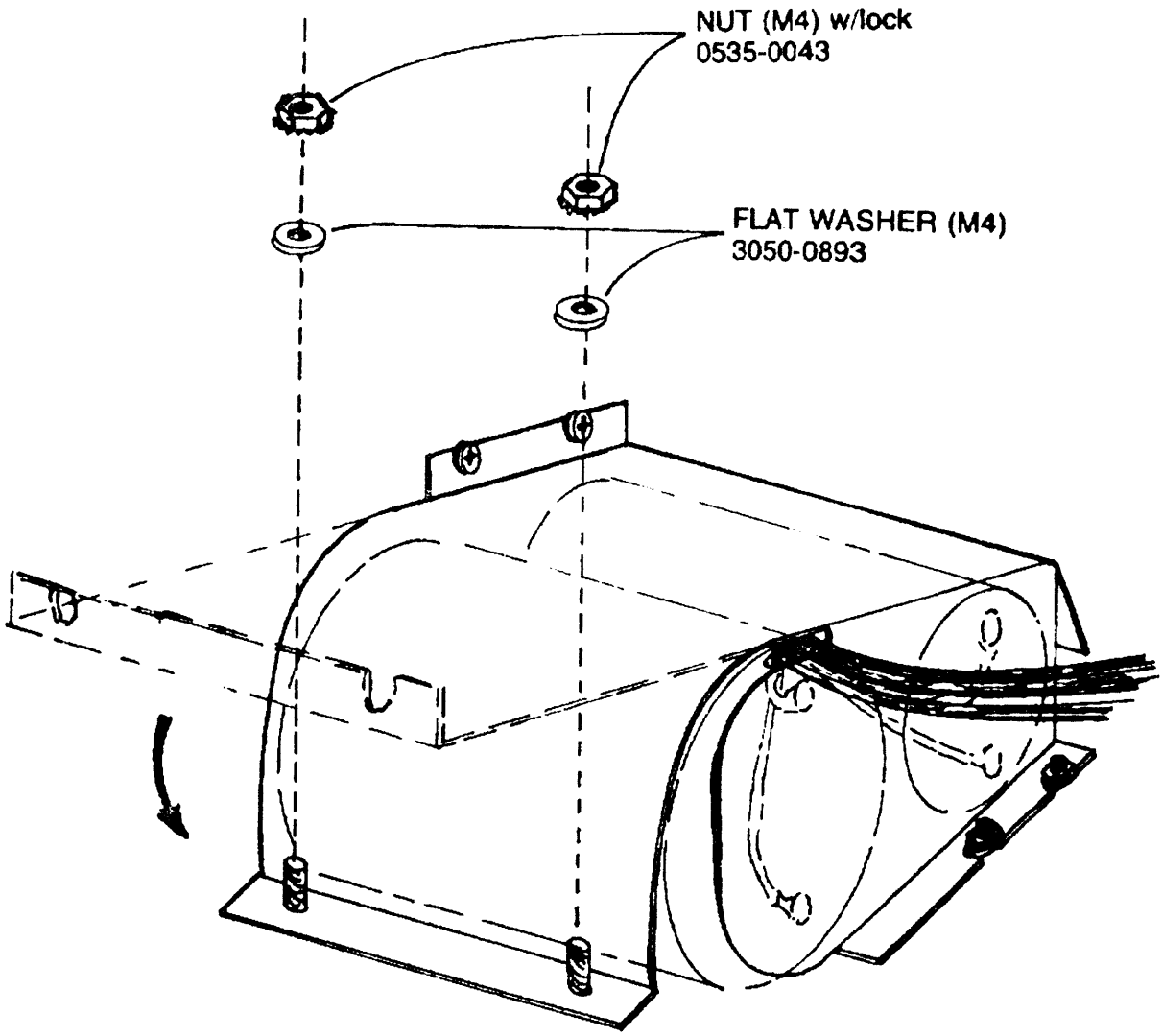


Figure (6) 2-12 Motor Driver Capacitors Placement

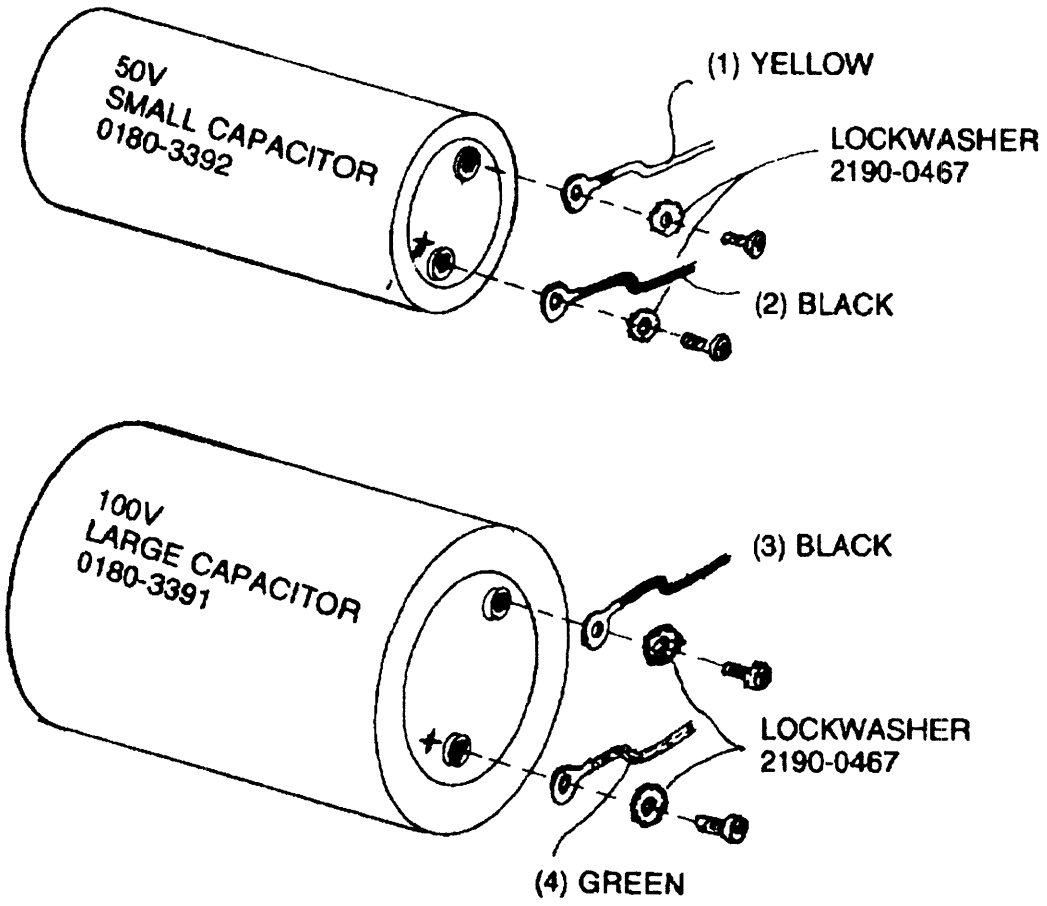


Figure (6) 2-13 Motor Driver Capacitors

REPLACEMENT

WARNING

Be sure capacitors are discharged before attempting to attach cables.

CAUTION

Be sure connections to the filter capacitors are tight to prevent arcing.

1. The black wires from the filter capacitors to the Motor Driver Assembly are interchangeable - they go to the same "electrical" point. Attach one black wire to the positive terminal of the small (50V) capacitor and the other black wire to the negative terminal of the large (100V) capacitor.

2. Attach the yellow wire to the minus terminal of the small (50V) capacitor.

3. Attach the green wire to the positive terminal of the large (100V) capacitor.

4. Put the small capacitor under the plastic enclosure first with its top facing to the right. Firmly push the capacitor to the rear of the enclosure. Route its cables over the top right wall of the capacitor enclosure.

5. Put the large capacitor in the enclosure, also with its top to the right. Firmly push on the large capacitor, using it to push the small capacitor fully to the rear of the enclosure. Route its cables over the top right wall of the capacitor enclosure.

6. Replace cover of enclosure by placing enclosure cover on top of screw shafts and pressing in and down. The cover slots should end up straddling the screw shafts at the floor of the chassis.

8. Attach M4 nuts and lockwashers to the cover screws.

9. Connect the motor driver PC board supply connector (contains the transformer and capacitor wires) to the receptacle in the center of the Motor Driver Assembly PC board next to the relay.

Transformer

REMOVAL

1. Begin by accessing the front of the capacitor/transformer area. Remove the power cable that goes to the supply reel motor (vertical connector on the right side of the board). Squeeze to unlock connector.

2. Remove the power cable that goes to the takeup reel motor (vertical connector on the left side of the board). Squeeze to unlock connector.

3. Remove the ribbon cable from the Preamplifier Assembly (A12) to the Read Assembly (A8).

4. Remove the round cable that goes from the Tape Head Assembly (A11) to the Write Assembly (A7).

5. Use a flat-bladed screwdriver to loosen the two captive screws on the card restraint across the front of the card cage. Remove the card restraint to allow removal of all edge connectors.

NOTE

Right-handed people will probably find it easiest to loosen the left fastener first.

6. Remove the four cables to the Servo Controller Assembly (A1).

7. Open the cable clamps on the left and right front walls of the chassis.

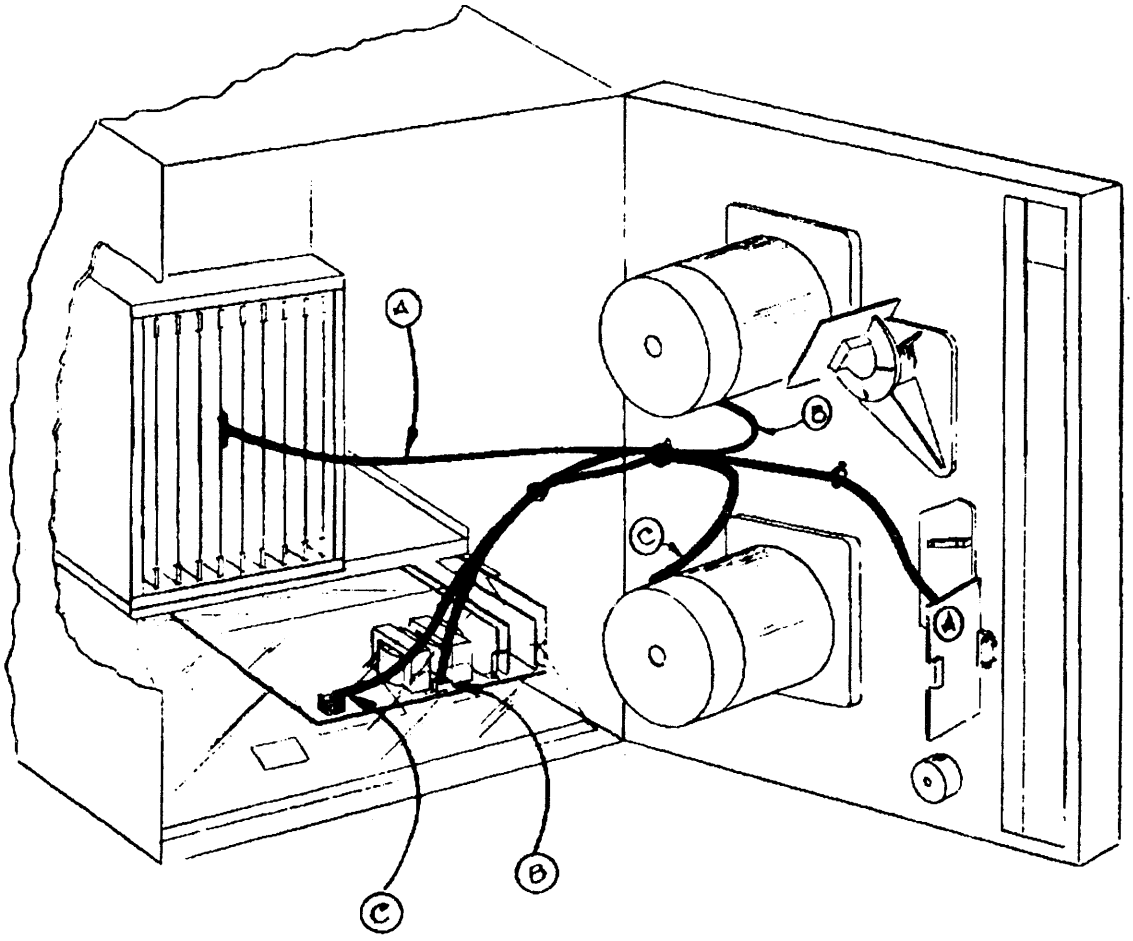
8. Lay all cables out of the way to the right. The ribbon cable from the Servo Controller (A1) down to the Motor Drive Assembly (A2) will remain on the left until access is gained to the Motor Drive Assembly in the next step.

9. Remove the plastic safety shield over the Motor Drive Assembly by hooking fingers through holes in the face of the shield or around its edges and firmly, and slowly, pulling. The plastic push-in rivets should release with a moderate amount of upward and outward pressure on the shield.

10. Remove the motor driver board power supply connector from the center of the PC board, next to the relay. Squeeze to unlock connector.

WARNING

The capacitors in the Motor Driver PC board power supply are large and may retain a charge. Uncover them with care. Discharge them as soon as they are accessible.



A – HEAD CABLE
B – UPPER MOTOR CABLE
C – LOWER MOTOR CABLE

Figure (6) 2-14 Motor Cables

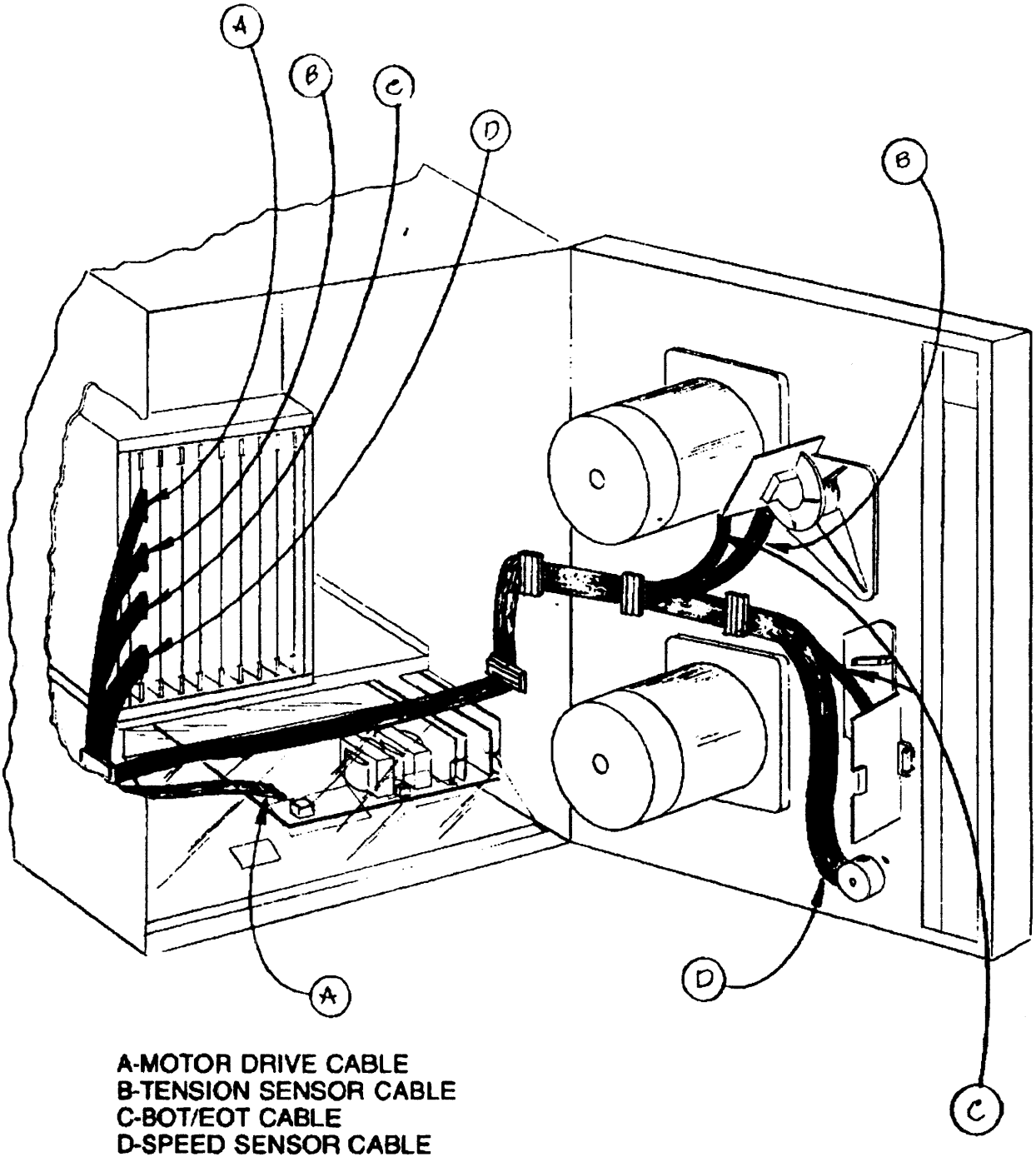


Figure (6) 2-15 Control Cables

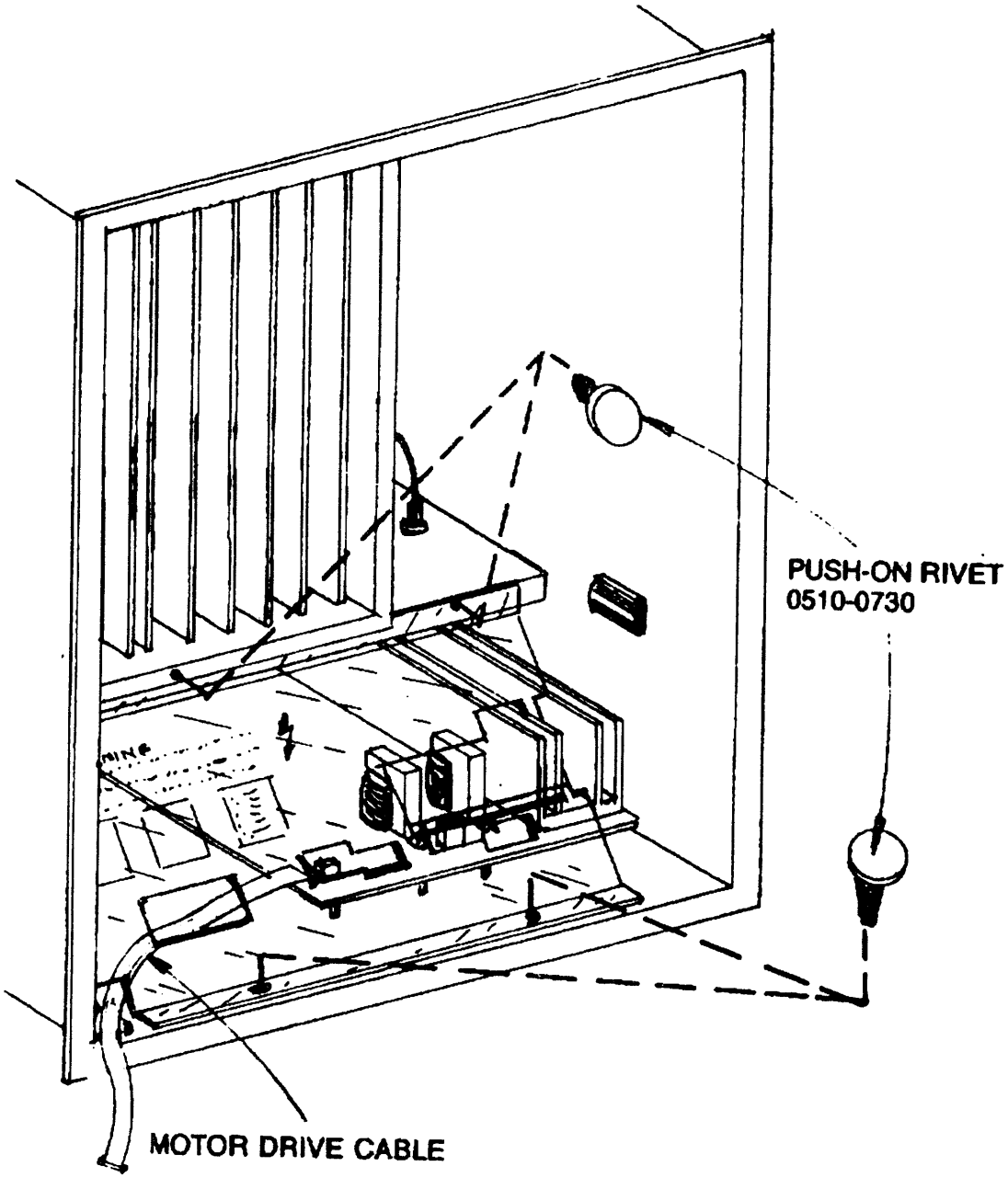


Figure (6) 2-16 Safety Shield Rivets

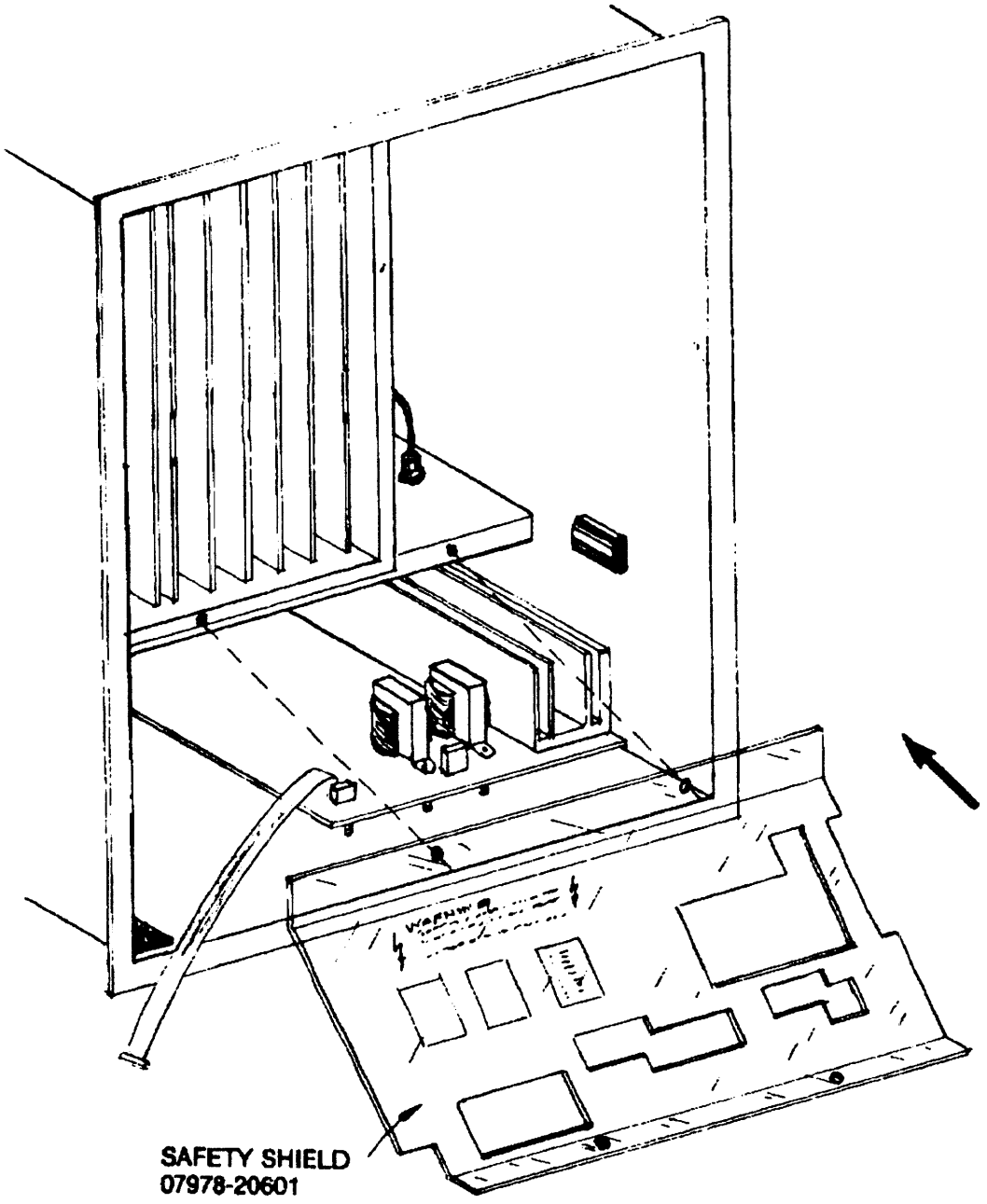


Figure (6) 2-17 Safety Shield

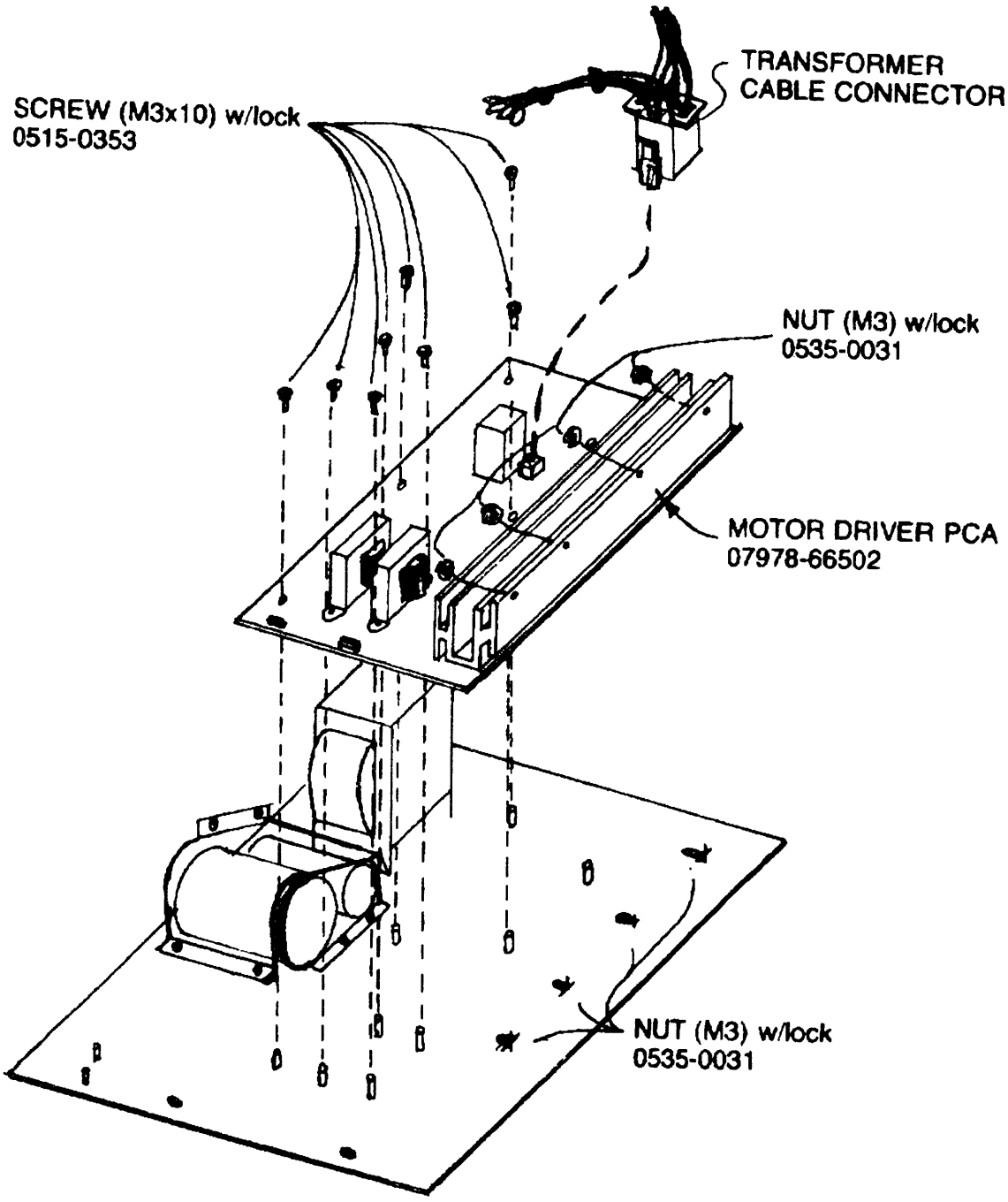


Figure (6) 2-18 Motor Drive Board

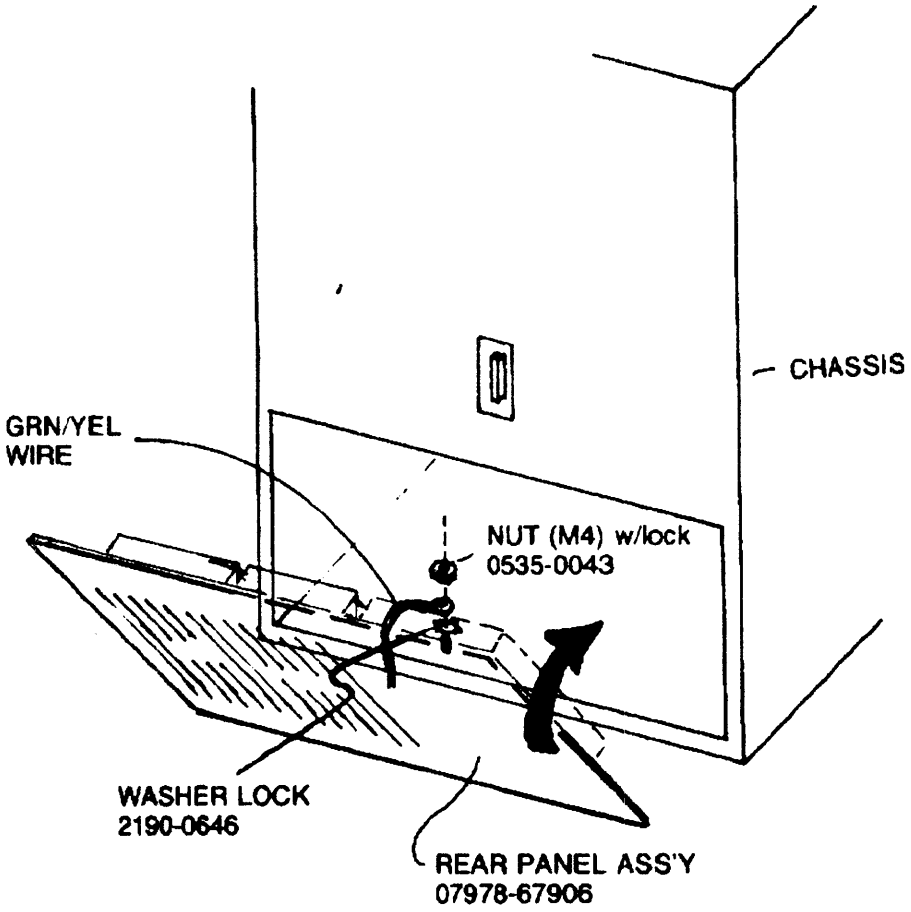


Figure (6) 2-19 Rear Access Panel

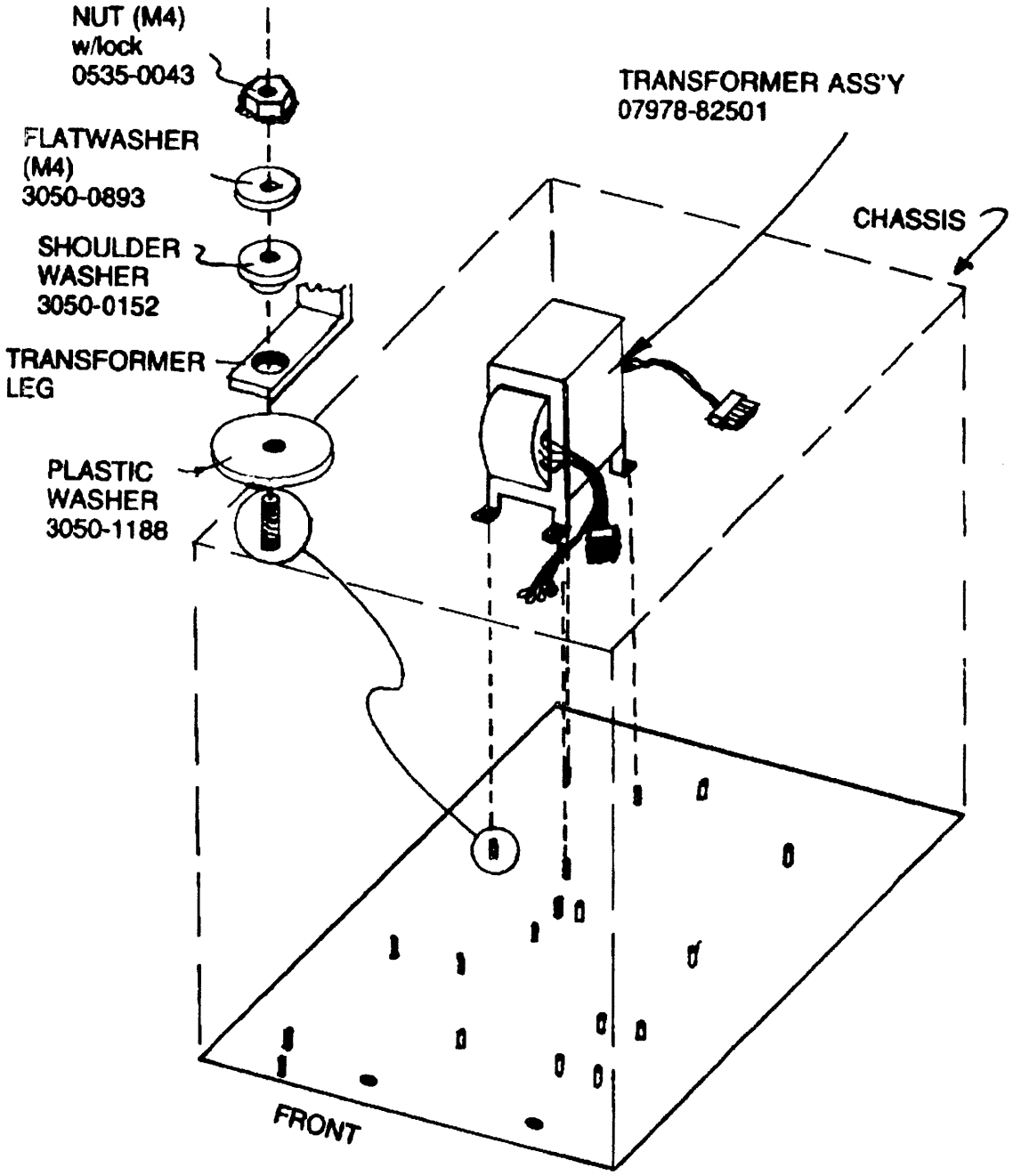


Figure (6) 2-20 Transformer Holdown Hardware

11. Remove the two M4 nuts and lockwasher from the upright screws holding the capacitor cover down.

NOTE

If the nuts are only loosened, and not removed, the capacitor cover can not be pulled away from the screw shafts far enough to raise it.

12. Insert screwdriver shaft under the front of the cover. Slide the screwdriver forward, leveraging the cover up and off the screw shafts.

13. See previous WARNING note. Pull capacitors forward and out from under the plastic cover.

14. Remove the capacitor enclosure. Two #2 Posidriv screws hold the enclosure to the left chassis wall, and two M4 nuts hold the bottom right side of the enclosure to the chassis floor.

15. Remove the M4 nut, flat washer, and shoulder washer that holds each front leg of the transformer to the chassis floor.

16. Unlatch rear door of the tape drive cabinet. Use a flat-bladed screwdriver (or coin) and rotate the locking screw counterclockwise 1/2 turn.

17. Use M4 nutdriver to remove 8 nuts on the perimeter of the Rear Panel Assembly.

NOTE

"Left" and "right" are as you look down into the chassis over the half-opened Rear Panel.

18. Rotate the panel out far enough to gain access to the inside of the chassis. Remove the M4 nut holding the ground wire that comes from the Rear Panel to the floor of the chassis (green/yellow wire).

19. Remove the two right-hand connectors on the back panel of the Power Module. Squeeze to unlock. These connectors go to the Motor Driver Assembly power supply transformer (left connector) and the Power Supply Assembly (A10).

20. Remove the M4 nut, flat washer, and shoulder washer that holds each rear leg of the transformer to the chassis floor.

21. Remove the transformer.

REPLACEMENT

1. Put transformer in the chassis by way of the Rear Panel opening. Position legs over the large, flat washers on the screw shafts (these should have been left in place when the previous transformer was removed). The cables should be to the left as you look in from the rear. Add shoulder washer, flat washer, and M4 nut to both rear leg bolts. Hand tighten.

2. Put shoulder washer, flat washer, and M4 nut on each front leg bolt. Tighten front leg nuts.

3. Tighten rear leg nuts.

4. Install capacitor enclosure. Two M4 screws are used on the chassis wall, and two M4 nuts hold the right side of the enclosure to the chassis floor.

5. Insert small capacitor into the enclosure first with its top facing to the right. Firmly push the capacitor to the rear of the enclosure. Route its cables over the top right wall of the capacitor enclosure.

6. Put the large capacitor in the enclosure, also with its top to the right. Firmly push on the large capacitor, using it to push the small capacitor fully to the rear of the enclosure. Route its cables over the top right wall of the capacitor enclosure.

7. Replace cover of enclosure by placing enclosure cover on top of screw shafts and pressing in and down. The cover slots should end up straddling the screw shafts at the floor of the chassis.

8. Attach M4 nuts and lockwashers to the cover screws.

9. Connect the motor driver PC board supply connector (contains the transformer and capacitor wires) to the receptacle in the center of the Motor Driver Assembly PC board next to the relay.

10. Install rear panel. Position Rear Panel with Power Module near the top and to the right (as you look down at the rear of the chassis.

11. Resting the bottom edge of the Rear Panel on the chassis rear edge, attach the green/yellow grounding wire to the chassis floor using an M4 nut.

12. Connect the cables to the rear of the Power Module. The left hand connector (as you look down) is to the fans, the middle connector is to the Motor Driver PC board power supply transformer, and the right connector is to the Power Supply Assembly (A10).

13. Rotate the Rear Panel up and over the mounting screw posts.

14. Use a M4 nut driver to attach the eight nuts to the screws around the perimeter of the Rear Panel.

15. Thread the tape drive power cord through the lower hole in the rear door of the cabinet.

16. Attach HP-IB cable (if this has been disconnected). Pass the cable out the hole halfway up the rear door of the cabinet.

2.6 POWER SUPPLY ASSEMBLY (A10)

REMOVAL

1. Use a flat-bladed screwdriver to loosen the two captive screws on the vertical card restraint.

2. Unplug the power cord from its receptacle on the front edge of the Power Supply PC board. The power cord is tie-wrapped to the card restraint, so both are removed together. Move these pieces out of the way to the right.

NOTE

Some early units have a longer jumper cable than the one discussed in the following step. Watch the action of the cables as you pull the PC board forward to determine if you have a short jumper cable or a long one. If you find you have a long jumper cable, you will be able to pull the PC board forward about one foot and will be able to easily see the connection to the 110V pin.

3. Slide the PC board forward about 3-4 inches (early units). Reach around to the rear of the board and disconnect the single jumper wire that branches off the main power cable. The main power cable comes from the rear panel up though the metal cover over the Motor Driver Assembly (A2).

4. Disconnect the jumper wire that is attached to the 110V pin near the capacitors near the lower rear of the PC board. The 110V pin is the uppermost pin when the PC board is mounted on the chassis.

5. Slide Power Supply Assembly all the way out.

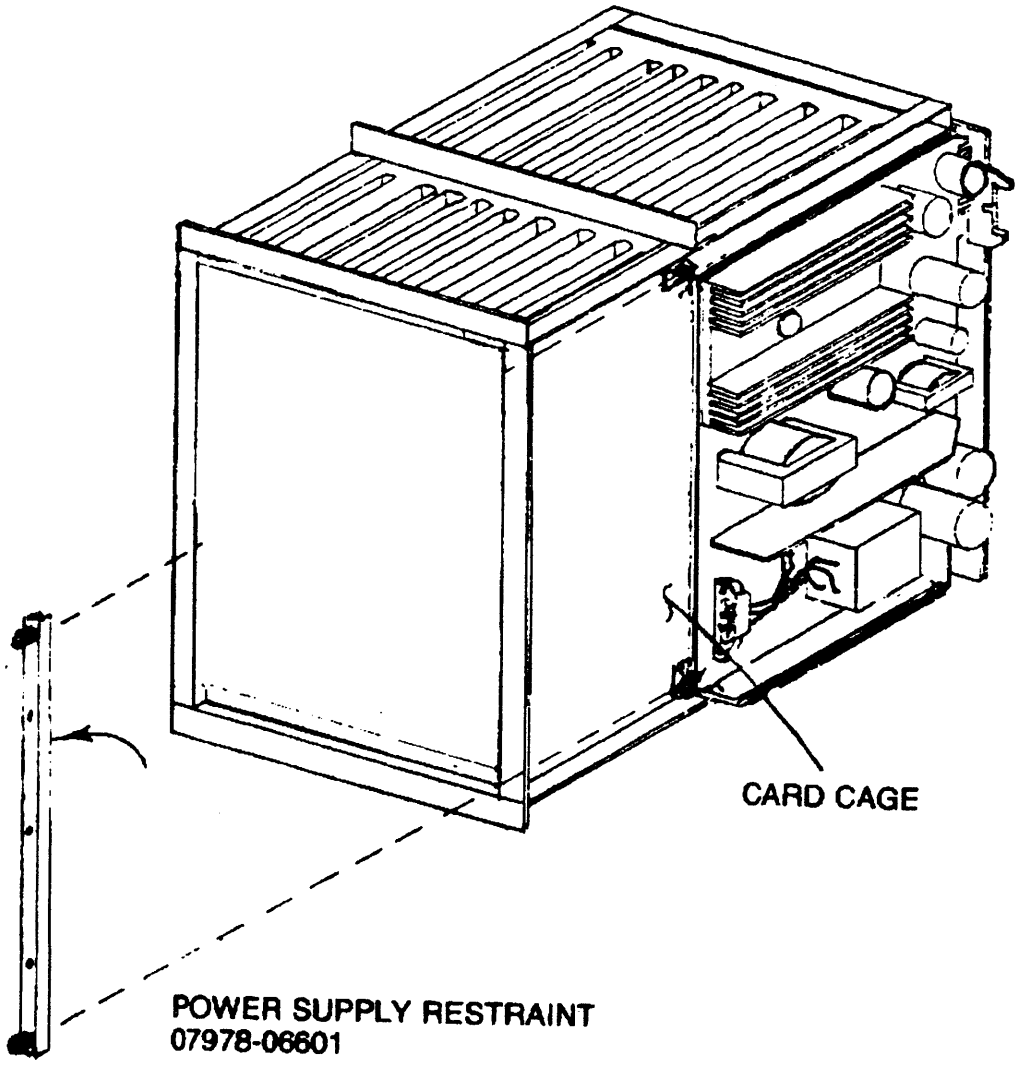


Figure (6) 2-21 Logic Power Supply Board Restraint

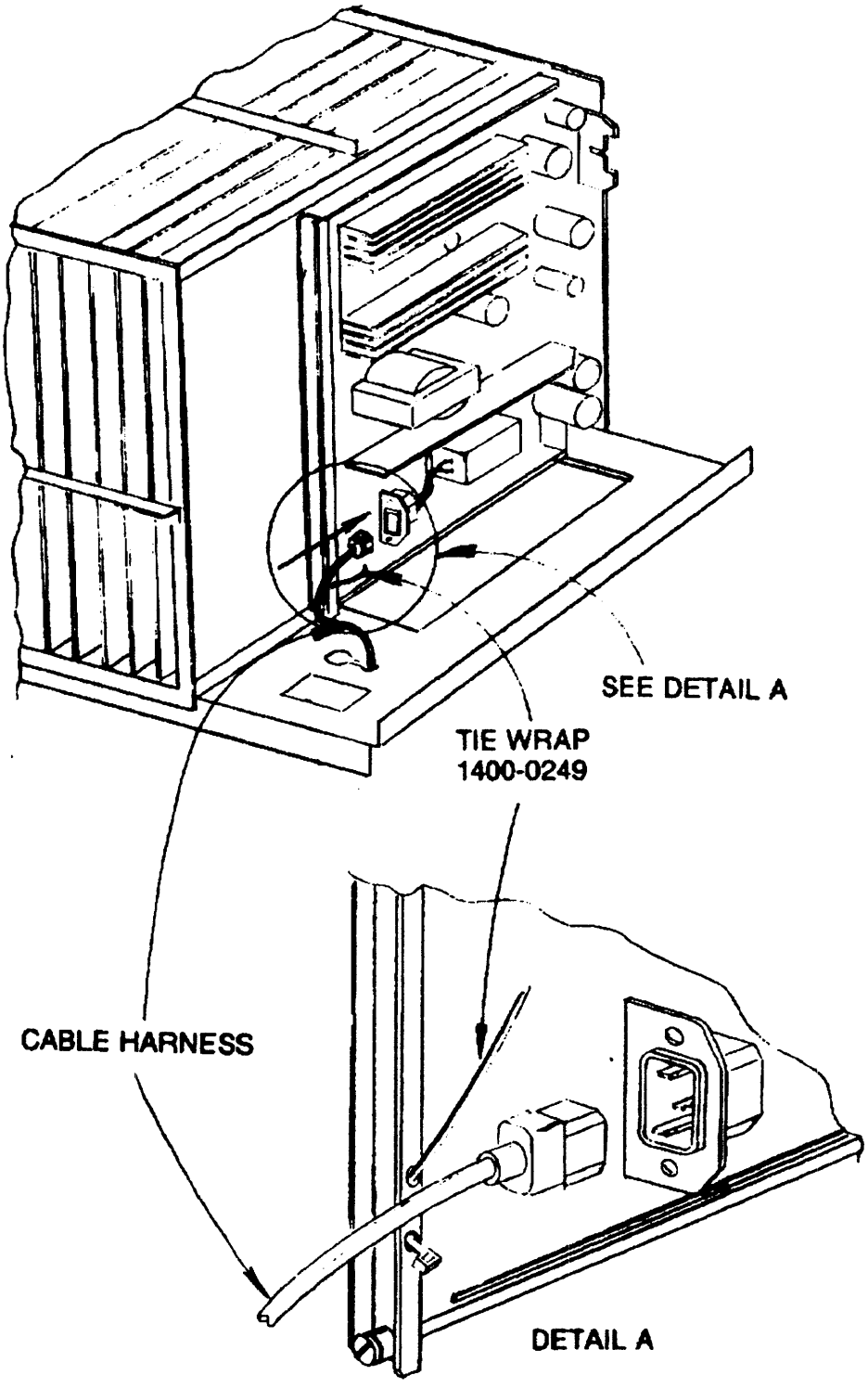


Figure (6) 2-22 Logic Power Supply

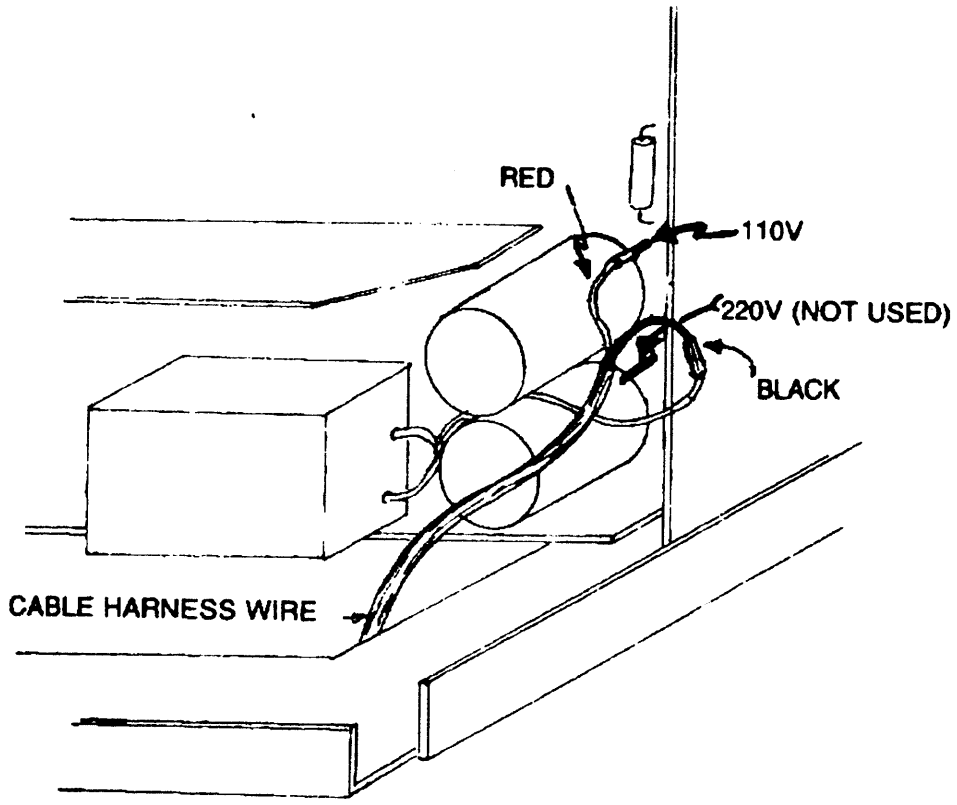


Figure (6) 2-23 Logic Power Supply Jumpers

REPLACEMENT

1. Slide Power Supply PC most of the way back into the chassis. Stop about 3-4 inches short of putting the board all the way in.

2. Connect the single, *female* slip connector onto the 110V pin on the lower rear edge of the PC board above the capacitors.

3. Connect the single, *male* slip connector to the connector on the single, yellow wire branching off the main power cable.

4. Slide the PC all the way into the motherboard.

5. Move the card restraint (tie-wrapped to the power cord) into position. Insert the power cord into the receptacle near the front edge of the PC board. Use flat-bladed screwdriver to fasten card restraint.

2.7 REAR PANEL

ACCESSING THE AREA

1. Use a flat-bladed screwdriver (or coin) to unlatch rear cabinet door. Rotate counterclockwise 1/2 turn.

2. Use an M4 nutdriver to remove 8 nuts on the perimeter of the Rear Panel Assembly.

NOTE

"Left" and "right" are as you look down into the chassis over the half-opened Rear Panel.

3. Rotate the panel out far enough to gain access to the inside of the chassis. Remove the M4 nut holding the ground wire that comes from the Rear Panel to the floor of the chassis (green/yellow wire).

4. Remove the two right-hand connectors on the back panel of the Power Module. Squeeze tabs to unlock. These connectors go to the Motor Driver Assembly power supply transformer (left connector) and the Power Supply Assembly (A10).

5. Proceed to instructions for specific area.

Fans

REMOVAL (Described for one fan)

1. Remove the fan power cord.

2. Remove the four M3x45 screws and washers that hold the fan assembly to the Rear Panel. These screws also hold the fan guards to the fan enclosure.

3. Remove the M4 screw holding the ground wire to the fan.

REPLACEMENT

1. Install fan ground wire with a M4 screw.

2. Position fan assembly so that the arrow on the decal is on top and points away from the Rear Panel (towards what will be the inside of the chassis).

3. Install M3x45 screws through the four extended loops in the fan grill. These screws pass through the corners of the fan assembly into the Rear Panel. It is possible to mount the guard with either side near the fan blades. Choose the side that keeps the guard away from the blades when the screws are tightened.

4. Connect the fan power cord.

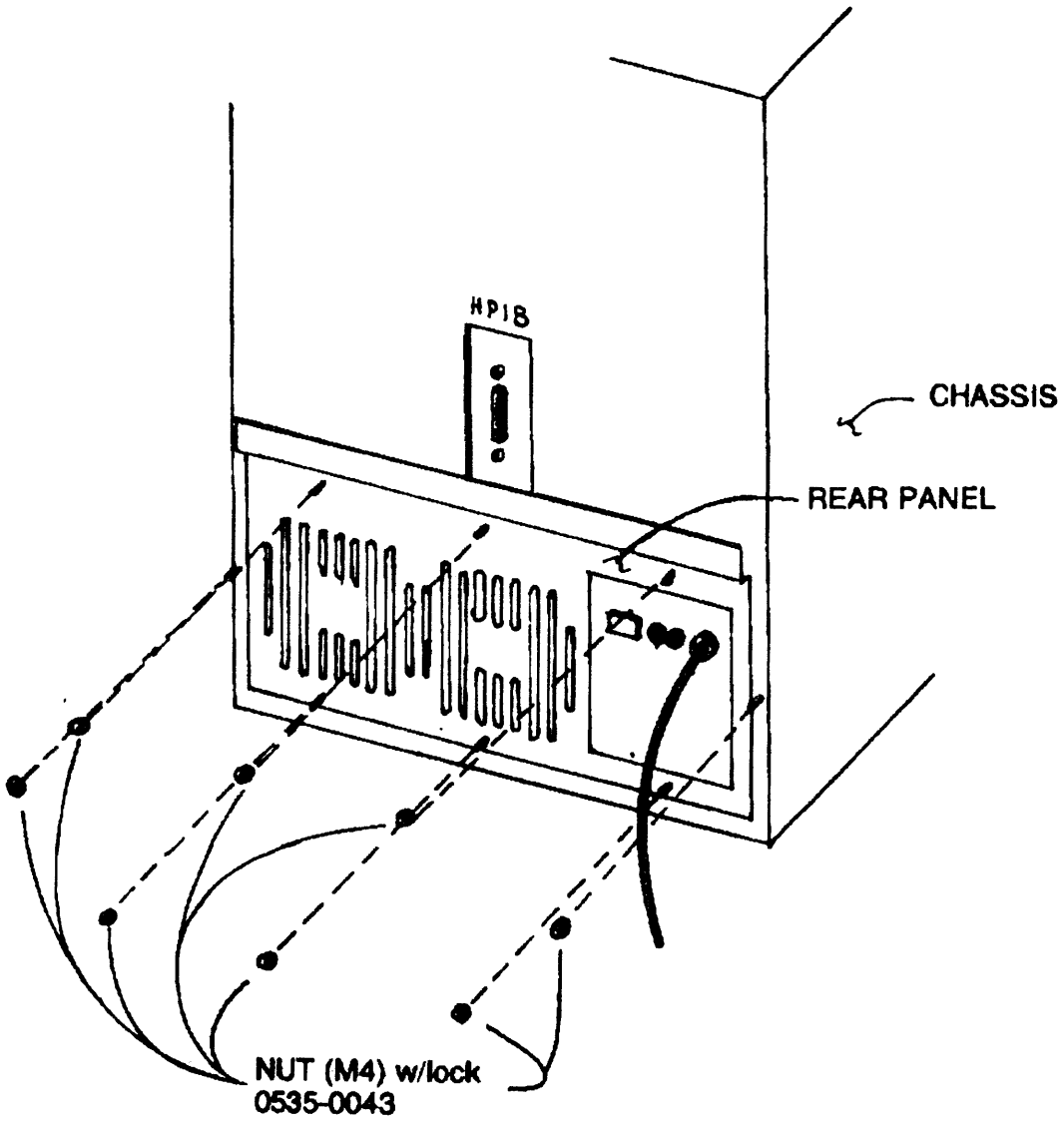


Figure (6) 2-24 Rear Access Nuts

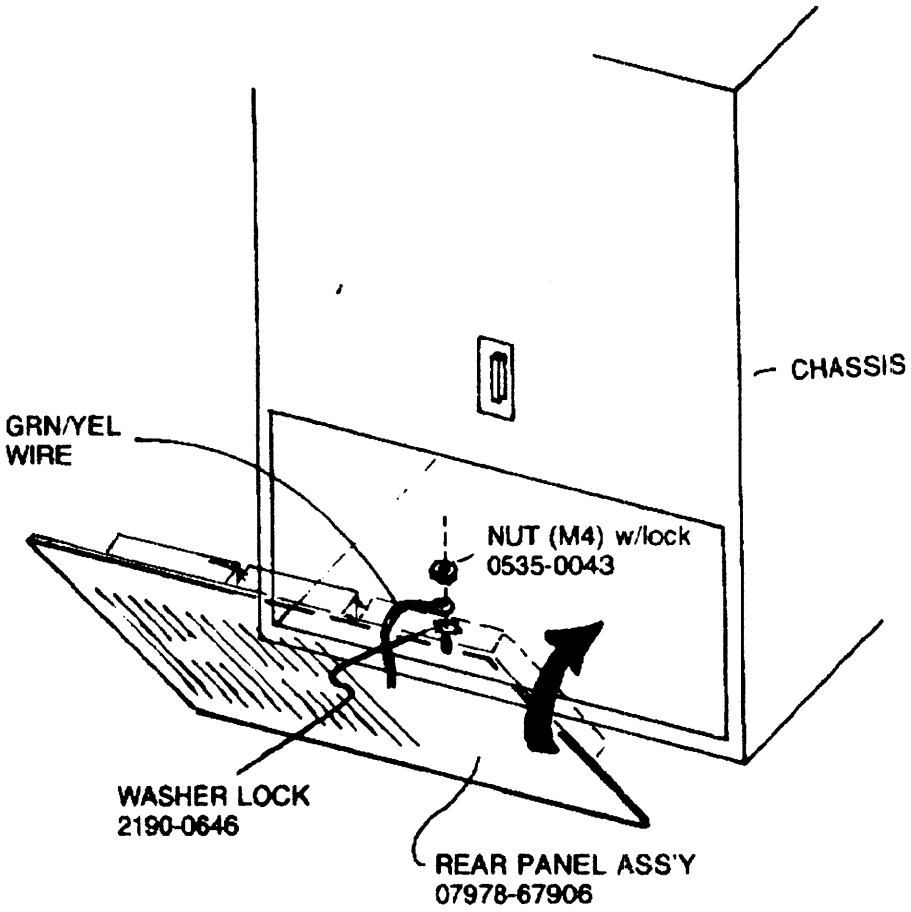


Figure (6) 2-25 Rear Access Panel

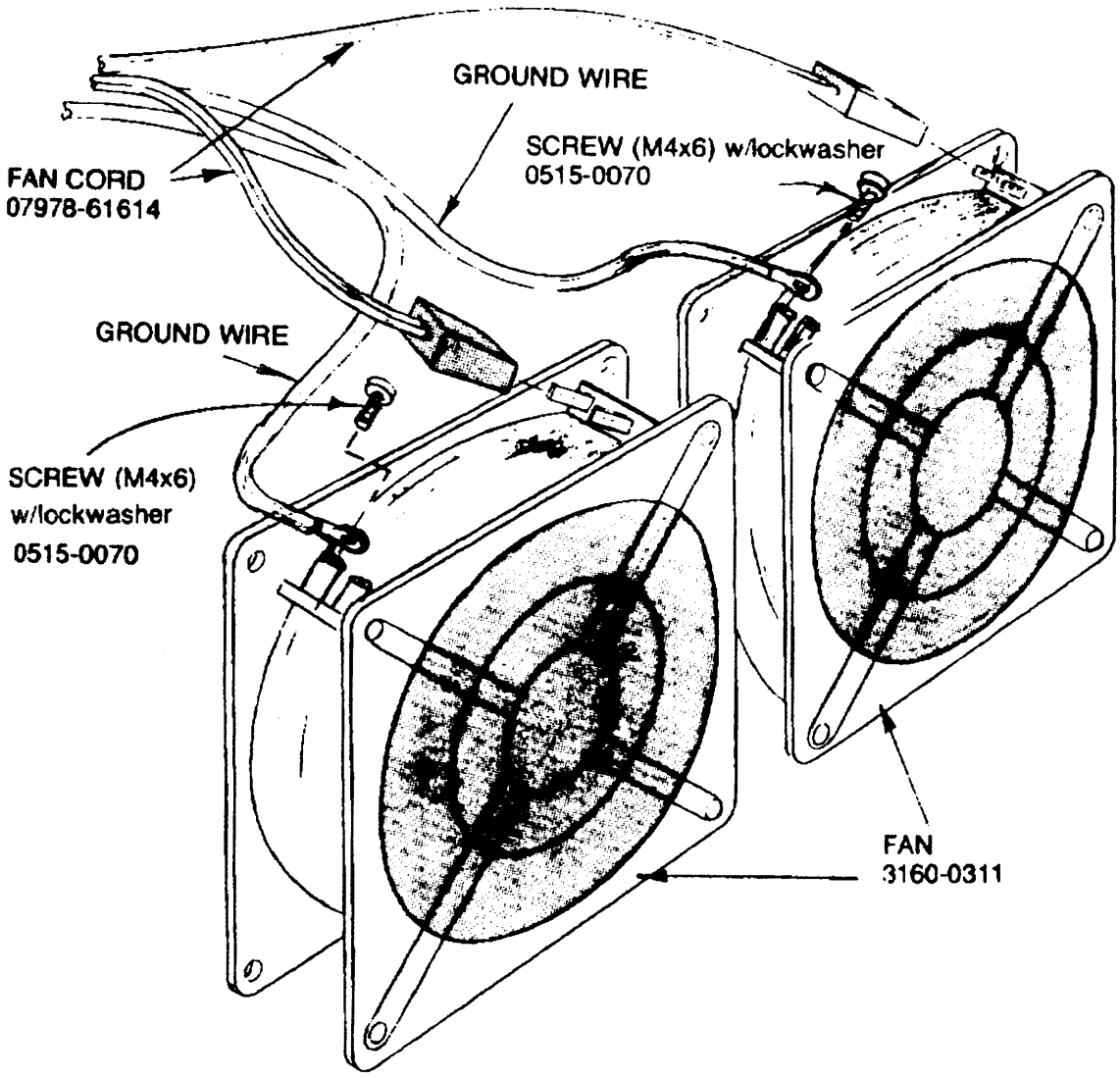


Figure (6) 2-26 Fan Power Cords

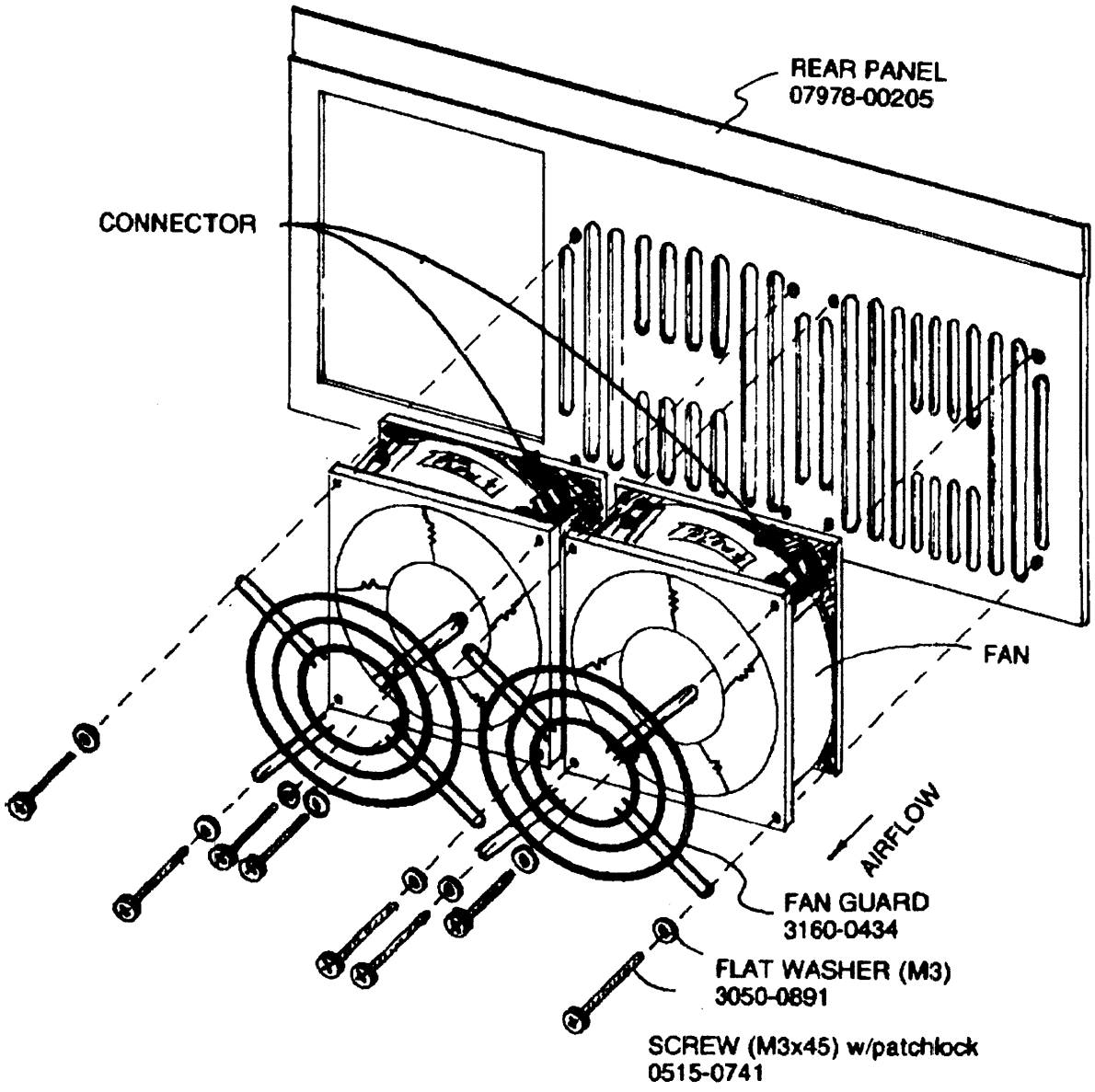


Figure (6) 2-27 Fan Mounting

Power Module Assembly

REMOVAL

1. Remove the connector to the fans. The connector tabs must be squeezed to unlock it. The connectors to the Motor Driver PC board, power supply transformer, and Power Supply Assembly (A10) should already have been removed during "ACCESSING THE AREA".

2. Use M3 nut driver to remove four nuts holding down the Power Module cover; one on each corner of the module.

3. Remove the M4 nut holding the green/yellow ground wire that goes from the Power Module to the Rear Panel. This nut also holds the green/yellow Rear-Panel-to-chassis ground wire and a starwasher.

4. Remove the Power Module.

REPLACEMENT

1. Thread the Power Module power cord through the large opening in the Rear Panel - from inside (chassis side) to outside.

2. Place Power Module on the inside of the Rear Panel so that the green/yellow ground wire and the PC board are at the inside top of the Rear Panel.

3. Stack the Power Module ground wire, starwasher, and Rear-Panel-to-chassis ground wire on the ground wire screw. The screw is located near the top of the Rear Panel between the Power Module hole and the first fan.

4. Install and tighten the four M3 nuts on the corners of the Power Module.

5. Connect the fan connector to the vertical connector on the Power Module PC (AC configuration) board. The fan connector goes to the connector on the far left (closest to the fans).

6. Proceed to the following section "EXITING THE AREA".

EXITING THE AREA

1. Position Rear Panel with Power Module near the top and to the right (as you look down at the rear of the chassis.

2. Resting the bottom edge of the Rear Panel on the chassis rear edge, attach the green/yellow grounding wire to the chassis floor using an M4 nut.

3. Connect the cables to the rear of the Power Module. The left hand connector (as you look down) is to the fans, the middle connector is to the Motor Driver PC board power supply transformer, and the right connector is to the Power Supply Assembly (A10).

4. Rotate the Rear Panel up and over the mounting screw posts.

5. Use an M4 nut driver to attach the eight nuts to the screws around the perimeter of the Rear Panel.

6. Thread the tape drive power cord through the lower hole in the rear door of the cabinet.

7. Attach HP-IB cable (if this has been disconnected). Pass the cable out the hole halfway up the rear door of the cabinet.

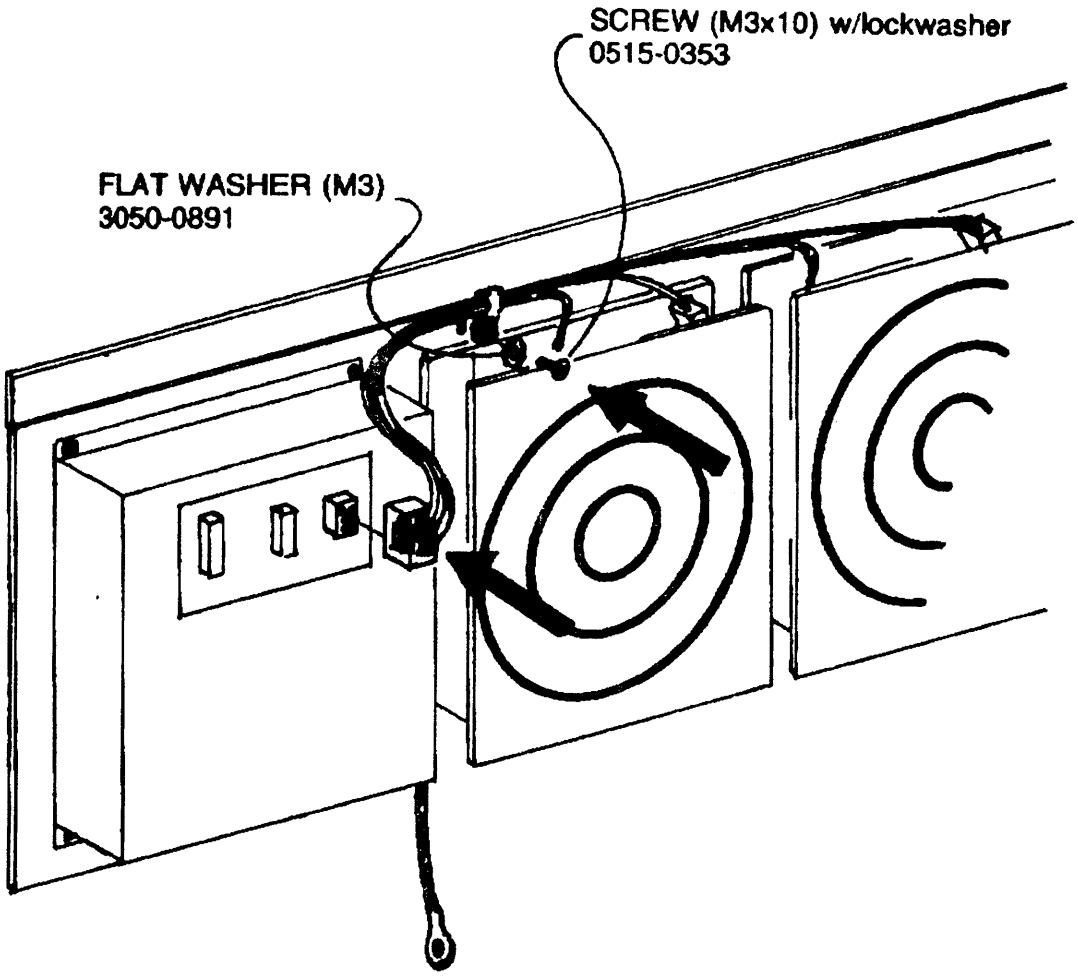


Figure (6) 2-28 Fan Power Cord

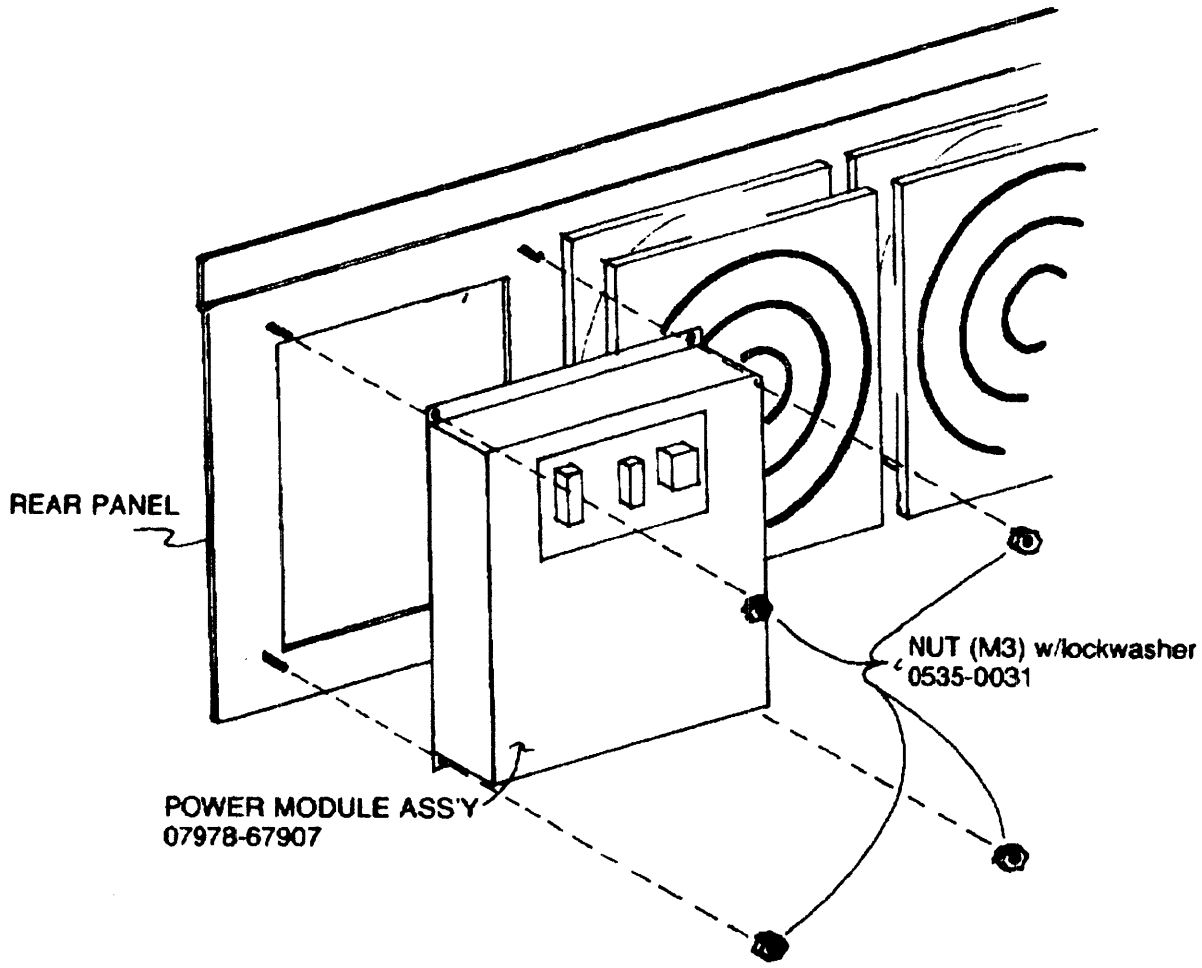


Figure (6) 2-29 Power Module Mounting

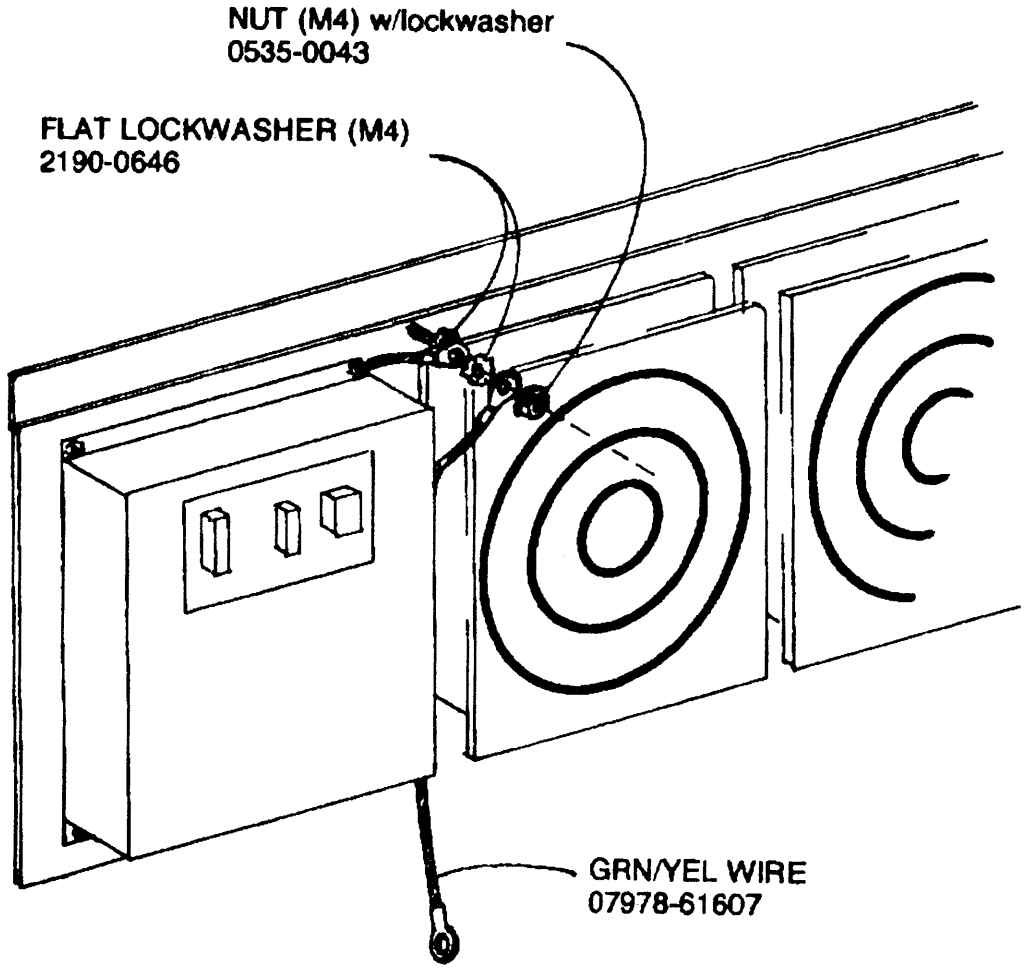


Figure (6) 2-30 Power Module Ground Strapping

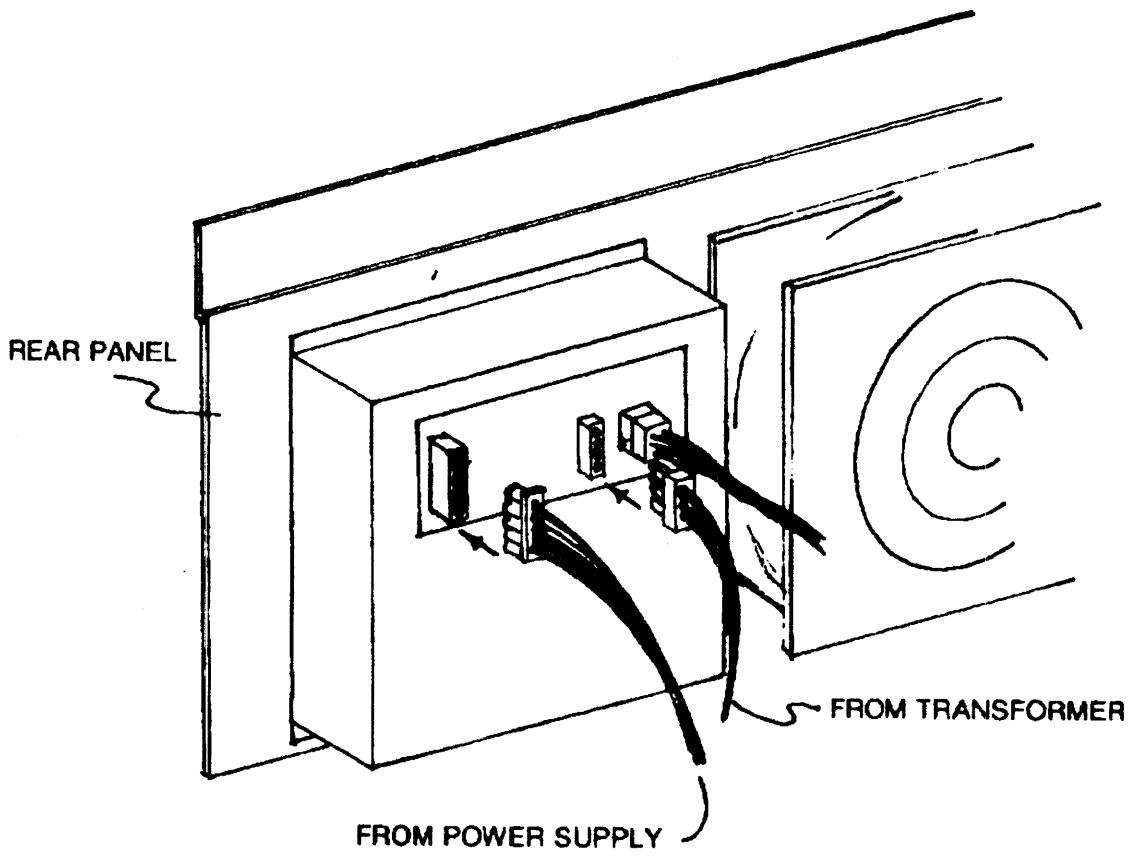


Figure (6) 2-31 Power Module Outputs

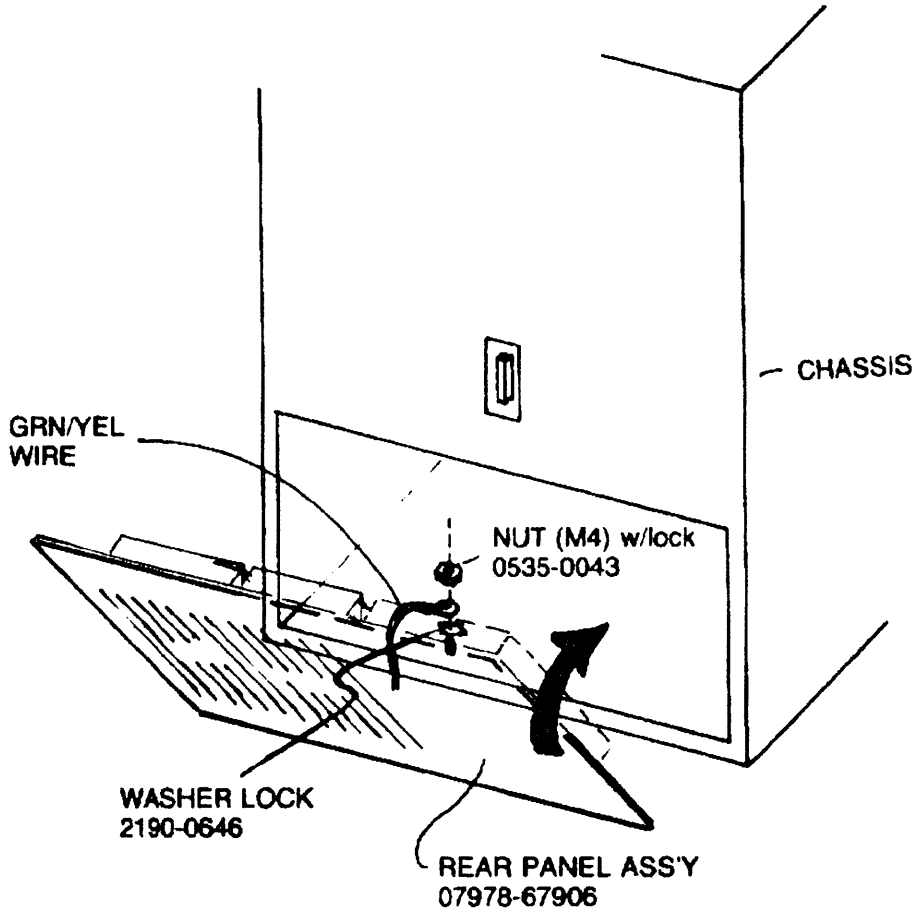


Figure (6) 2-32 Rear Access Panel

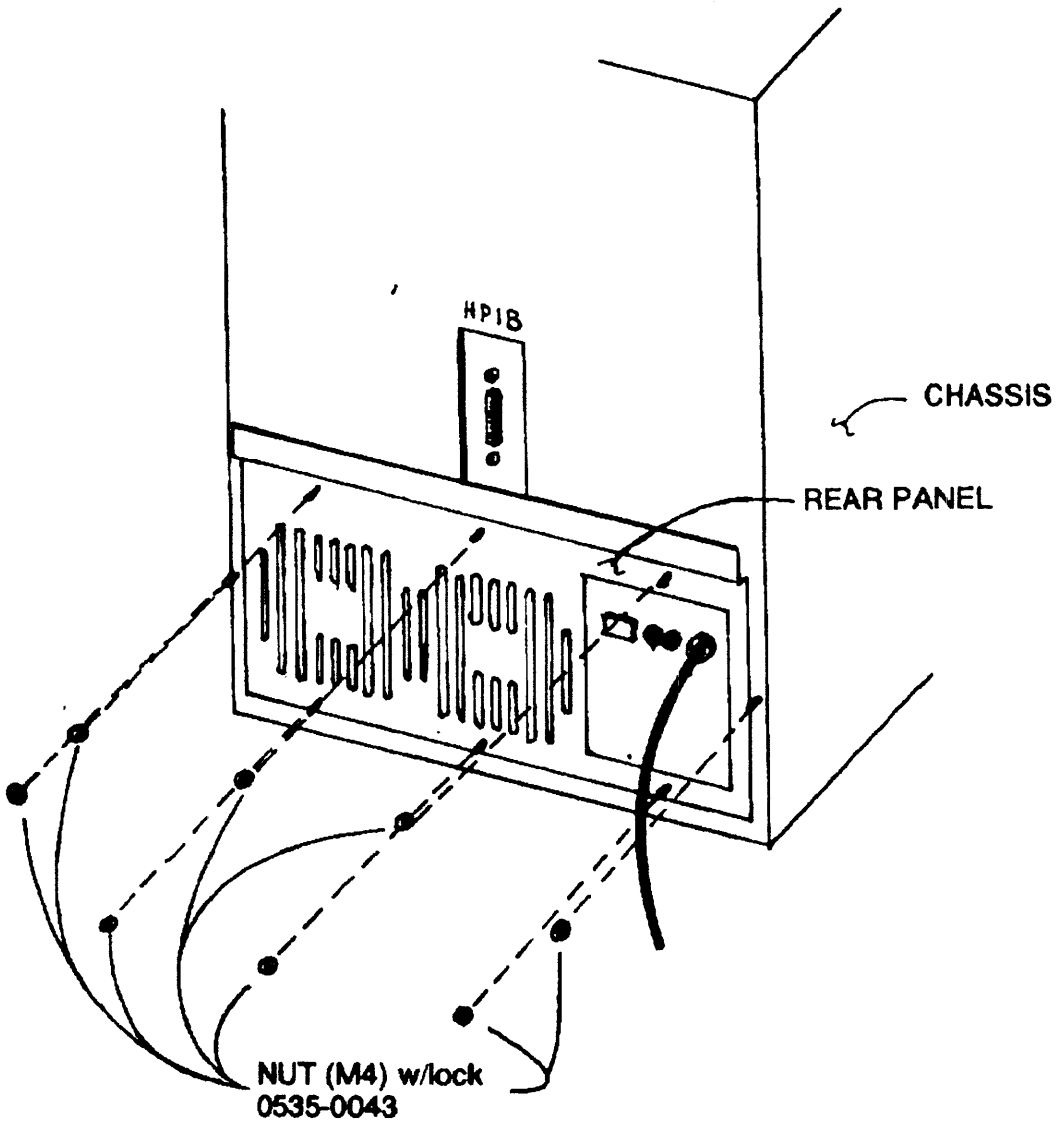
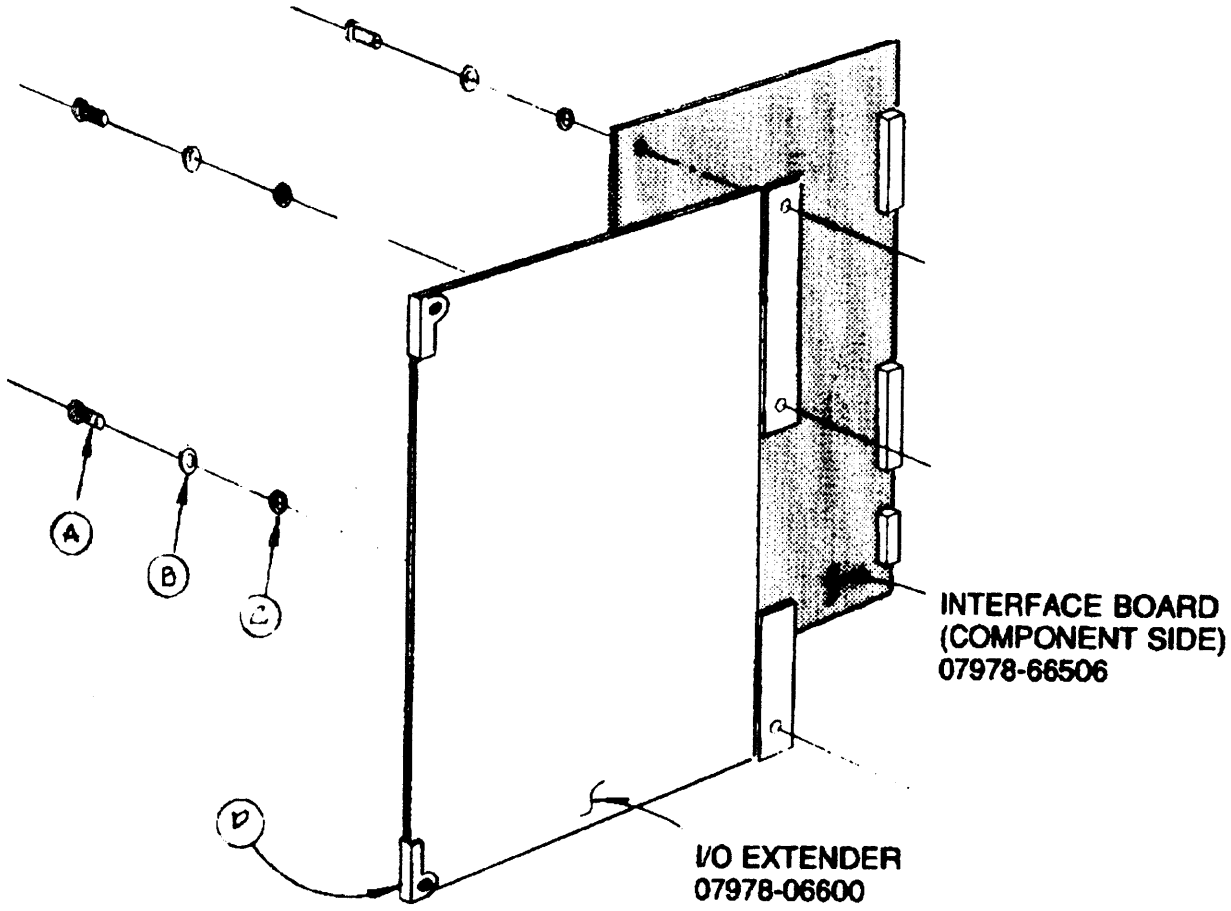


Figure (6) 2-33 Rear Access Nuts

2.8 MISCELLANEOUS- CHASSIS



A – SCREW (M3x6) 0515-0055
B – LOCKWASHER (M3)
C – PLASTIC LOCKWASHER 2190-0199
D – PCB EXTRACTOR 0403-0481

Figure (6) 2-34 HP-IB Extender

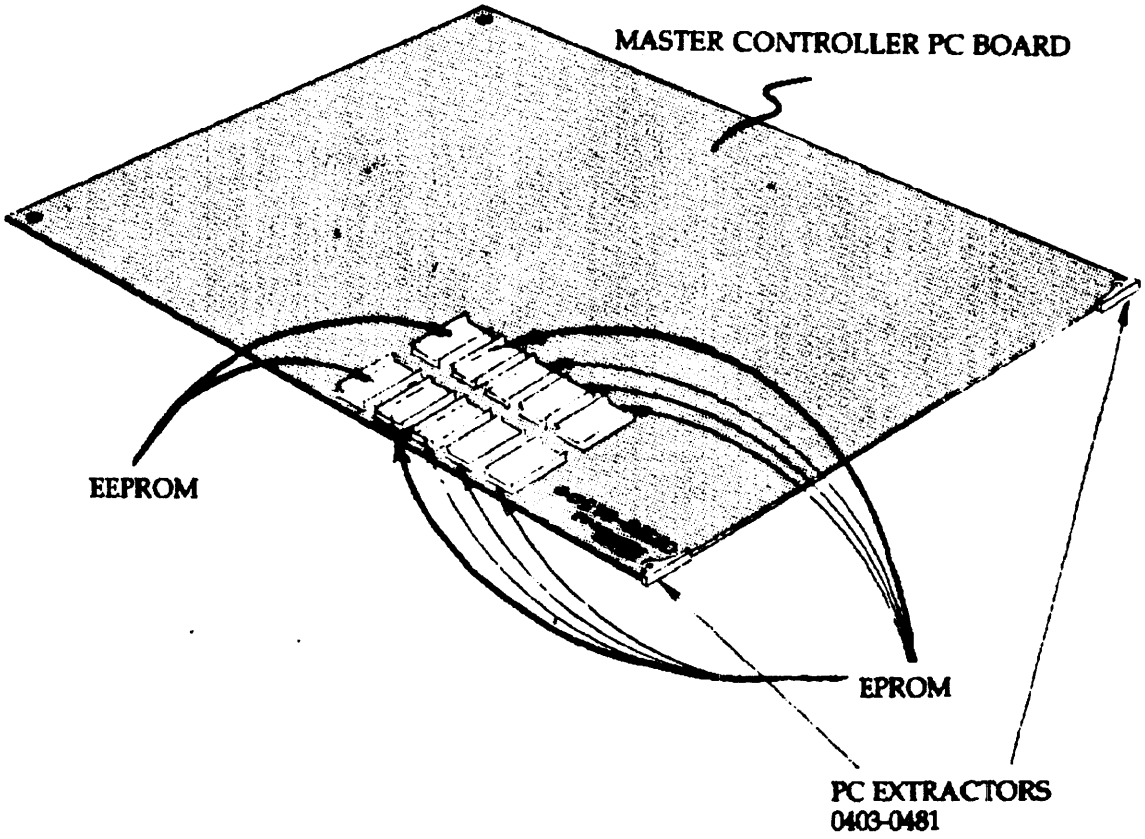


Figure (6) 2-35 Master Controller Board EPROM and EEPROM Sockets

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ADJUSTMENTS

VII ADJUSTMENTS

[1] FIRMWARE UPDATES

1.1 DESCRIPTION

The firmware update feature allows corrections to be made to the 7978A firmware without changing ROMs. Two 2K x 8 EEPROMS on the Master Controller Board are programmed with the updated firmware procedures and these procedures are then executed in place of the defective procedures.

The firmware may be updated either by what is known as a "local" firmware update or may be updated "remotely". A "local" update is made by mounting a tape containing the Firmware Update Record and executing Test 30 from the Front Panel of the drive. The second method, "remote" update, is accomplished by using a Host utility program which reads the Firmware Update Record into the Host computer (possibly over the phone) and then transfers this record into the tape drive. The "remote" update eases the problem of distributing update tapes.

This ability to update, while providing significant benefits, does have some drawbacks that must be watched carefully.

First, performing a firmware update in the field must be done carefully. If not done correctly, the tape drive firmware can be left in an indeterminate state and difficult-to-diagnose bugs may occur. The tape drive may even be made inoperable. Another potential problem might be the complexity of tracking which customers have which update.

GENERAL DATA STRUCTURE AND ALGORITHM

The EEPROM on the Master Controller Board is organized into a 1-byte wide and n-bytes long structure, where n equals the number of bug-fixed modules. Figure (7) 1-1 shows the structure of the EEPROM.

An indexing code is placed in the first area of EEPROM, depending on whether the module is bug-fixed (conatains a value of 2 or greater) or not bug-fixed (contains a 0). In the 7978A there are approximately 500 modules that could be bug-fixed, therefore the EEPROM is 1 byte wide and about 500 bytes long.

The next area in EEPROM consists of a data structure that is 2 bytes wide and 32 bytes long. This table starts with 2 and increments by 2. This area acts as an index into the next area of EEPROM which contains the actual code to bug-fix the module.

A description of the process is as follows:

Procedures in the 7978A are accomplished though a sequence of CALLS to subroutines. The first step in CALLing any subroutine in the procedure, however, is to find out whether the subroutine has been bug-fixed or not. If the subroutine has been bug-fixed, it will not be executed from ROM but from EEPROM.

In the example shown in the figure, a call is made to the subroutine 'Y'. Each byte in the first area of EEPROM is assigned to a different module and the check of the byte assigned to 'X' in this first area of EEPROM shows a value of, in this case, 2. Execution of this module, therefore, continues as a bug-fixed module.

The value found in the 'X-assigned' byte in EEPROM provides an offset value to be used to access the offset value (in the second area of EEPROM) of the new code (in the third area of EEPROM).

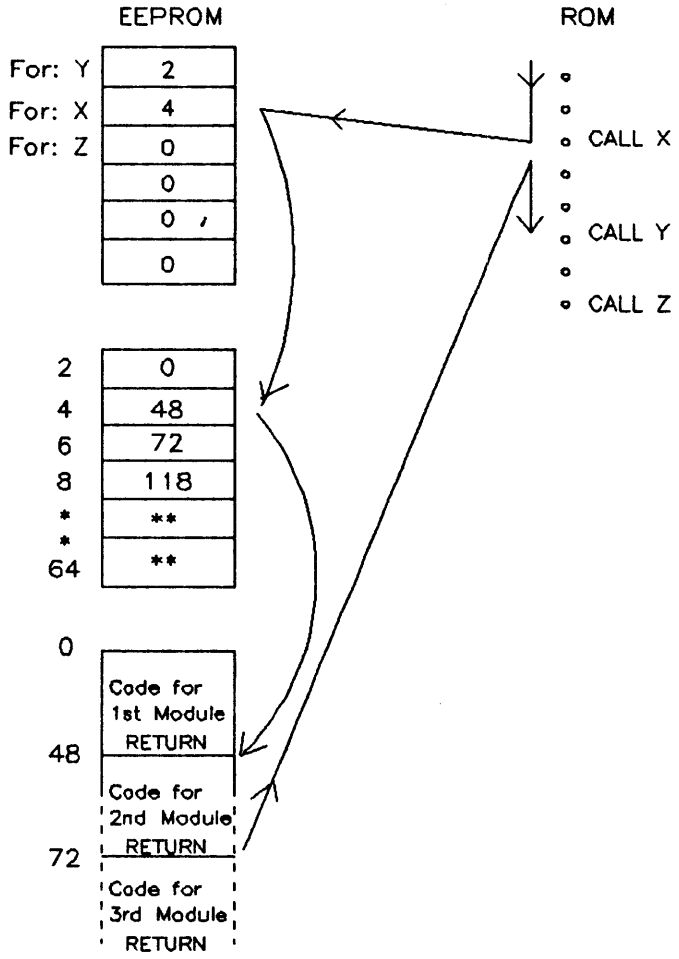


Figure (7) 1-1 EEPROM Data Structure and Algorithm

1.2 LOCAL UPDATE PROCEDURES

There are several steps involved to perform a local update. First, obtain a valid firmware update tape that contains the appropriate Firmware Update Record. Firmware Update Records are designed for a specific device (example: HP7978A or HP7974), and for a particular ROM release (Version 2, 3 etc.).

1. Mount and LOAD the tape on the drive. The normal load sequence is to be followed as outlined in Section III, INSTALLATION AND CONFIGURATION, of this manual or in Section III of the HP7978A OPERATOR'S MANUAL.

2. Select and execute diagnostics Test 27. This test will show the current ROM version number in the drive.

3. Select and execute diagnostics Test 30. After a short delay, the Front Panel display will begin flashing "00". This is a prompt meaning that the version number of the Update Record on the tape should be entered. This version number entered is both the ROM version number confirmed in Step 2 and the number of the update revision on the tape.

   Example: At introduction the HP7978A had a ROM revision number of "03" and a EEPROM update number of "00". The display will initiate the flashing "00" display (if no button is pressed in a few seconds) until the full sequence is entered.

   When the version number is fully entered, the drive will read the Update Record from the tape. After reading a valid record, the EEPROMS on the Master Controller board will be updated. This process takes up to approximately 20 seconds to complete.

   During the update, a countdown from 8 to 0 will be displayed on the Front Panel to provide feedback that the firmware update is proceeding normally. When zero is reached, the drive enters a power-on selftest.

4. At the completion of the power-on selftest, remove the firmware update tape.

If the RESET button is pressed during the update sequence, a "D4" will be displayed at the end of the countdown sequence. This code indicates that the power should be cycled and the ROMS changed. This is a special feature that allows a firmware update to be made prior to changing ROMS.

If the RESET button is pressed during the period of time that the version ID is to be entered, the update process will terminate.

Removing power from the tape drive during the execution of a firmware update may cause the drive to become inoperable.

ERROR MESSAGES DURING LOCAL UPDATE

The following list shows the error messages that could be displayed during the local update after a tape has been loaded. Refer to Section VIII, TROUBLESHOOTING AND DIAGNOSTICS for a description of the error messages that may be received during the LOAD sequence.

Error shown in display	Failure and recommended action
D201	Device program protocol error. Power cycle and repeat. May need to isolate failure using diagnostics.

D202	More than 7 retries have occurred while trying to read record. Repeat or get different update tape.
D203	Soft error occurred in trying to read the record. Repeat or get different update tape.
D204	Tape runaway in trying to read record. Most likely no record was written initially on the tape.
D310	The tape was not positioned at BOT. Check that tape is properly loaded and restart.
D340	A tape-related error occurred during the update. Repeat or get a different tape.
D345	EEPROM failure detected during a firmware update. Check out EEPROM circuits with associated tests.
D350	A valid Firmware Update Record was not found. Repeat or get different update tape.
D368	Firmware update is too big. Verify that update tape is correct one.
D369	Invalid ID for firmware update. Re-enter version number or get correct tape.
D36A	Invalid version ID. Re-enter version number or get correct tape.
D36B	Bad firmware update checksum. Retry tape or get different tape.
D36C	Less than the minimum four bytes of data were contained in the update data record. Retry tape or replace.
D36D	An odd number of bytes was in the Firmware Update Record. Retry tape or replace.
D36E	Wrong update for current ROM revision. Replace update tape with correct one.
D36F	RESET button was pressed instead of entering a version number on the Front Panel. This may be what was intended. Exit diagnostics or repeat update procedure.

1.3 REMOTE UPDATE PROCEDURES

Most of the details of a remote update are dependant upon how the Host implements the feature. At CSY, the procedure is to sign onto the 32340 group of the support account. An application program is run that searches in the 32340 group for the filename to download. A device file is opened which requires that the Antelope have a scratch tape loaded (!). (This will change with a new version of Sherlock in the future). At this point, the user performs the same sequence of operations as with the local update. The user will enter the code on the front panel and observe the same countdown message from 8 to 0. At the conclusion of the update, either the power is cycled or self-test is run depending upon whether or not the reset button was pressed during the update (but after correct entry of the version ID).

ERROR MESSAGES DURING REMOTE UPDATE

The error codes returned from the drive during a remote update are a subset of those listed in the ERROR MESSAGES DURING LOCAL UPDATE. Not included are error codes that relate to tape loading errors or errors in reading the record from the tape. Note that a remote update could have HPIB transfer errors. In this event, loopback tests

and data buffer tests should be performed to isolate failures.

1.4 ROM CHANGE PROCEDURE

No standard procedure for changing ROMS is included in this manual.

Each ROM change will be accompanied by written instructions specifying a strict sequence of operations which must be performed exactly to successfully complete the change. This method has been adopted to help prevent possible problems caused by having drives in the field with differing software.

Also, changing ROM may require modifications to EEPROM. This is because the EEPROM may have firmware updates present that are valid with one ROM revision but totally incorrect for a subsequent revision.

A new procedure will probably be specified for each ROM update.

Changing ROMS also requires some modifications to the EEPROMS. This is because the EEPROM may have firmware updates present that are valid with one ROM revision but totally incorrect for a subsequent revision.

VIII TROUBLESHOOTING AND DIAGNOSTICS

[1] TROUBLE > SYMPTOM > PROBABLE CAUSE > ACTION TAKEN

1.1 DIAGNOSTIC INTERPRETATION

DIAGNOSTIC ERROR MESSAGE DESCRIPTION

A diagnostic error message is generated whenever a diagnostic is executed. When a diagnostic fails, the error message is stored into an error message log. This log will contain the ten most recent failed error messages.

The error message cannot be written to the front panel or returned to the Host in its entirety. For that reason, the error message is divided into two halves. The first half (MSB) of the error message contains the failed FRU and the subsystem, within the failed FRU, which was detected as an error. The second half (LSB) of the error message contains a multi-test code and a code indicating what action was used to cause the failure, or a firmware or Host protocol error. The multi-test code is used when a diagnostic test covers more than an unique interface or hardware function which may cause the diagnostic isolation to a specific FRU to be incorrect. See the multi-test table in the appendix.

The Host will request the error message when a diagnostic fails.

Diagnostics requested from the Front Panel call diagnostic test 0 to display the error message when the test is completed.

DIAGNOSTIC FRU TABLE

Abbreviation	Description	FRU Error Code (MSB)
	No Status Available	00H
SC	Servo Controller Assembly	1xH
MDRIVE	Motor Drive Assembly	2xH
FP	front panel Assembly	3xH
MC	Master Controller Assembly	4xH
F	Formatter Assembly	5xH
HP-IB	HP-IB Assembly	6xH
WE	Write Electronics Assembly	7xH
RE	Read Electronics Assembly	8xH
PLL	Phase Lock Loop Assembly	9xH
P	Preamp Assembly	ni*
Head	Head Assembly	ni*
Motors	Two Motors	ni*
MB	Mother Board	ni*
Tape	Tape Medium	ni*
	Runtime-Detected Errors	DxH
	Firmware Failure	ni*
	Protocol Errors	ExH
	Remote Status	FxH

* ni Indicates the assembly is not isolated.

DIAGNOSTIC TESTS

Codes*	Test # (Decimal)	Test	FRU's Tested**
L,U	0	Display_Error	N/A
L,U	1	Display_Error_Log	N/A
R,L,U	2	Clear_Error_Log	N/A
L,U	3	Power-on self test failure override.	
R,L,T,I,Off	4	Power-on self test	MC, HP-IB, F, WE, PLL, SC
R,L,T,I,Off	5	Master Controller PON Test	MC, HP-IB, F, WE, PLL, SC
R,L,T,I	6	Kernal_MC_Tests	MC
R,L,U	7	Front_Panel_Display	FP
R,L,T,I	8	Walking_RAM_Tests	MC
R,L,T,I	9	Timer_Tests	MC
R,L,T,I	10	EEPROM_Read_Test	MC
R,L,T,I	11	Data_Buffer_Tests	MC
R,L,T,I	12	Write_Clock_Test	WE
R,L,T,I	13	HP-IB_Internal_Loopback	HP-IB
R,L,T,I	14	HP-IB_DB_Loopback	HP-IB, MC
R,L,T,I	15	Digital_Loopback	F, PLL, WE, MC
R,L,T,I	16	Read Board Present test.	RE
R,L	17	Non-existent test.	
R,L	18	Non-existent test.	
R,L,T	19	EEPROM_Write_Test	MC
L,U	20	Front_Panel_Confidence_Test	FP
R,L,T,I,W,On	21	Write_PE_Data_Block	MC, F, PLL, WE, P, RE, SC, Head, Motors, Tape Medium
R,L,T,I,W,On	22	Write_GCR_Data_Block	same as test #21
R,L	23	Non-existent test.	
R,L,U	24	Auto_Gain_Value_Update	RE
L,U	25	Set_To_Single_Looping	N/A
L,U	26	Set_To_Infinite_Looping	N/A
L,U	27	Display_MC_Revision	N/A
L,U	28	Display_Tape_Odometer	N/A
L,U	29	Display_Densities_Supported	N/A
L,U	30	Local_Firmware_Update	N/A
R,L,U	31	Set_Write_Test_Reposition	N/A
R,L,U	32	Set_Write_Test_To_Walk	N/A
R,L,T,I,W,On	33	Read_PE_Data_Block	MC, F, PLL, WE, P, RE, SC, Head, Motors, Tape Medium
R,L,T,I,W,On	34	Read_GCR_Data_Block	same as test #33
R,L,U,On	35	BOT_EOT_Erase_Test	
R,L,U,On	36	BOT_EOT_PE_Write_Test	
R,L,U,On	37	BOT_EOT_GCR_Write_Test	

R,L,U,On	38	BOT_EOT_PE_Read_Test	
R,L,U,On	39	BOT_EOT_GCR_Read_Test	
L,U	40	Worst_Case_Servo_Reposition	
R,L,T,I,Off	41	SC_MC_Handshake	SC, MC
R,L,T,I,Off	42	SC_Power_On_Test	SC
R,L,T,I,Off	43	SC_Board_Test	SC
R,L,T,I,Off	44	SC_Gap_Interrupt_Test	SC, F, MC
L,T	45	SC_Buffer_Arm_Interactive_Test	
L,T	46	SC_Speed_Encoder_Inter_Test	
R,L	47	Non-existent test	
L,U	48	Display_SC_Revision	N/A
R,L,T,I,Off	49	SC_Sensor_Test	SC
R,L,T,I,Off	50	SC_Connector_Test	SC
R,L,T,I,Off	51	SC_Shutdown_Test	SC
R,L,T,I,Off	52	SC_Comparator_Test	SC
R,L,T,I,Off	53	SC_DAC_Test	SC
R,L,T,I,Off	54	SC_State_Machine_Test	SC
R,L,T,I,Off	55	SC_Interrupt_Test	SC
L,T	56	SC_BOT_EOT_Sensor_Test	SC
R,L,T,I,Off	57	SC_Power_On_Tests	SC
L,T	58	SC_Partial_Interactive_Test	
L,T	59	SC_Scope_Interactive_Test	
	60-255	Non-existent tests.	

* R -- Remote access is from the Host via the HP-IB.
L -- Local access is by User input from the front panel.
U -- The diagnostic is a utility.
T -- The diagnostic is a test.
I -- A diagnostic test may also be executed in an infinite loop, rather than the default of single execution.
W -- A read or write tape test may be "walked" down the tape, rather than the default of repositioning after each data block.
On - Remote access to diagnostics only when drive is online.
Off Remote access to diagnostics only when drive is offline.

** Reference the Diagnostic FRU Table for FRU code explanation.

SPECIAL REMOTE DIAGNOSTICS

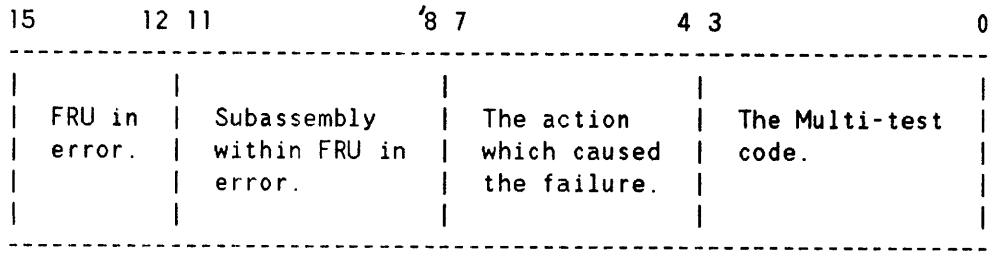
NOTE

The following diagnostics are available to the HOST via talk secondary and listen secondary protocol commands.

```
Listen 30  Send loopback data from the Host to HP-IB.
Talk 30    Return the loopback data from the HP-IB to the Host.
Listen 3   Download a diagnostic test to BUCKHORN.
           The downloaded diagnostic must be in the form:
           DOWNLOAD ID  = 4E72H
           DOWNLOAD CHECK SUM = 16 bit number created by adding the
                                download data as 8 bit data.
           THE DOWNLOAD.  THE FIRST 16 BITS SHOULD BE A VALID MC68000
                          OPCODE.
Talk 4     Return the downloaded diagnostic results to the Host.
Listen 6   Remote Firmware Update.
           REMOTE UPDATE ID = 66xxH  The xx version number of the
                                     code update in hex.  (0-63H)
           ROM ID = xxH  The ROM ID will contain a value in the
                         range 0-99 (0-63H).
           REMOTE UPDATE CHECK SUM = 16 bit number created by adding
                                     the update data as 8 bit data.
           UPDATE DATA = 4068 bytes (8 bit) of data.
Talk 6     Return the Firmware Update Data from EEPROM.
           FIRMWARE UPDATE ID = 7F06H
           ROM IO = xxH  The ROM ID will contain a value in the
           CHECK SUM = 16 bit number created by adding the firmware
                       update data as 8 bit data.
           FIRMWARE UPDATE DATA = 4068 (8 bit) bytes of data.
Talk 5     Return BUCKHORN Status from EEPROM and RAM.
           IMAGE DUMP ID = 0407H
           IMAGE DUMP CHECK SUM = 16 bit number created by adding the
                                  image dump's data as 8 bit data.
           IMAGE DUMP DATA = 4124 bytes (8 bit) data.
```

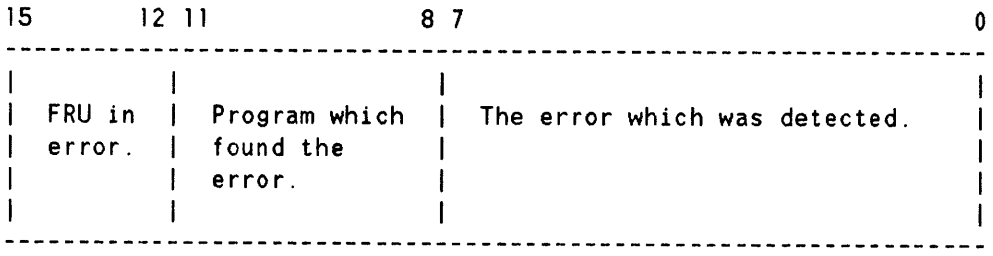
ERROR FORMATTING

GRAPHICAL BREAKOUT OF THE DIAGNOSTIC ERROR MESSAGE



OR

Protocol and Firmware Generated Error Message.



DIAGNOSTIC ERROR CODES

1xx0H Servo Controller assembly FRU.

10xxH A general problem was found with the Servo Controller.

1001H The Servo Controller was unable to perform a soft shutdown during an Unload operation.

1010H The Servo Controller experienced an unexpected loss of tape tension.

1021H The Servo Controller detected that connector J25 is disconnected.

1022H The Servo Controller detected that connector J26 is disconnected.

1023H The Servo Controller detected that connector J27 is disconnected.

1024H The Servo Controller detected a failure on the Buffer Arm assembly.

1025H The Servo Controller was unable to open its relay.

1026H The Servo Controller was unable to close its relay.

1027H The Servo Controller detected a failure in its external counter.

1028H The Servo Controller detected a direction bit failure.

1029H The Servo Controller detected a failure in its internal counter.

102AH The Servo Controller detected a failure in its Quadrature circuitry.

102BH The Servo Controller detected MOT1__FAIL__NEG.

102CH The Servo Controller detected MOT1__FAIL__POS.

102DH The Servo Controller detected a sensor test failure.

102FH The Servo Controller DAC failed uner 0 volts.

1030H The Servo Controller DAC failed over 0 volts.

1031H The Servo Controller DAC failed under -6 volts.

1032H The Servo Controller DAC failed over -6 volts.

104xH Invalid two-port RAM value.

105xH Invalid diagnostic parameter.

1060H The Servo Controller detected an in-position echo failure.

1061H The Servo Controller detected a gap echo failure.

1070H Requested moving fast while not moving at -75 ips.

1080H Reposition overflow.

1081H Not in moving state when an in-position interrupt occurred.

1082H In-position interrupt sign error.

10DxH Servo firmware error.

10ExH Servo table lookup error.

12x0H A Servo Controller related error has been detected by the Master Controller.

1210H The Servo Controller found an error in its kernal test.

1220H The Servo Controller failed the interface test with the Master Controller.

1230H The Servo Controller failed the gap interrupt test.

1240H An in-position interrupt was not received.

1250H A gap interrupt was not received.

1260H The write enable signal was not high in the sensor test.

1270H The write enable signal was not low in the sensor test.

12F0H The Servo Controller was not present or responsive.

3xx0H Front panel assembly FRU.

3F00H The hardware is not present or responsive.

4xx0H Master Controller assembly FRU.

41x0H CPU error on Master Controller assembly.

4110H CPU data register malfunction. The data value written was not the value read while verifying.

4120H CPU address register malfunction. The data value written was not the value read while verifying.

4130H CPU condition code malfunction.

4140H A CPU register had it's data fade after a two second wait.

4160H CPU addressing malfunction.

42x0H Master Controller RAM failure.

4220H RAM failure found during the selective one walking bit test.

4230H RAM failure found during the selective zero walking bit test.

43x0H Master Controller Data Buffer subassembly failure.

4310H Data Buffer RAM failure in marching RAM test.

4320H Data Buffer register failure in walking '1' bit test.

4330H Data Buffer register failure in walking '0' bit test.

4340H Data Buffer length counter/USM function failure.

4350H Data Buffer usage counter/USM function failure.

4360H Data Buffer parity/USM function failure.

4370H The data transferred was not received. Possible HP-IB problem.

4380H The data transferred is missing an EOR. Possible HP-IB problem.

44x0H Master Controller timer chip subassembly failure.

4410H Timer interrupt status error.

4420H Timer interrupt status could not be cleared.

4430H Timer 1 didn't count down to zero.

4440H Timer 1 or timer 2 is substantially faster than the other timer.

4450H Timer 1 or timer 2 is substantially slower than the other timer.

4460H Timer 1 or timer 3 is substantially faster than the other timer.

4470H Timer 1 or timer 3 is substantially slower than the other timer.

45x0H Master Controller EEPROM chip subassembly failure.

4510H The read/write ready status was not present.

4520H The computed EEPROM check sum was not the same as the stored check sum.

4530H An EEPROM read value was incorrectly read.

4540H A write value into the EEPROM did not verify after write.

4550H The computed EEPROM check sum did not verify after being written.

4560H The EEPROM is write enabled when it should be disabled.

4570H The EEPROM is not write enabled when it should be enabled.

45H Master Controller EEPROM failure during a firmware update.

46H Master Controller ROM checksum failure.

5xyzH Formatter assembly FRU.

y denotes an event.

y=1 Write ID y=2 Write Data

y=3 Verify Data y=4 Write a Tape Mark

y=5 Force 1 track in error y=6 Force 2 tracks in error

y=7 Force unrecoverable data y=8 Force a Parity error

y=9 Force data overruns y=A Force data underruns

z denotes a multi-test code.

51yzH Write Formatter failure.
5sssH Hardware status at time of error detection.

52yzH Data Detect and Deskew failure.
5sssH Hardware status at time of error detection.

53yzH Read Formatter failure.
5sssH Hardware status at time of error detection.

5sssH Hardware status at time of error detection.
Bits 1-0 Write Formatter status.
Bits 7-0 Data Detect and Deskew status.
Bit 11 Parity or bad data in buffer status.
Bits 10-0 Read Formatter status bits 14-4.

6xx0H HP Interface Bus (HP-IB) assembly FRU.

61x0H HP-IB failure.

6110H The inbound FIFO was not empty after an attempt to clear.

6120H The internal HP-IB loopback has failed.

6130H The 'end' bit in the interface is not functional.

62x0H HP-IB/Master Controller interface failure.

6210H The data transferred was not received. Possible Data Buffer problem.

6220H The data transferred was missing an EOI. Possible Data Buffer problem.

7xx0H Write Electronics assembly FRU.

71x0H Write Clock failure.

7110H The GCR Density frequency is not working.

7120H The GCR Data frequency is not working.

7130H The PE Density frequency is not working.

7140H The PE Data frequency is not working.

8xx0H Read Electronics board FRU.

8abcH Auto-gain error code. Parameter 0 indicates which tracks are bad by putting a '1' in the track fields. Parameter 1 indicates low or high amplitude by putting a '0' or '1' in the indicated tracks for low or high, respectively. Note: The high order bit is 15, while the low order bit is 0.

a Bit 11 contains the parameter. Bits 10-9 contain the density. (PE=2,GCR=3) Bit 8 contains track 9 data.

b Bits 7-4 contain tracks 8-5.

c Bits 3-0 contain tracks 4-1.

9xx0H Phase Locked Loop (Clock Recovery) assembly FRU.

y denotes an event.

y=1 Write ID y=2 Write Data

y=3 Verify Data y=4 Write a Tape Mark

y=5 Force 1 track in error y=6 Force 2 tracks in error

y=7 Force unrecoverable data y=8 Force a Parity error

y=9 Force data overruns y=A Force data underruns

z denotes a multi-test code.

91yzH An error was detected while accessing the Write Formatter.

92yzH An error was detected while accessing the Data Detect and Deskew.

93yzH An error was detected while accessing the Read Formatter.

Note: The next error code contains status as explained under 5sssH.

BxH Unexpected exceptions. Front panel reportable only.

B1H Address error exception.

B2H Illegal instruction exception.

B3H Divide by zero exception.

B4H Register bounds violation exception.

B5H Overflow exception.

B6H Privilege violation exception.

B7H Trace exception.

B8H Emulation of future instruction exception.

B9H Spurious interrupt exception.

BAH Unimplemented interrupt exception.

BBH Unassigned vector exception.

Bus Error Exceptions. Front panel reportable only.

43H The Master Controller Data Buffer subassembly is unresponsive.

51H Write Formatter is unresponsive.

52H Data Detect and Deskew is unresponsive.

53H Read Formatter is unresponsive.

61H The HP-IB is unresponsive.

C1H Bus error exception from an unknown source has occurred.

Halted state error codes. Front panel reportable only.

41H MC68000 CPU error.

42H Master Controller RAM failure.

45H The EEPROM failed during a firmware update.

46H Master Controller ROM failure.

D4H Power cycle the tape drive. Firmware update is complete.

DxxxH Runtime-Detected errors.

D0xxH Operating System detected failure.

D1xxH Channel Program detected failure.

D179H Transaction ID mismatch.

D17AH Missing pending command.

D17BH Report Queue error.

D17CH Report Queue full.

D17DH Unknown command to device program.

D17EH Full Command Queue.

D17FH Unknown non-Host command.

D183H Data buffer byte count mismatch. (Test MC)

D184H Bad message type.

D185H Process handshake abort. (Test HP-IB)

D186H Interface exception. (Test HP-IB)

D187H Outbound data freeze. (Test HP-IB)

D188H Inbound interface FIFO error. (Test HP-IB)

D189H EEPROM update failure. (Test MC)

D18CH Channel Program case error.

D1FFH Device Program is unresponsive to the Channel Program.

D2xxH Device Program detected failure.

D201H A timeout on a Device Program report occurred.

D202H More than seven (7) retries have occurred during a tape diagnostic.

D203H A soft error has occurred during a tape diagnostic.

D205H The tape is write protected.

D209H The read record/move command returned an unidentifiable tape.

D20AH The write gap/tape mark record command returned an unidentifiable tape.

D210H The tape is not at load point.

D213H Backward move command while tape is at load point.

D225H Tape positioning failure. (Test SC)

D226H System Reset.

D227H Readahead Reject.

D228H The door was open, so reject the command.

D229H Velocity is out of specification. (Test SC)

D22DH Multiple tracks were in error. (Test F)

D22FH Tape mark or ID was not verified. (Test F)

D230H Gap noise was detected. (Test F)

D231H Data format error. (Test F)

D232H Not identifiable on load or rewind commands. (Test F)

D233H Gap before end of data. (Test F)

D234H Data block dropout. (Test F)

D235H Redundancy error. (Test F)

D236H Read parity errors. (Test F)

D23CH Data Buffer overrun. (Test MC)

D23DH Data block timeout. (Test F)

D23EH Tape mark dropout. (Test F)

D23FH Tape mark unverified. (Test F)

D240H Tape mark timeout. (Test F)

D251H Servo Controller is unresponsive. (Test SC)

D252H Servo Controller command not complete.

D253H The Servo Controller shutdown. (Test SC)

D254H Servo Controller hardware failure. (Test SC)

D255H Servo Controller protocol error. (Test SC)

D256H Servo Controller runtime error. (Test SC)

D257H No in-position interrupt. (Test SC)

D258H No gap position interrupt. (Test SC)

D259H Safety shutdown. (Test MDRIVE)

D25AH No BOT marker.

D25BH Speed out of specification. (Test SC)

D25CH Desired state is invalid.

D25EH Tape position failure. (Test SC)

D265H Read Formatter unresponsive. (Test F)

D266H Read Formatter hardware error. (Test F)

D267H Bad detect on write. (Test F)

D268H Bad erase. (Test WE)

D269H No detect on write. (Test F, WE)

D26AH Track out of syncronization. (Test F)

D26EH Formatter byte count mismatch. (Test F)

D27CH Report Queue overflow.

D27DH Unknown command.

D280H No end of record on a write record. (Test F, MC)

D283H Data Buffer byte count mismatch. (Test MC)

D28AH Device Program case error.

D28BH Device Program hardware utility case error.

D3x0H Diagnostic Program detected failure.

D310H No tape was loaded when a read or write data block test was called.

D320H A tape with the wrong density ID was loaded for a read data block test.

D330H No write ring was installed on the tape loaded for a write date block test.

D340H A tape-related error was occurred during a local firmware update.

D345H EEPROM failure was detected during firmware update.

D350H A valid firmware update record was not found on the loaded tape.

D360H The EEPROM READY signal did not come true during a Tape Usage Odometer update.

D364H Download is too large.

D366H Invalid download ID.

D367H Incorrect Download checksum.

D368H The firmware update will not fit into EEPROM. Aborted.

D369H Invalid ID for a firmware update.

D36AH Invalid version number for the firware update. (Not found.)

D36BH Bad firmware update checksum.

D36CH Insufficient data for the firmware update.

D36DH Odd number of bytes for a firmware update.

D36EH The requested version number is incorrect for your installed ROM (PROM). No update was performed.

D36FH Firmware update has been aborted.

D370H The door was open while attempting to run a servo controller test which requires the door to be closed.

D380H Servo handshake/hardware failure during tests 35 - 40.

D390H A tape is mounted on the drive during motor drive tests.

D4H Power cycle the tape drive. Firmware update has successfully completed.

ExxxH Protocol errors.

E079H Command Queue not empty.

E0A2H Request DSJ expected.

E0A3H Request status expected.

E0A5H Unknown unit select.

E0A6H Listen 1 expected.

E0A7H Data byte expected.

E0A8H Missing EOI on data byte.

E0AAH Command phase protocol error.

E0ACH Read record report phase protocol error.

E0ADH Report phase protocol error.

E0AEH Cold load protocol error.

E0B0H End "complete" or "Complete - idle" expected.

E0B2H End "Data" expected.

E0B4H Improper secondary.

E0B5H Misplaced data byte.

E0B8H Interface loopback protocol error.

E0B9H Self test protocol error.

E0BCH Command parity error.

E0BDH Reset by the operator.

E0BEH Device clear received.

FxxxH Remote status.

FCFCH Only local access to diagnostic allowed.

FDFDH Incorrect Online/Offline mode for a diagnostic.

FEFEH Non-existent diagnostic.

FFFFH Diagnostic passed.

Front panel errors and warnings.

A1H Resetting the Device Program.

A2H Drive is active and is offline.

A3H Dirty tape path warning.

F0H Self test failure.

F1H The tape is not tensioned.

F2H BOT marker is not present.

F3H Hardware failure.

F4H Firmware error.

F5H Host protocol error.

Multi-Test Codes

The multi-test code within the LSB of the diagnostic error message is used to supply additional information about what may really have failed. An FRU and subsystem FRU will be contained in the MSB of the diagnostic error message, but may reflect a symptom rather than error isolation. The multi-test code is used to provide subsequent FRU's which may have caused the failure. The FRU's are listed below from most likely to fail to least likely to fail.

xxx1H Digital Loopback w/PLL Test -- PE	PLL, F, MC, WE.
xxx2H Digital Loopback w/PLL Test -- GCR	F, MC, WE.
xxx3H Digital Loopback w/o PLL Test -- PE	F, MC, WE.
xxx4H Digital Loopback w/o PLL Test -- GCR	F, MC, WE.

1.2 EXECUTING A DIAGNOSTIC TEST FROM THE FRONT PANEL

The following procedures describe the entering and execution of diagnostic tests from the front panel.

CAUTION

Execution of Test 24 changes the characteristics of the tape drive.

Tests 21, 22, 35, 36, and 37 write data, or an erase signal, to tape. Data currently on a tape is overwritten.

Other tests could cause loss of tape position information.

NOTE

A diagnostic test may not be executed when the drive is displaying a warning or error message. To clear a warning or error condition, press the RESET button. The display will clear and the status light will change to green.

If the error condition was caused by a failure in the power-on sequence, pressing the RESET button will clear the **F0** message from the display but the STATUS light remains red. This is the only situation where a diagnostic test may be initiated with a red STATUS light on.

Procedure:

1. Go offline

2. Press the TEST/ADDRESS button. The TEST light will come on and the STATUS light will go out.

3. Press the ENTER button to select the test mode. If the ENTER button is not pressed within 10 seconds, the selection process is aborted. When the process is aborted, the TEST light goes out and the STATUS light will come on green (the STATUS light comes on red if this process was initiated from a power-on failure condition).

4. The function of the TEST/ADDRESS button changes when the ENTER button is pressed. Pressing the button now increments the number in the display by one. If the button is held down, the display increments twice per second. The REWIND button may be used while in this mode to increment the display by 10. Use any of these methods to increment the display to the desired test number.

5. Press the ENTER button within 10 seconds of completing Step 4. The STATUS light briefly flashes amber as the execution command is accepted and the test called by the number in the display is executed.

The BUSY light remains on continuously during the execution of the test. When the test completes, the BUSY light goes off. If the test passed, the STATUS light will be green. If the test failed, the STATUS light will be red and there will be an alphanumeric service code in the display.

If the test passed, but the diagnostic test was executed after a power-on fail condition (see previous NOTE), the STATUS light will come on red but there will be no service code in the display.

PROBLEMS

Cannot Find BOT During Load Sequence

1. Unload the tape.

2. Check for presence of a reflective BOT marker tape within approximately 30 feet of the physical beginning of the tape. If marker is absent, replace marker.

3. If marker is present, check that nothing is covering BOT/EOT sensor windows.

4. Execute Test 5. If no error results from Test 5, execute Test 57 (see **Executing Diagnostic Tests From The Front Panel**). Record any error code that may appear. Contact your nearest Hewlett-Packard Sales and Support Office.

No Front Panel Lights

1. Check that the tape drive is plugged into the power receptacle.

2. Check that the power switch is on. The switch is located on the back panel of the drive electronics enclosure inside the cabinet.

3. If the power switch is on, press it again to remove power. Check the condition of the right-hand fuse (F2). This fuse is in the power supply to the logic circuits. Replace if necessary. Press the power switch again to apply power.

CAUTION

Replace the fuse with with one of the same rating.

4. If the problem has not been found, call the nearest Hewlett-Packard Sales and Support Office.

Tape Loses Tension

1. Check your mounting procedure. The tape should be wound around the takeup reel hub approximately three times to provide proper grip. All slack should be taken out before a Load command is given.

2. If this problem persists during normal operations, contact the nearest Hewlett-Packard Sales and Support Office.

Error Message When Power Is Applied

F0 is the only error code you should receive as a first display after power is applied to the tape drive. This error means that a test in the power-on sequence has failed.

1. Recycle power using the power switch located on the back panel of the drive electronics enclosure inside the cabinet.

Warning Message A3 Remains In Display After Tape Is Unloaded

The **A3** warning indicates a soft error rate above an allowable threshold (see Subsection 4.2). The usual cause for this message is a dirty tape path. Next in probable causes is a worn out or dirty tape. Finally, there is the possibility of a hardware failure.

1. Ensure tape drive is being maintained in accordance with the procedures outlined in Section IV, "PREVENTIVE MAINTENANCE".

2. Clean tape path as explained in Section IV.

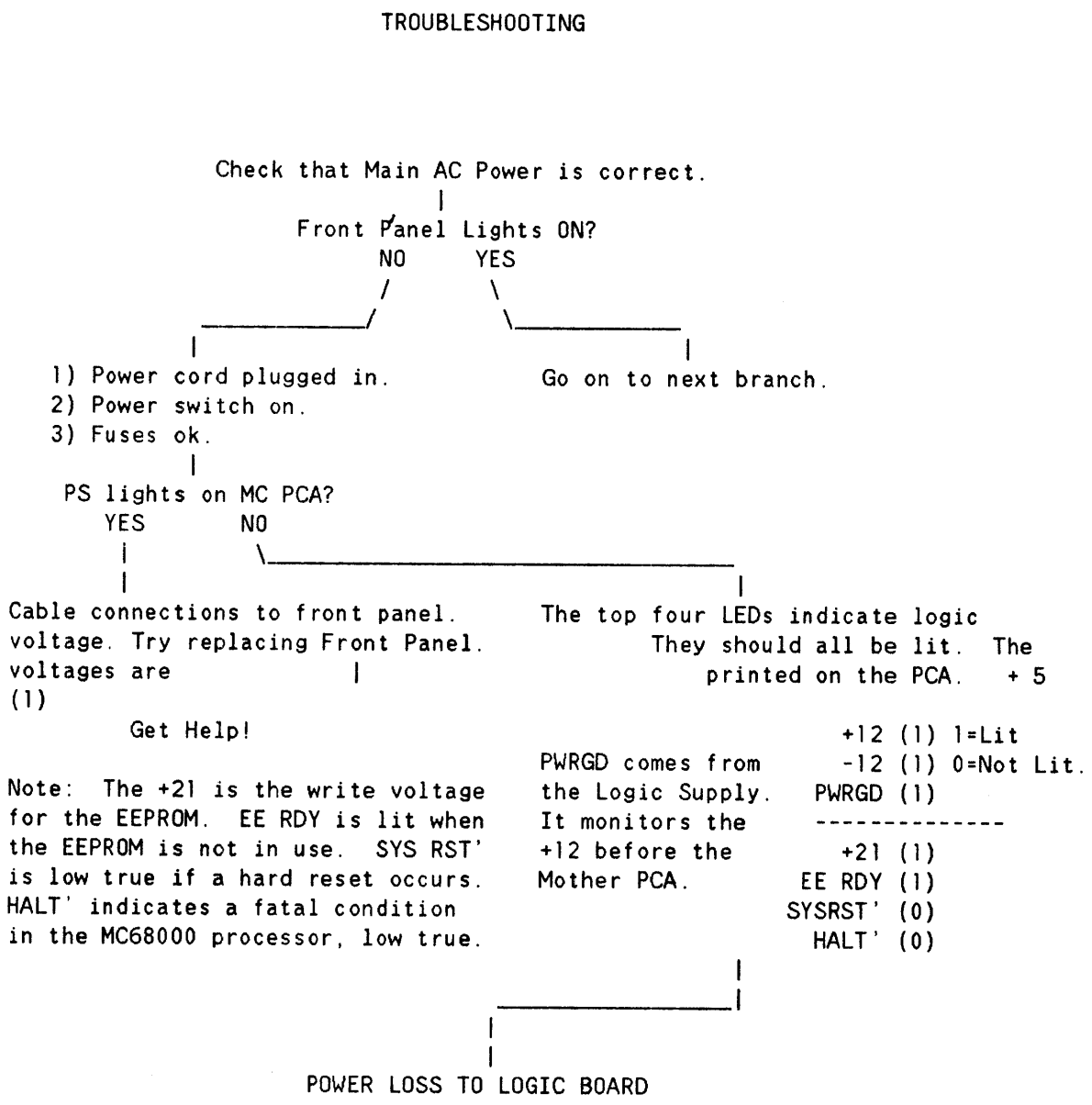
3. Ensure that the tape being used is of high quality and has not deteriorated.

4. If, after cleaning the tape path and using known good tape,the **A3** message still appears frequently or remains on, a hardware problem might exist.

NOTE

The selection and use of media, supplies and consumables is the customer's responsibility. Hewlett-Packard reserves the right to exclude from the warranty or service agreement any repairs for damage to HP products which HP reasonably determines or believes was caused by use of non-HP media or cleaning supplies. Hewlett-Packard will, upon request, repair such damage on a time and material basis.

1.3 FLOWCHARTS



The LEDs show the voltage outputs of the Mother Board to the Master Control. The top four LEDs are voltage indicators, the bottom four indicate CPU processing "status". If an LED is off, check the voltage at the test point on the edge of the PCA. IF no LEDs on the logic board, it doesn't necessarily mean that the MC PCA is bad.

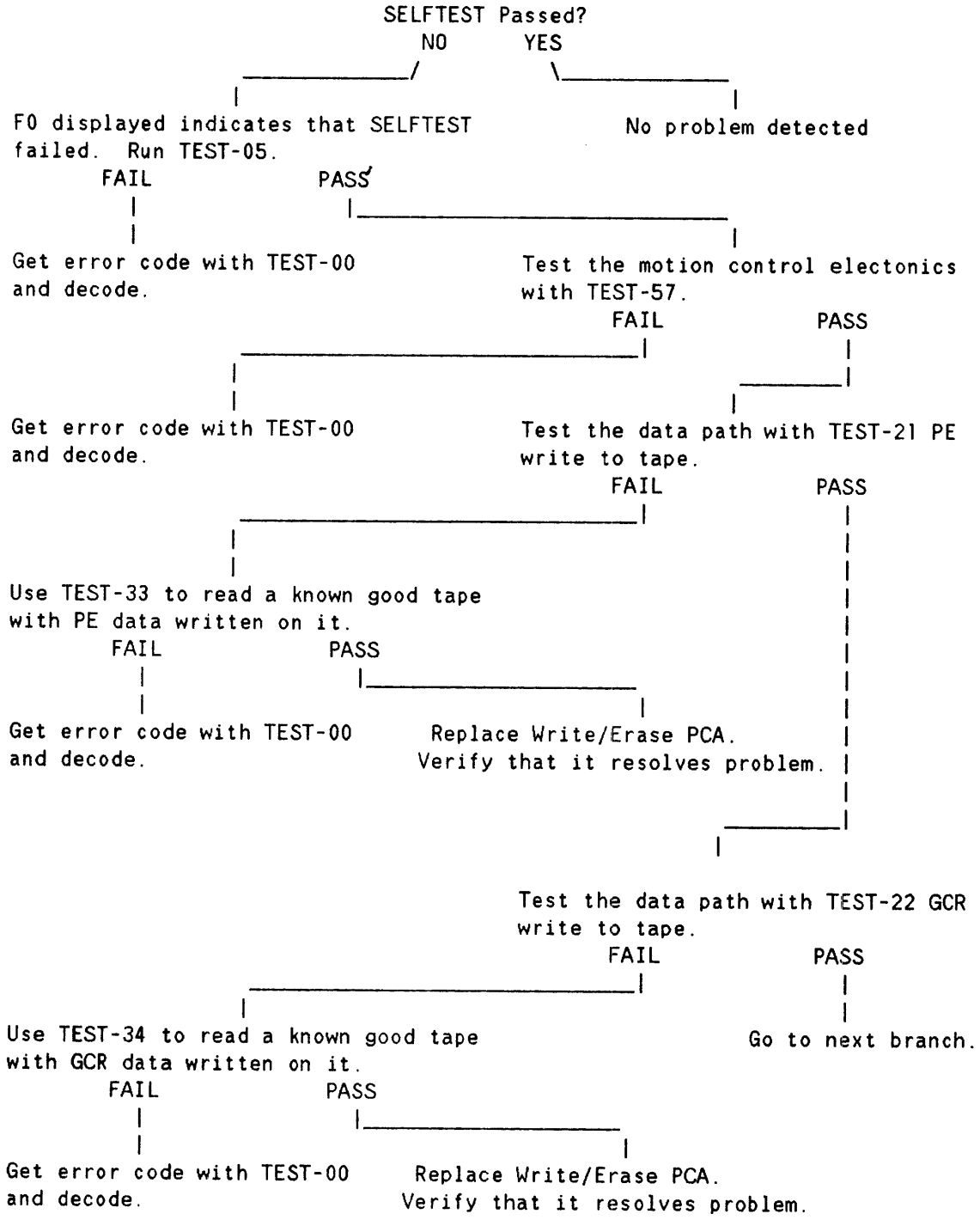
There is a possibility that power is ok to the card cage but it is being lost before it gets to the LEDs. Check the power at other places:

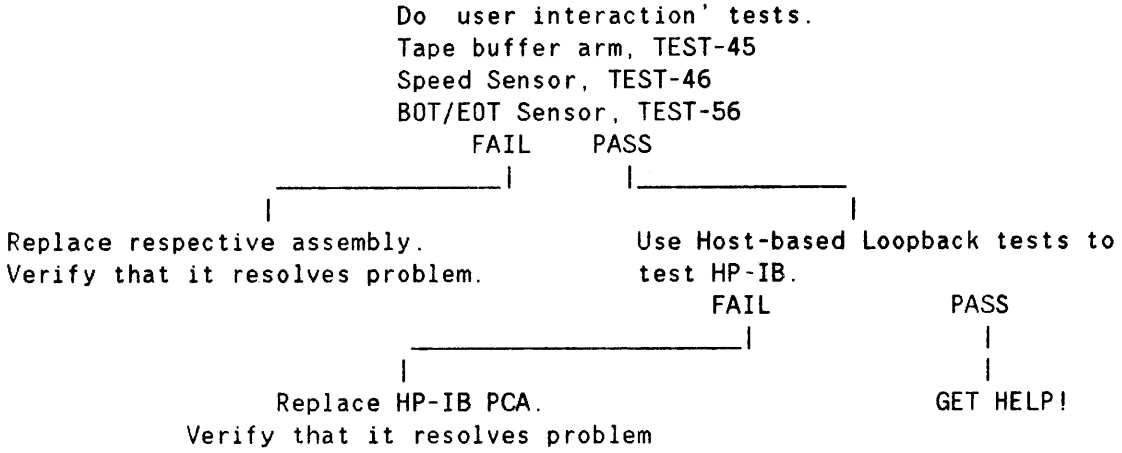
Take a look at the motor drive assembly.
Look at the +12 and -12 on the preamp board.
The logic supply
The motor drive assembly

If it doesn't show up one place, but shows up everyplace else, it's probably the Mother Board. If power doesn't appear, it is the power supply.

CAUTION

Ensure that power is turned off before changing any electronics board in the drive.


SELFTEST Passed?
NO
YES
F0 displayed indicates that SELFTEST failed. Run TEST-05.
No problem detected
FAIL
PASS
Get error code with TEST-00 and decode.
Test the motion control electonics with TEST-57.
FAIL
PASS
Get error code with TEST-00 and decode.
Test the data path with TEST-21 PE write to tape.
FAIL
PASS
Use TEST-33 to read a known good tape with PE data written on it.
FAIL
PASS
Get error code with TEST-00 and decode.
Replace Write/Erase PCA. Verify that it resolves problem.
Test the data path with TEST-22 GCR write to tape.
FAIL
PASS
Use TEST-34 to read a known good tape with GCR data written on it.
Go to next branch.
FAIL
PASS
Get error code with TEST-00 and decode.
Replace Write/Erase PCA. Verify that it resolves problem.


Do user interaction' tests.
Tape buffer arm, TEST-45
Speed Sensor, TEST-46
BOT/EOT Sensor, TEST-56
FAIL
PASS
Replace respective assembly.
Verify that it resolves problem.
Use Host-based Loopback tests to test HP-IB.
FAIL
PASS
Replace HP-IB PCA.
Verify that it resolves problem
GET HELP!

What is the symptom?

Do you have a focus for your suspicions?

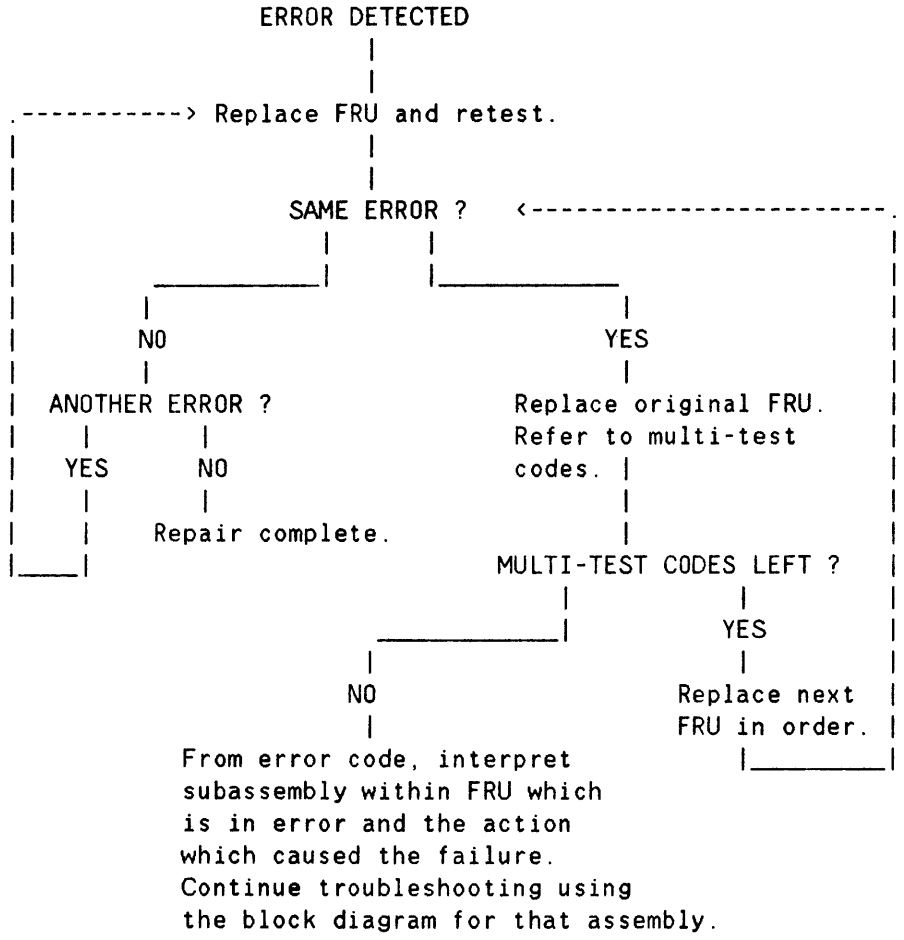
If not, then put the tape drive into a "maximum use" mode that puts the most stress on the electronics. Use the following utilities:

Utility TEST-25; sets the drive to NOT loop on test.
Utility TEST-26; sets the drive to loop on test.
Utility TEST-31; sets the drive to reposition tape on each test.
Utility TEST-32; sets the drive to "walk" the tape through the test.
Utility TEST-01; Displays the ERROR LOG.
Utility TEST-02; Clears the ERROR LOG.

Decoding Error Codes (TEST-00)

The error code is a FRU number relating to a specific assembly or PCA. A location diagram is on the plastic shield that covers the capacitors and Motor Driver Assembly (A2).

Follow the order of troubleshooting on the following page whenever possible.


ERROR DETECTED
Replace FRU and retest.
SAME ERROR ?
NO
YES
ANOTHER ERROR ?
YES
NO
Repair complete.
Replace original FRU.
Refer to multi-test
codes.
MULTI-TEST CODES LEFT ?
YES
NO
Replace next
FRU in order.
From error code, interpret
subassembly within FRU which
is in error and the action
which caused the failure.
Continue troubleshooting using
the block diagram for that assembly.

[2] TESTS AND ALIGNMENTS

2.1 MOTOR DRIVER BOARD

Motor Drive Board tests are available by selecting Tests 58 and 59. Test 58 gives audible and visual results for a quick check of the motor/servo subsystem and Test 59 is a more extensive set of tests that requires an oscilloscope.

Test 58 can reveal large problems in the motor drive/servo subsystems, especially in the output transistors.

Test 59 repeats a few of the tests done in the "audio/visual" Test 58 and adds more tests to extensively check the motor drive/servo circuits. Test 59 requires the use of an oscilloscope.

Both the series of subtests in Test 58 and the series of subtests in Test 59 require that the door be closed and that no tape is mounted.

Enter Test 58 by pressing the TEST/ADDESS button. You should see the word TEST backlighted (if not, press the TEST/ADDRESS button one more time). Increment the visual display to 58 by use of the TEST/ADDRESS button for the 'units' digit and the REWIND button for the 'tens' digit.

When the number 58 is in the display, press the ENTER button to start the test. The BUSY light will come on and 00 will appear in the display. showing that sequence 00 is running. Sequencing though the subtests is caused by pressing the ENTER button. The subtests are terminated by pressing the RESET button.

CAUTION

In case of problems such as motor runaway or violent oscillation, press the RESET button.

In general, if an output transistor fails in the open position in the following tests, the motor of that circuit will move in one direction and stop on command, but no motion can be stimulated in the reverse direction. If an output transistor fails in the shorted state, a motor will continuously go in one direction.

Subtest 00 -- VERIFY POWER AVAILABLE

This verifies that the power is being delivered to the Motor Drive Board. The relay on the Motor Drive Board is pulsed at about a 10-HZ rate with approximately a 10% duty cycle.

A clicking sound should be heard at the 10-HZ rate. Supplies of both +5 and +12 volts are required to pulse the relay. If either output transistor to either motor is shorted, the corresponding motor would creep.

Subtest 01 -- CHECK TRI-STATE OPERATION AND POSSIBLE SHORTS

The relay supplying power to the Motor Driver board is held closed. Approximately 5 volts is supplied to the output stage of the Motor Driver Board but is tristated and should not pass through the output stage and be output to the motors. The motors should remain motionless. The motors, in this condition, are servoing around 5 volts.

If the tristate is not working properly, the motors will turn at low speed (approximately 150 rpm) because of the low voltage being supplied.

If an output-stage transistor is shorted to the supply, the corresponding motor will rotate at approximately 700-800 rpm.

Motionless motors do not necessarily confirm that the tristate is working properly. Other factors could cause the same result. For example, the input lines could be open and the motors would be servoing around 0 volts. Continue the test sequence to Subtest 02.

Subtest 02 - OUTPUT STAGE PUSH-PULL - PART 1

This tests the condition where the upper reel is given a SH1 (0) signal and the lower reel is given a positive signal. The upper reel should remain stationary during this test and the lower reel should rotate slowly in a clockwise direction.

The positive side of the push-pull output stage transistor is checked here. If there is an open, the lower motor will rotate in the *counterclockwise* direction rather than a clockwise direction. The opposite side of the push-pull output is checked in the next subtest.

Subtest 03 -- OUTPUT STAGE PUSH-PULL - PART 2

As in Subtest 02, the upper motor is given a SH1 (0) signal to keep it stationary and the lower motor is given a motion signal - negative in this case. The lower motor should rotate slowly in a counterclockwise direction.

If there is an open in the negative side of the output stage transistor, the lower motor will rotate in the *clockwise* direction rather than in the counterclockwise direction.

Subtest 01 checked for shorts, Subtests 02, and 03 check for opens. If these tests are passed, a general good condition of the output transistor stages can be reasonably assumed.

Subtest 04, Subtest 05 -- OUTPUT STAGE CHECK FOR UPPER MOTOR

Subtests 04 and 05 check the upper motor in the same way as the lower motor was checked in Subtests 03 and 04. A positive signal is sent to the upper motor and then in Subtest 05, a negative signal is sent. Upper motor rotation should be the same as described for the lower motor in Subtests 02 and 03.

The same signals are also sent to the lower motor. Both motors should rotate in the same direction and at a similar speed.

Subtest 06 -- STRESS CHECK

This is a combination of all the previous tests (except Subtest 1). Both motors are made to oscillate back and forth at approximately 2 HZ to verify that substantially greater currents can be handled by the drive electronics.

The DC bias on the motors may cause some creep as the motors oscillate. A small amount of creep is normal however a large amount of creep indicates a problem.

Test 59 -- OSCILLOSCOPE TESTS

Test 59 is not always necessary when looking for a Field Replaceable Unit, but can become useful when visual tests seem to indicate everything is OK but there still is something wrong in the operation of the motor/servo loops. For example; oscillations, high frequency noise, etc., may average out and remain hidden, as far as a visual inpection goes, but be enough to make the read channel inoperative or even cause overheating on the output transistors.

Failures in the Motor, Motor Drive Board, Tension Board (or anything inside the servo loop can cause speed and tension variations that ultimately would appear as error rate. The motor(s) may have a cogging problem. These problems could exist even while the "audio/visual" results of Test 58 seemed good.

The significant results of these oscilloscope tests are the general waveforms, not exact voltages. The diagrams given in this manual are to show something very close to the correct output waveform. Compare actual results in terms of close approximation.

These subtests are constructed so that the motor drive amplifiers are checked under no-load conditions before the motors are included in the tests. The motors are then brought in as a low load and their current draw increased in steps to maximum. First, voltages are tested, then currents-- allowing an orderly progression from non-destructive to potentially destructive testing of the motor drive system.

Figure (8) 2-1 shows the location of the input and output test points on the Motor Drive Board.

Connect Channel A lead to AMP1 - output for Motor #1
Connect Channel B lead to AMP2 - output for Motor #2
Connect EXT TRIG to SHDN* - trigger for most tests

NOTE

> An asterisk (*) after any signal means the signal is active LOW. This symbol is used instead of a bar over the signal name because a superscript bar is not available in the laser fonts used for this manual.

Select 0.5 millisecond per division as an initial time base.

BEFORE BEGINNING TEST 59-

1. Mount a reel of tape on the supply hub. This should be a full, small-to-medium tape reel. Do not allow the tape to wind around any of the parts of the tape path, including capstans. The best way to prevent this is to mount a tape with a tape lock ring mounted. The purpose of the tape is to provide a damping weight for some tests that move the motors (Tests 0A through 0D). THE WRITE RING MUST BE REMOVED FROM THIS TAPE.

2. Run Test 45 to insure that the Tension Sensor is operating correctly. A safety shutdown caused by the positioning of the Tension Sensor Arm or by the failure of the Tension Sensor LED will prevent the series of tests in Test 59 from running.

Enter Test 59 by pressing the TEST/ADDRESS button. You should see the word TEST backlighted (if not, press the TEST/ADDRESS button one more time). Increment the visual display to 59 by use of the TEST/ADDRESS button for the 'units' digit and the REWIND button for the 'tens' digit.

When the number 59 is in the display, press the ENTER button to start the test. The BUSY light will come on and 00 will appear in the display. showing that sequence 00 is running. Sequencing though the subtests is caused by pressing the ENTER button. The subtests are terminated by pressing the RESET button.

CAUTION

In case of problems such as motor runaway or violent oscillation, press the RESET button.

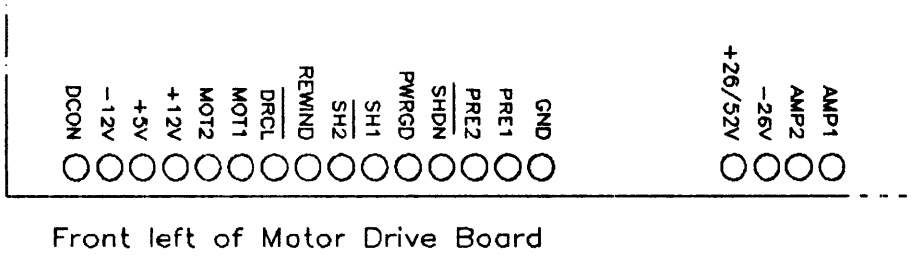


Figure (8) 2-1 Motor Drive Board Test Points

Subtest 00 CHECK FOR PRESENCE OF MOTOR DRIVER BOARD

Verifies the Motor Drive Board is awake and can listen to the Servo Board. The SHDN* signal is also tested.

A series of 0.01-second pulses are sent to the relay on the Motor Driver Board and these pulses should cause a 10-HZ clicking sound to be heard. The time between pulses is 0.09 seconds and this 10% duty cycle does not allow the relay to fully close, preventing possible electrical damage until the Motor Drive Board is checked further.

The output of the Motor Driver Amplifiers should be in their tri-state mode.

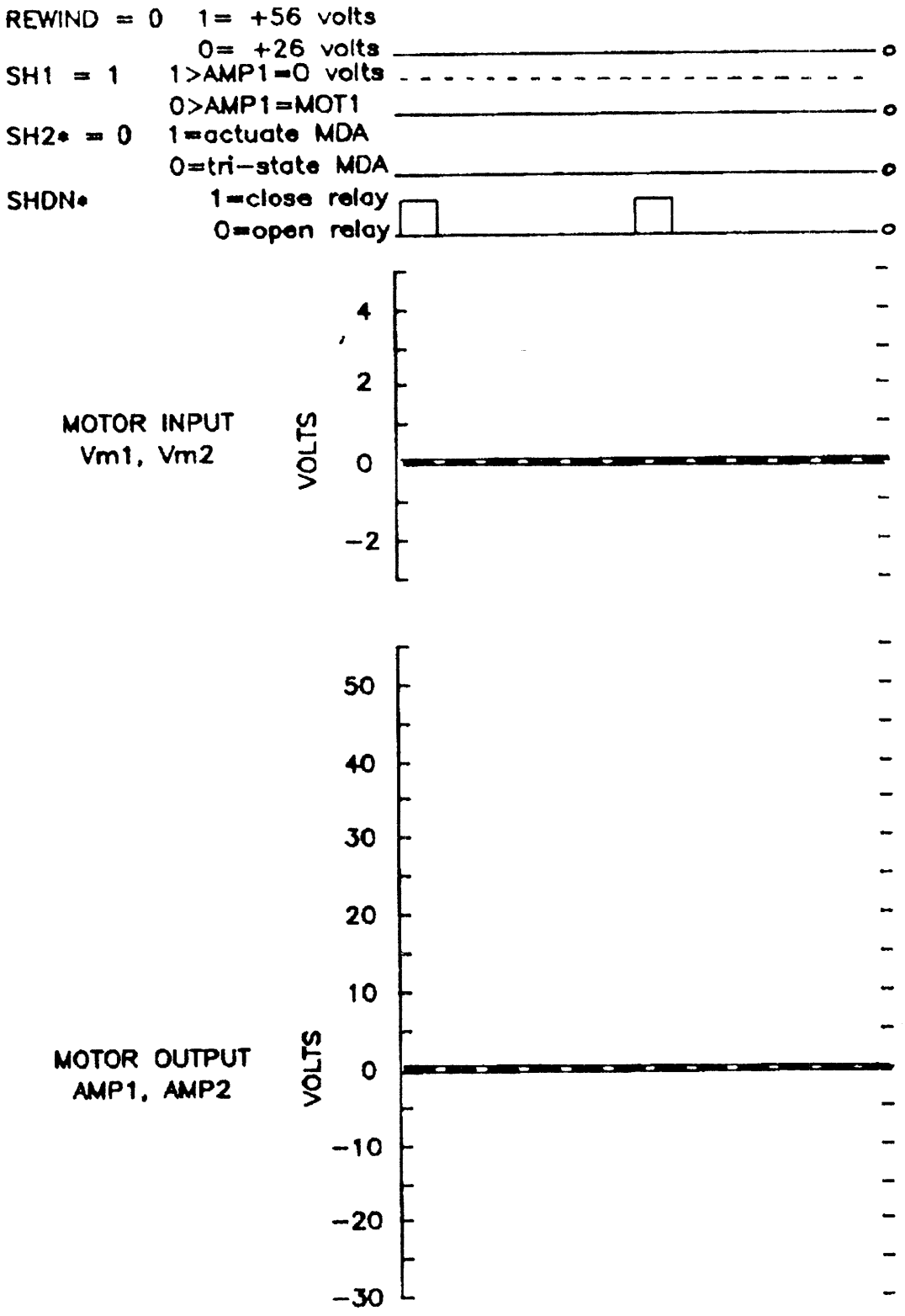


Figure (8) 2-2 Subtest 00 Input Conditions--Output Waveforms

Subtest 01 CHECK FOR SHORTED OUTPUT TRANSISTORS

Verifies that no TO-3 transistors are shorted to a power supply.

In this test, both inputs are placed at 0 volts. The AMP1 and AMP2 outputs should lie within about +/-200 millivolts of the 0-volt line. If a short exists, the appropriate output waveform will be pulled to either +26 or -26 volts.

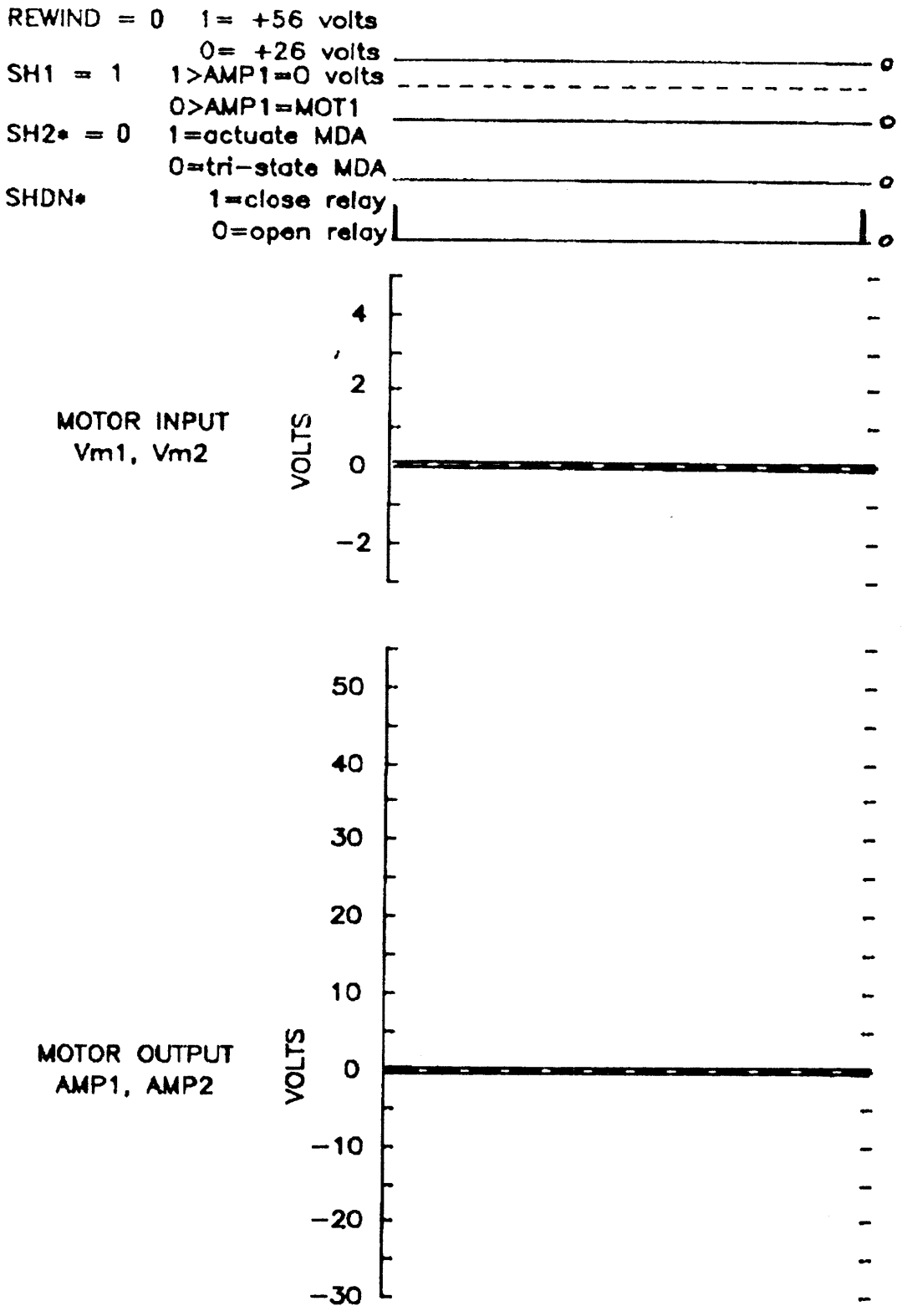


Figure (8) 2-3 Subtest 01 Input Conditions--Output Waveforms

Subtest 02 VERIFY CLOSED LOOP OPERATION

Verifies the closed-loop operation of the Motor Driver Amplifiers when servoing around 0 volts.

The difference between this test and Subtest 01 is that the Motor Drive Enable signal, SH2*, is changed to a HIGH, enabling the Motor Driver Amplifiers. (The motor drive amplifiers are active and not tri-stated as in Subtest 01). Approximately 30% of the circuitry on the Motor Driver Board is checked, including all transistors.

With an input of 0 volts, the correct output should be 0 volts.

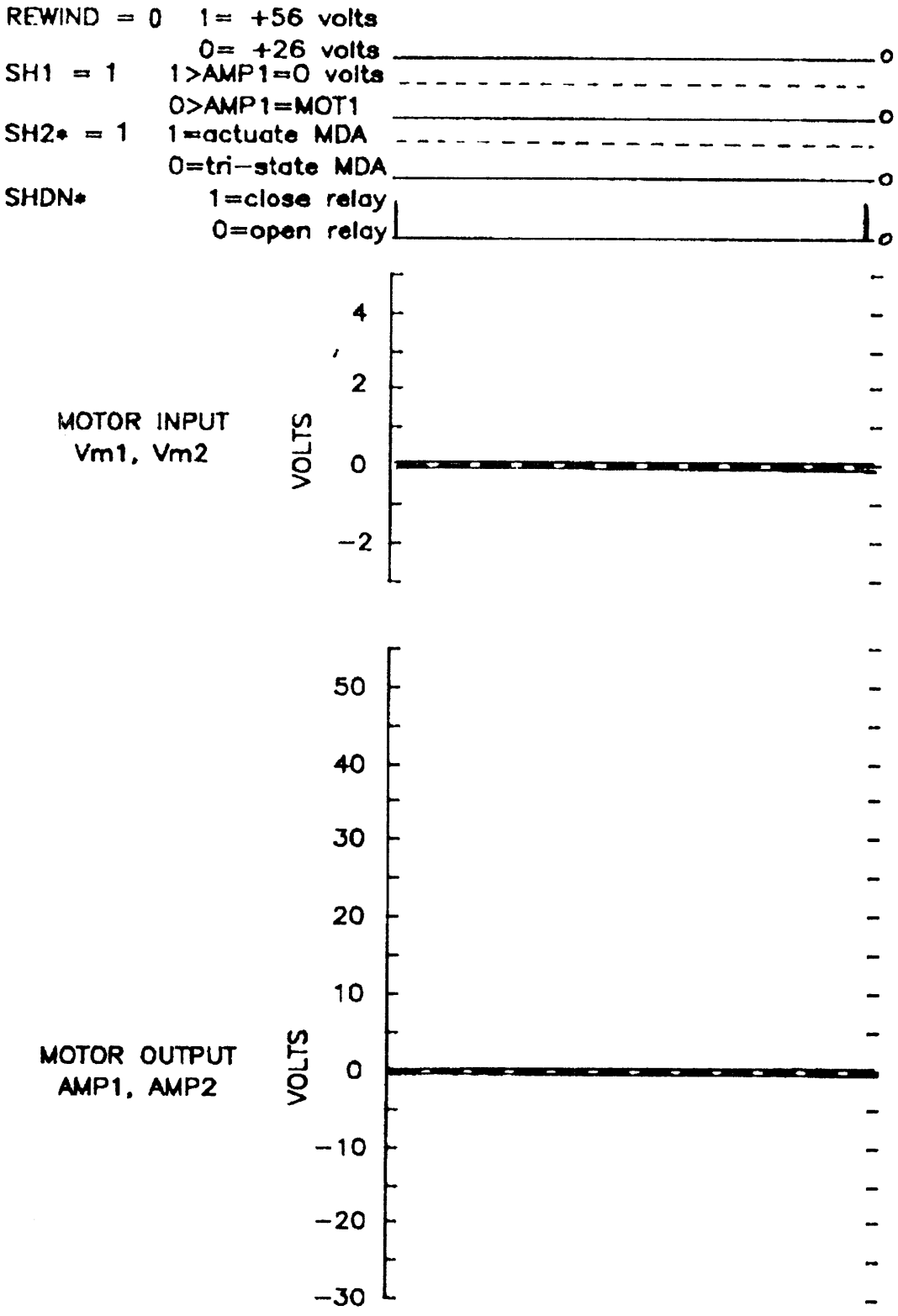


Figure (8) 2-4 Subtest 02 Input Conditions--Output Waveforms

Subtest 04 VERIFY SH2* TRISTATE OPERATION

Checks that the SH2* can tristate Motor Driver Amplifiers when Vm1=Vm2 and is not 0 volts.

This is a more rigorous test than Subtests 00,01,and 02 where the Motor Drive Amplifiers were tristated. The difference is that an oscillating input voltage of +/- 1.28 volts peak is applied at Vm1 and Vm2. AMP1 and AMP2 should still be kept tri-stated by SH1* and the output should lie close to the 0-volt line.

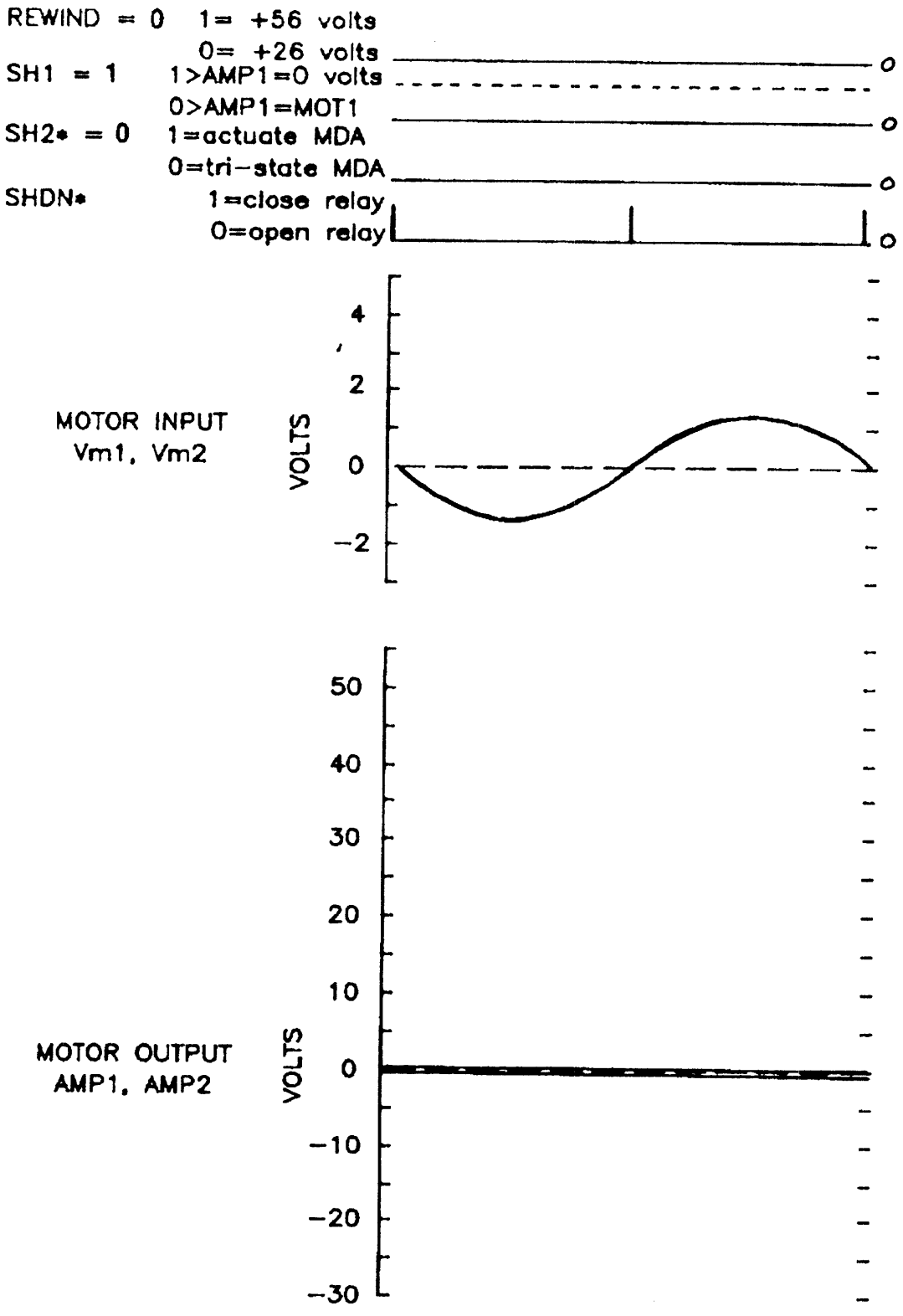


Figure (8) 2-5 Subtest 03 Input Conditions--Output waveforms

Subtest 04 CHECK OPERATION OF MOTOR DRIVER AMPLIFIER #1

Tests Motor Driver Amplifier #2 under no-load conditions and verifies that SH1 correctly forces Motor Driver Amplifier #1 to 0 volts output.

The purpose of SH1 is to force AMP1 to zero volts using a FET switch circuit on the Motor Driver Amplifier. This is done under no-load conditions.

Two waveforms should be seen. AMP1 should be held at 0 volts by SH1 and AMP2 should be a sine wave with a maximum swing of +/- 25 volts, peak.

A 0.2 millisecond deadband jog should be seen in the AMP2 waveform at zero crossing point. This comes from the switching between the two "halves" of the Motor Driver Amplifier.

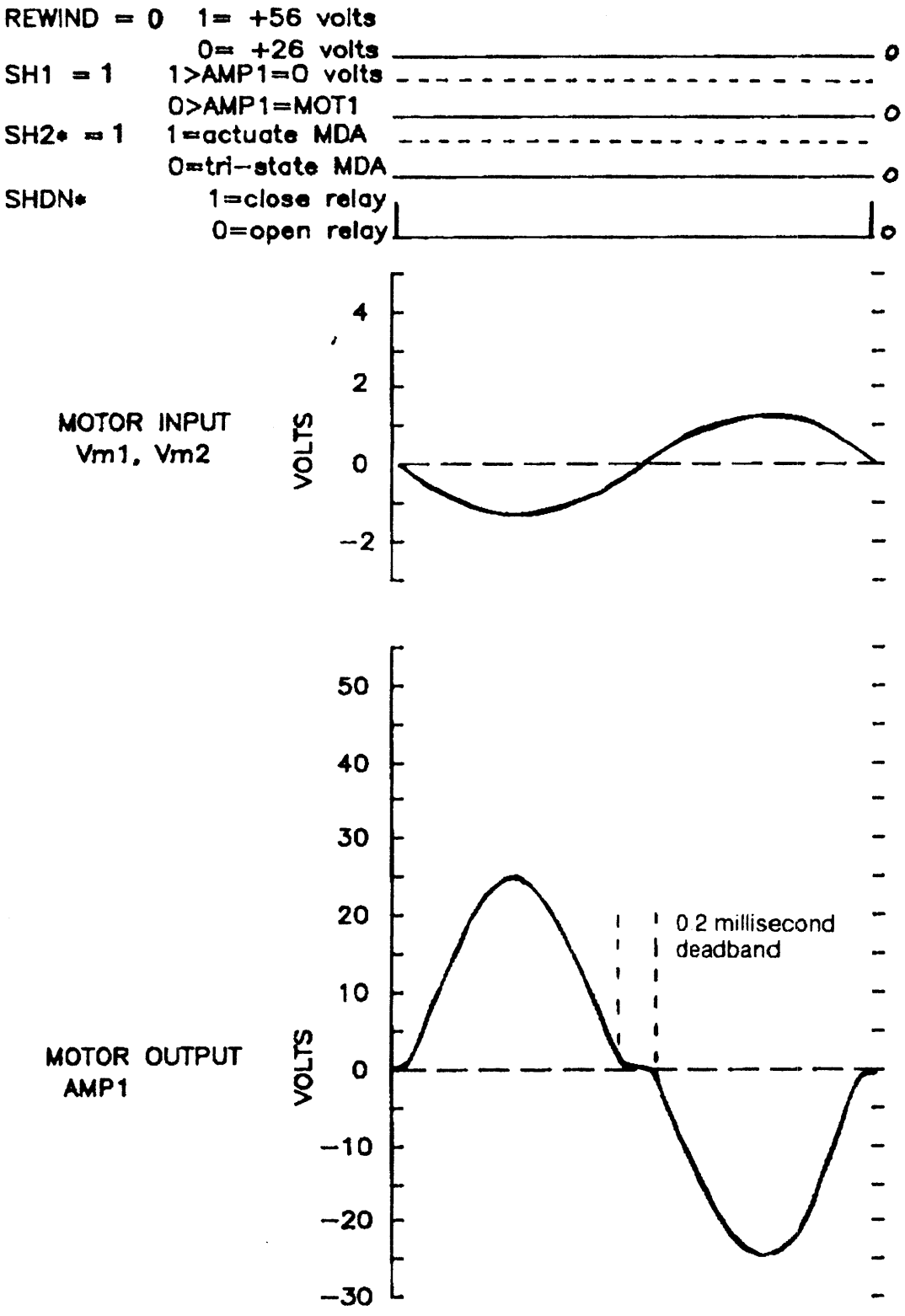


Figure (8) 2-6 Subtest 04 Input Conditions--Output Waveforms

Subtest 05 CHECK OPERATION OF BOTH MOTOR DRIVER AMPLIFIERS

Verifies that both Motor Driver Amplifiers can amplify under no-load conditions.

Compared to Subtest 04, this no-load test should show both AMP1 and AMP2 outputs as sine waveforms with voltage swings of +/- 25 volts peak.

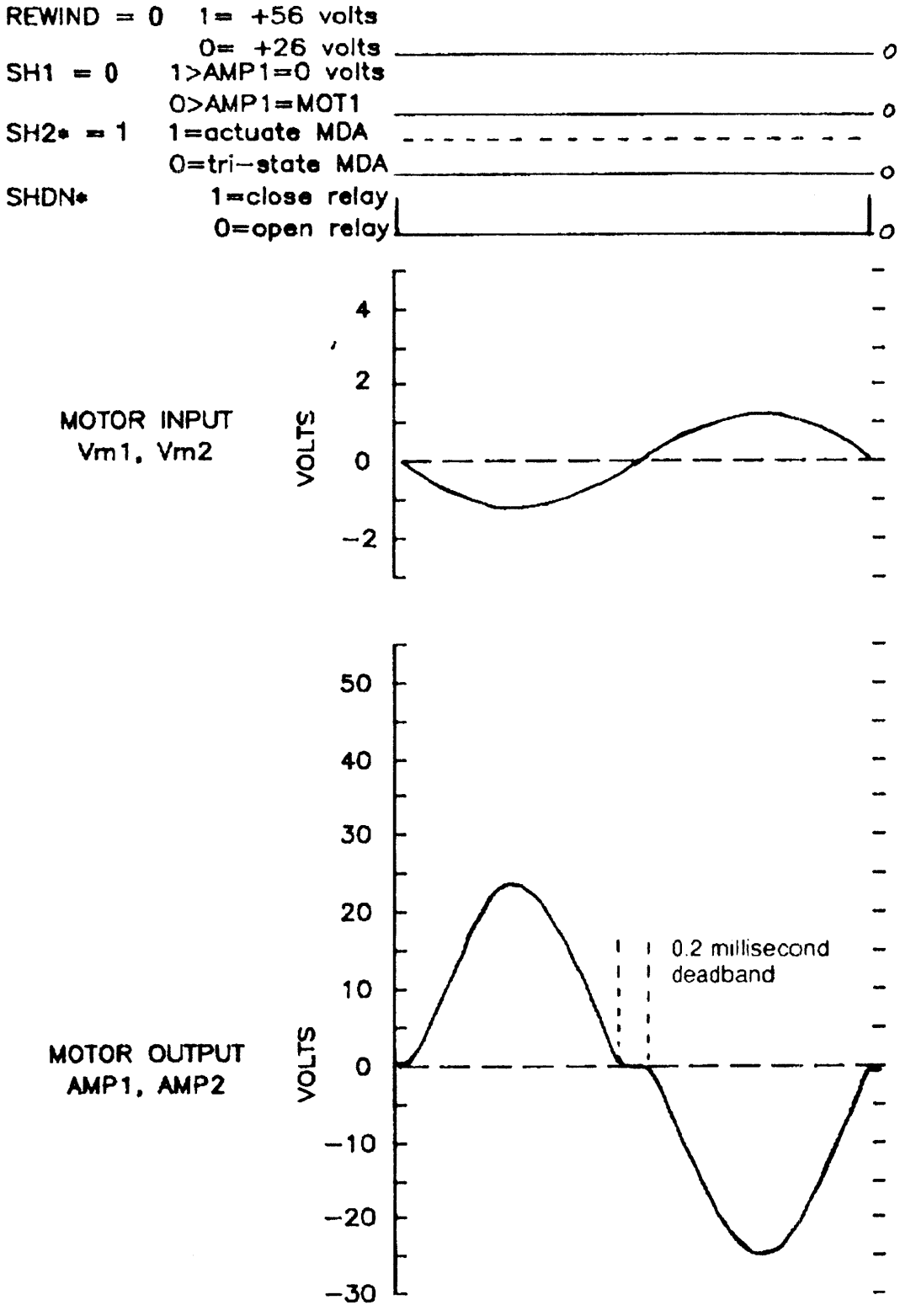


Figure (8) 2-7 Subtest 05 Input Conditions--Output Waveforms

Subtest 06 CHECK SATURATION OF MOTOR DRIVER AMPLIFIERS

Checks that both Motor Driver Amplifiers can saturate at their voltage supply limits. Also checks the rough accuracy of the preregulated voltage outputs.

The waveform for both AMP1 and AMP2 should clip at approximately +/- 26 volts.

The preregulator takes approximately 30% of the circuitry on the Motor Driver Board and its operation is checked out by this test. The positive 26-volt output of the preregulator is doubled to 52 volts when the Servo Board calls for rewind voltage to be supplied to the motors.

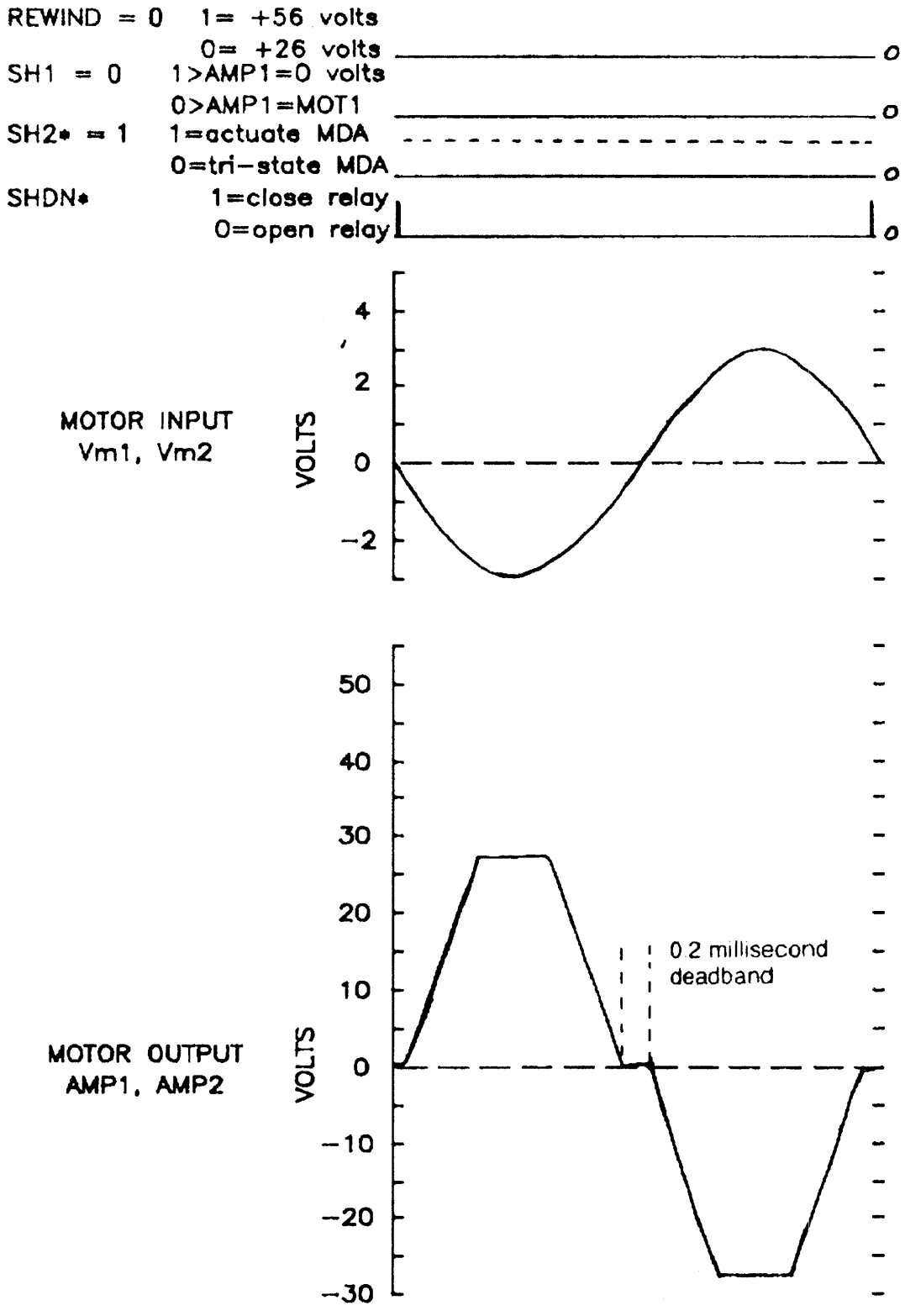


Figure (8) 2-8 Subtest 06 Input Conditions--Output Waveforms

Subtest 07 CHECK RESPONSE TO REWIND SIGNAL

Checks that the REWIND signal correctly doubles the positive preregulated voltage.

The positive half of the waveform for AMP1 and AMP2 should reach +52 volts. The negative half of the waveform should remain clipped at -26 volts.

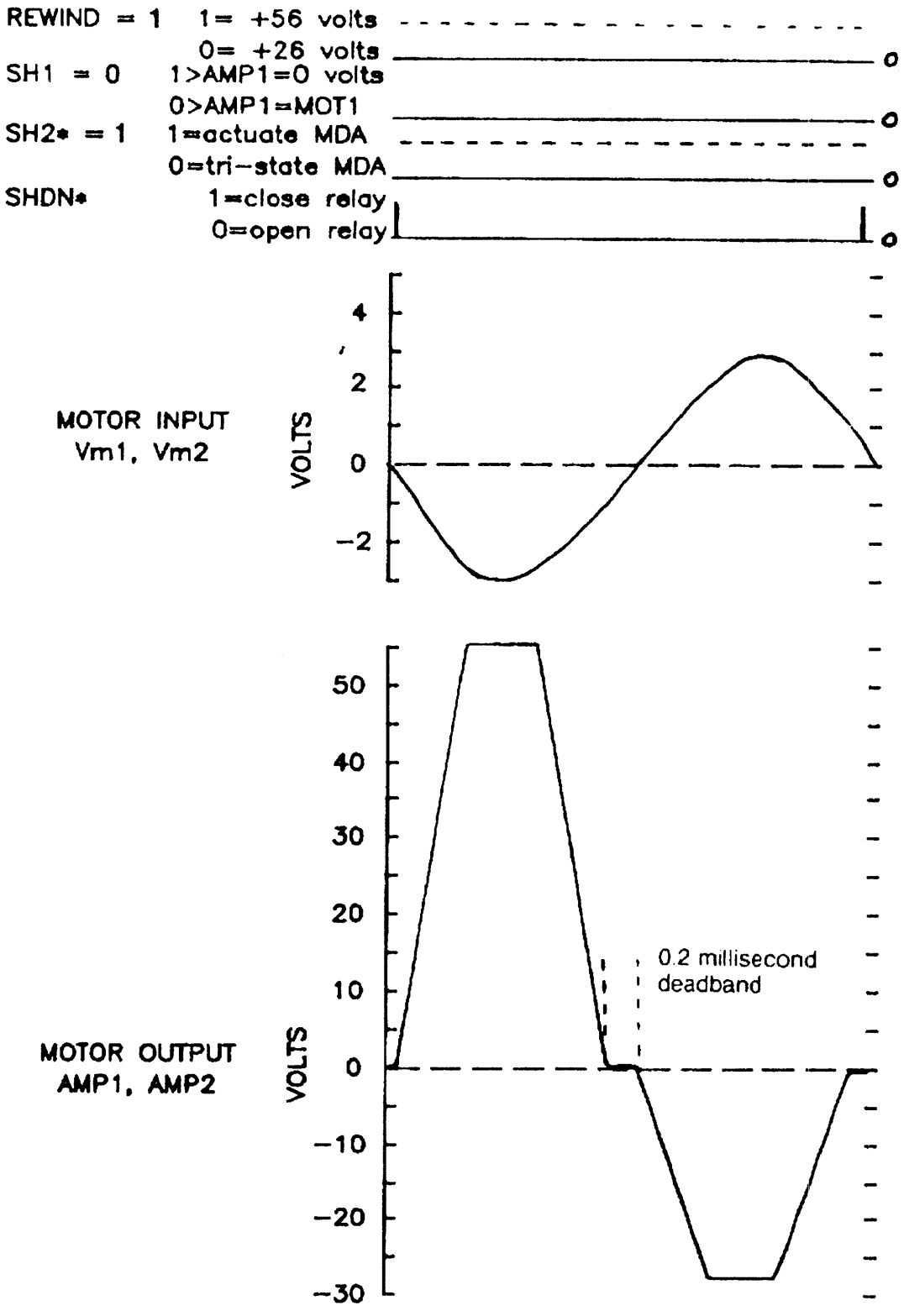


Figure (8) 2-9 Subtest 07 Input Conditions--Output Waveforms

Subtest 08 CHECK OPERATION OF PREREGULATOR BLEED CIRCUIT

Generally confirms that the preregulator bleed circuit is functional.

Change the oscilloscope to 2 milliseconds per division.

When a rewind is over and the preregulator is then called on to drop from +52 down to +26 volts, the bleed circuit pulls the charge off the capacitor as quick as possible so that read/write operations, which need only +26 volts, can be initiated. Bleedoff takes about 300 milliseconds.

This test oscillates the REWIND signal between 0 and 1 at 0.65-second intervals. The voltages from the preregulator should go from +26 to +52. The SHDN* signal is strobed 0.020 second before the change in voltage selection.

The significant information we're looking for on the oscilloscope is whether this bleedoff from +56 volts has occurred in the time alotted. Triggering is done twice every cycle in this test, so if the oscilloscope is set with its triggering mode in AUTO, the picture will be as shown in Figure (8) 2-10. You should see a continous band of traces with the high boundary at +56 volts and the lower boundary at +26 volts.

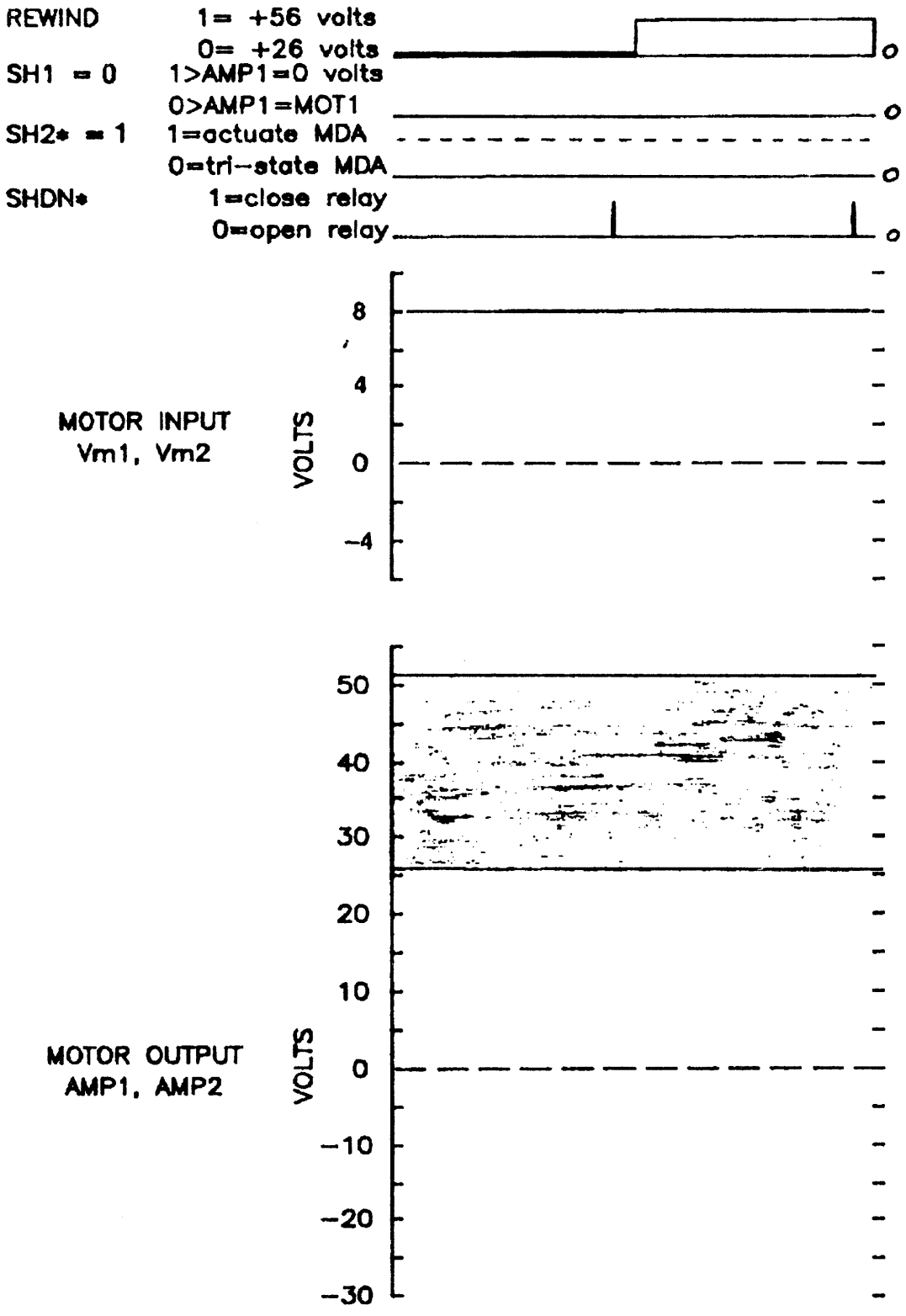


Figure (8) 2-10 Subtest 08 Input Conditions--Output Waveforms

Subtest 09 CHECK STEP RESPONSE OF MOTOR DRIVER AMPLIFIERS

Checks the step response of the Motor Driver Amplifiers and that their high and low frequency gain is correct.

A square wave of +/-0.714 volts is applied to Vm1 and Vm2. The waveforms of AMP1 and AMP2 should be as shown. Particularly note if the waveforms level out at plus and minus 5 volts in the area before the deadband gap.

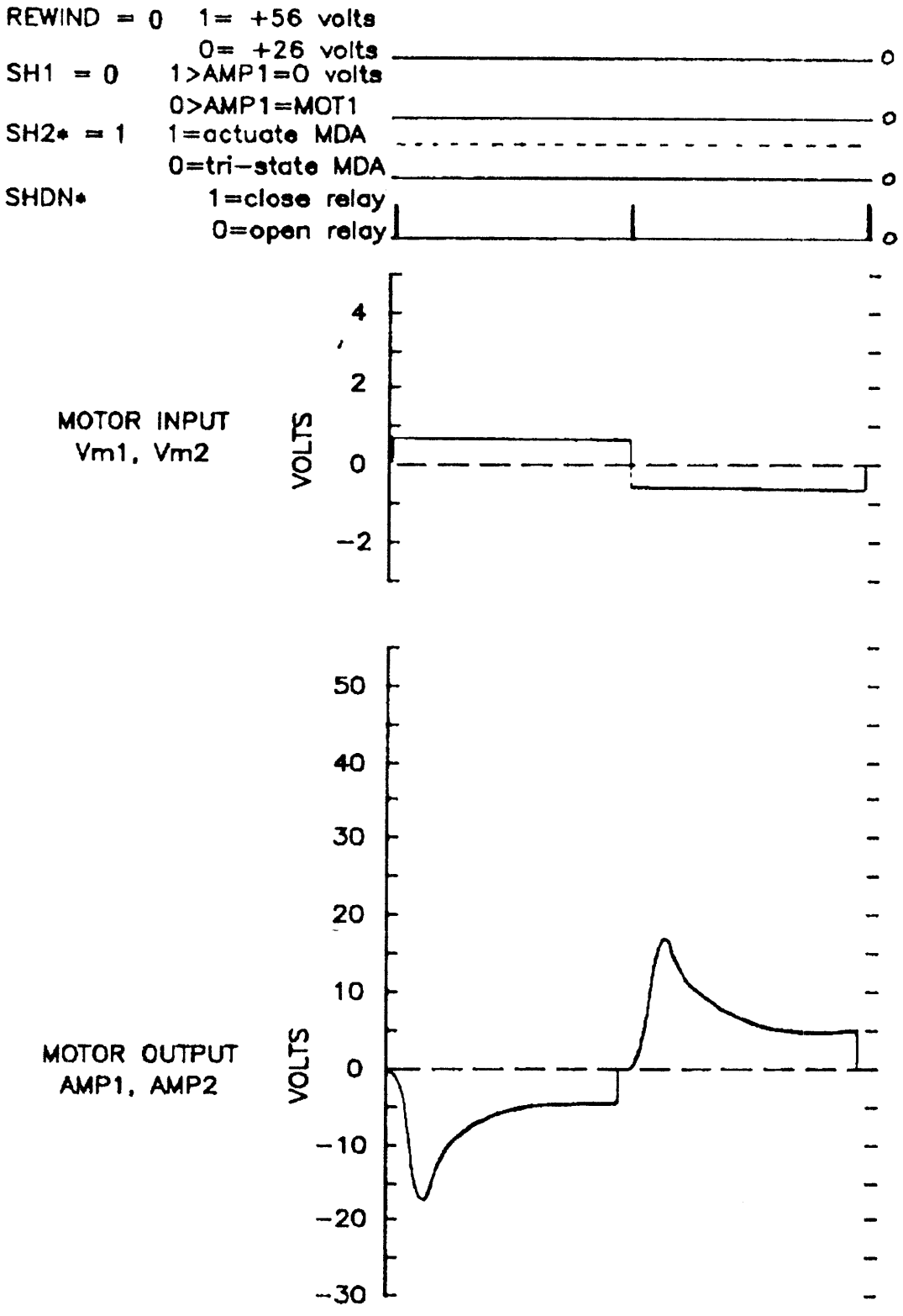


Figure (8) 2-11 Subtest 09 Input Conditions--Output Waveforms

Subtest 0A CHECK PULSE RESPONSE OF AMPLIFIERS (WITH LOAD)

Verifies the pulse response of the Motor Driver Amplifiers while a motor load is present.

This test is similar to Subtest 10 but with a load present. The inputs (Vm1 and Vm2) oscillate around +0.714 volts.

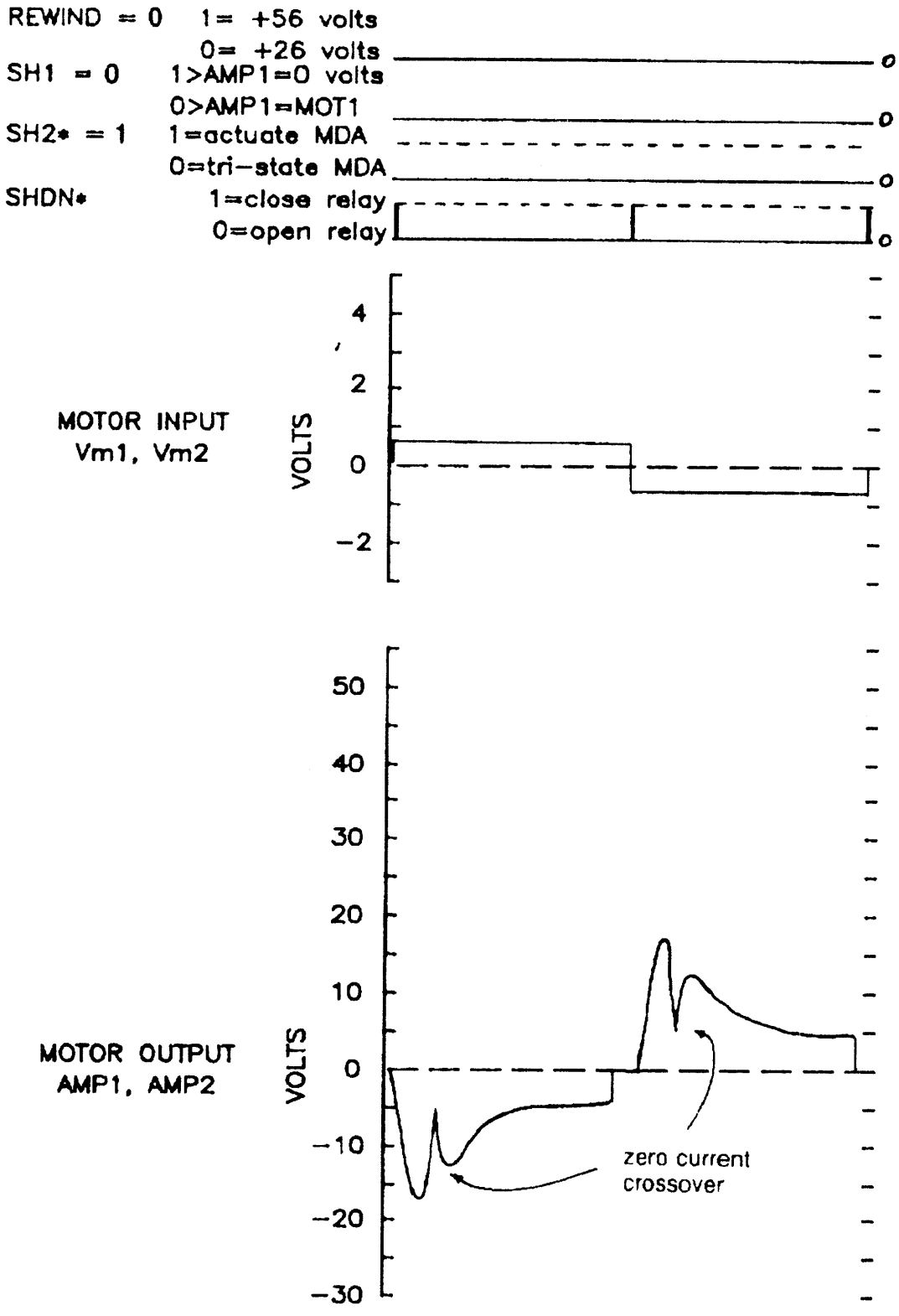


Figure (8) 2-12 Subtest 0A Input Conditions--Output Waveforms

Subtest 0B CHECK CURRENT HANDLING CAPABILITY (LOW)

Verifies the current handling capability of the Motor Driver Amplifiers with typical low-level motor load currents (~2 amps peak).

The current limiter circuit determines the maximum amount of current the Motor Driver Amplifier can output at any given time. Should this circuit fail, the Motor Driver would be unprotected and could destroy itself if given the wrong demands.

This test is the first of three tests (0B,0C,0D) that progressively ask for more current from the Motor Driver Amplifiers. Input at Vm1 and Vm2 is a sine wave of 20 HZ centered around 0 volts. Amplitude is 0.581 volts.

Output from AMP1 and AMP2 are 10-volt p-p sine waves. The dips from the waveform to the 0-volt level are characteristic of a push-pull (Class C) amplifier and are not significant to the output of this test.

The motors should be turning back and forth at 20 HZ. The motors will make a small sound.

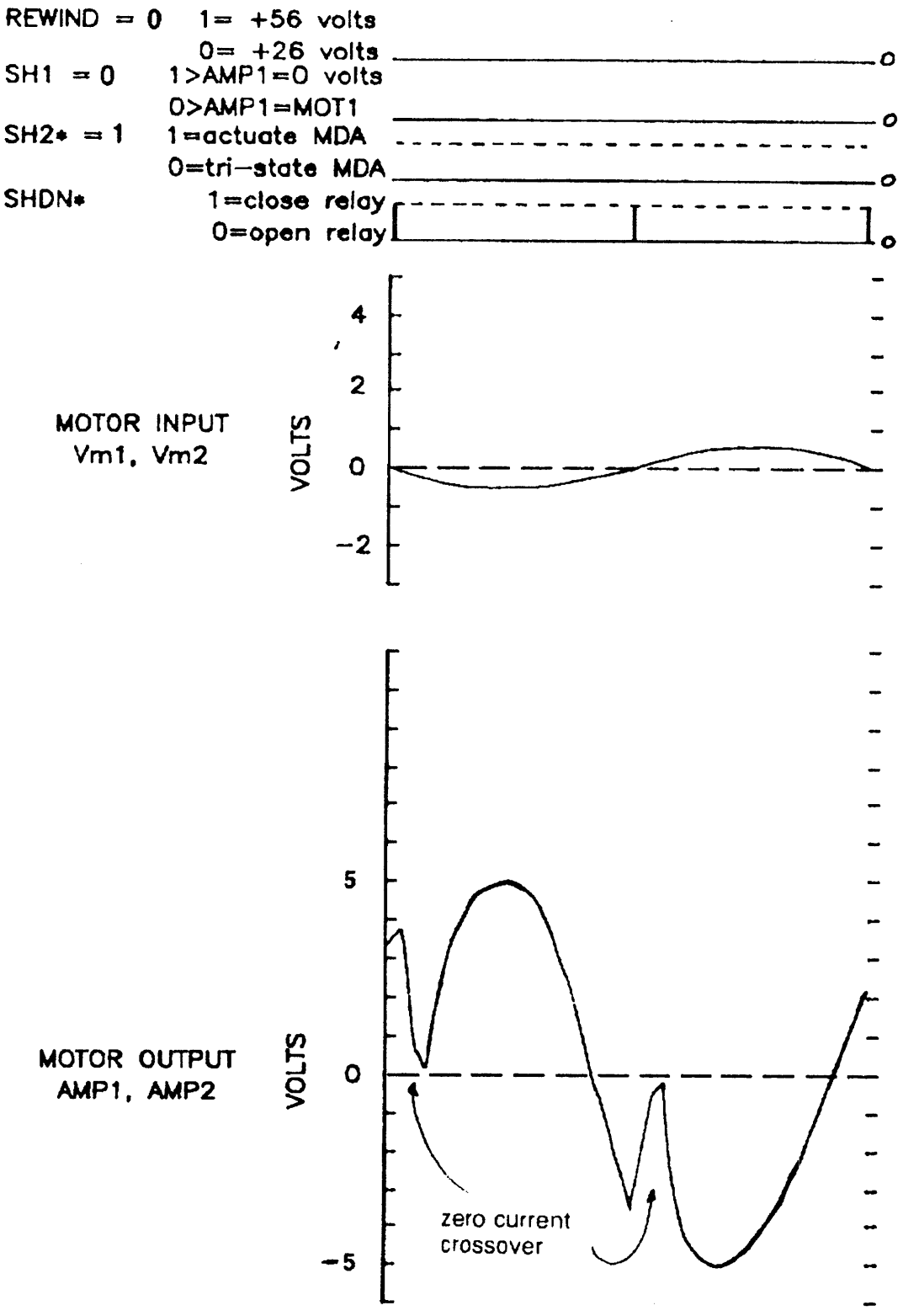


Figure (8) 2-13 Subtest 0B Input Conditions--Output Waveforms

Subtest 0C CHECK CURRENT HANDLING CAPABILITY (MEDIUM)

Verifies the current handling capability of the Motor Driver Amplifiers with moderate motor load currents (~6 amps peak).

Asks for more current than Subtest 0B. The Vm1 and Vm2 frequency remains at 20 HZ and the amplitude is increased to +/- 1.74 volts.

The outputs at AMP1 and AMP2 should go to +15 volts and -15 volts. The push pull spikes mentioned in Subtest 0B should still be visible.

The motors should oscillate at 20 HZ and the sound should increase over the level heard in Subtest 0B.

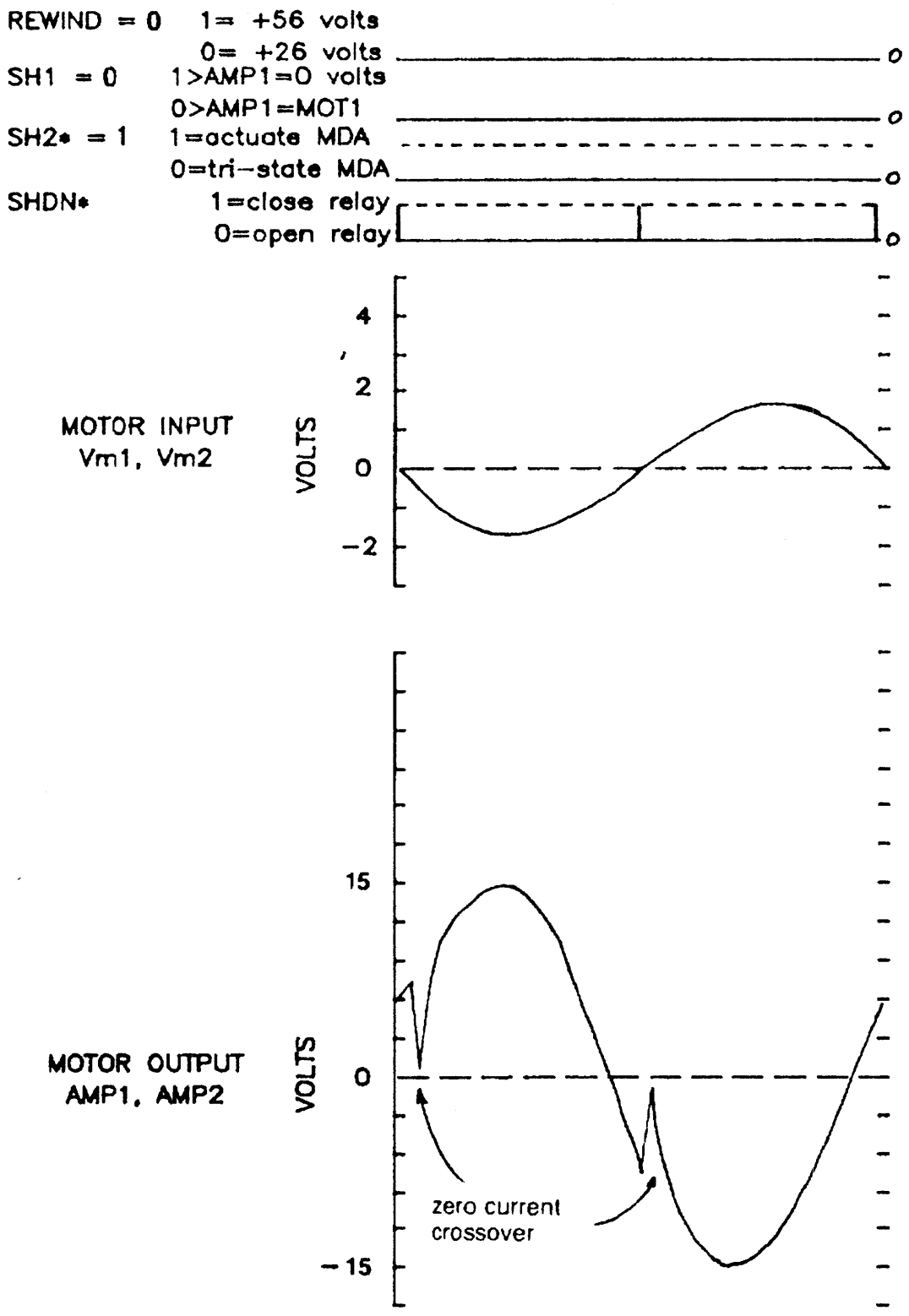


Figure (8) 2-14 Subtest 0C Input Conditions--Output Waveforms

Subtest 0D CHECK CURRENT HANDLING CAPABILITY (HIGH)

Verifies the current handling capability of the Motor Driver Amplifiers with excessive motor load currents (~10 amps).

This is the last test in the series to test the current handling capabilities of the Motor Driver Amplifiers under load conditions. This last test is the only test that actually tests the limit.

The output waveforms should be close to that shown in Figure (8) 2-15. A half-cycle approach should be made to about +/-27.5 volts and then the current limiting function should take effect. The voltage should drop to close to 18 volts as the current limiting function clamps the output to 10 Amperes. The positive and negative halves of the sine wave should be mirror images of each other.

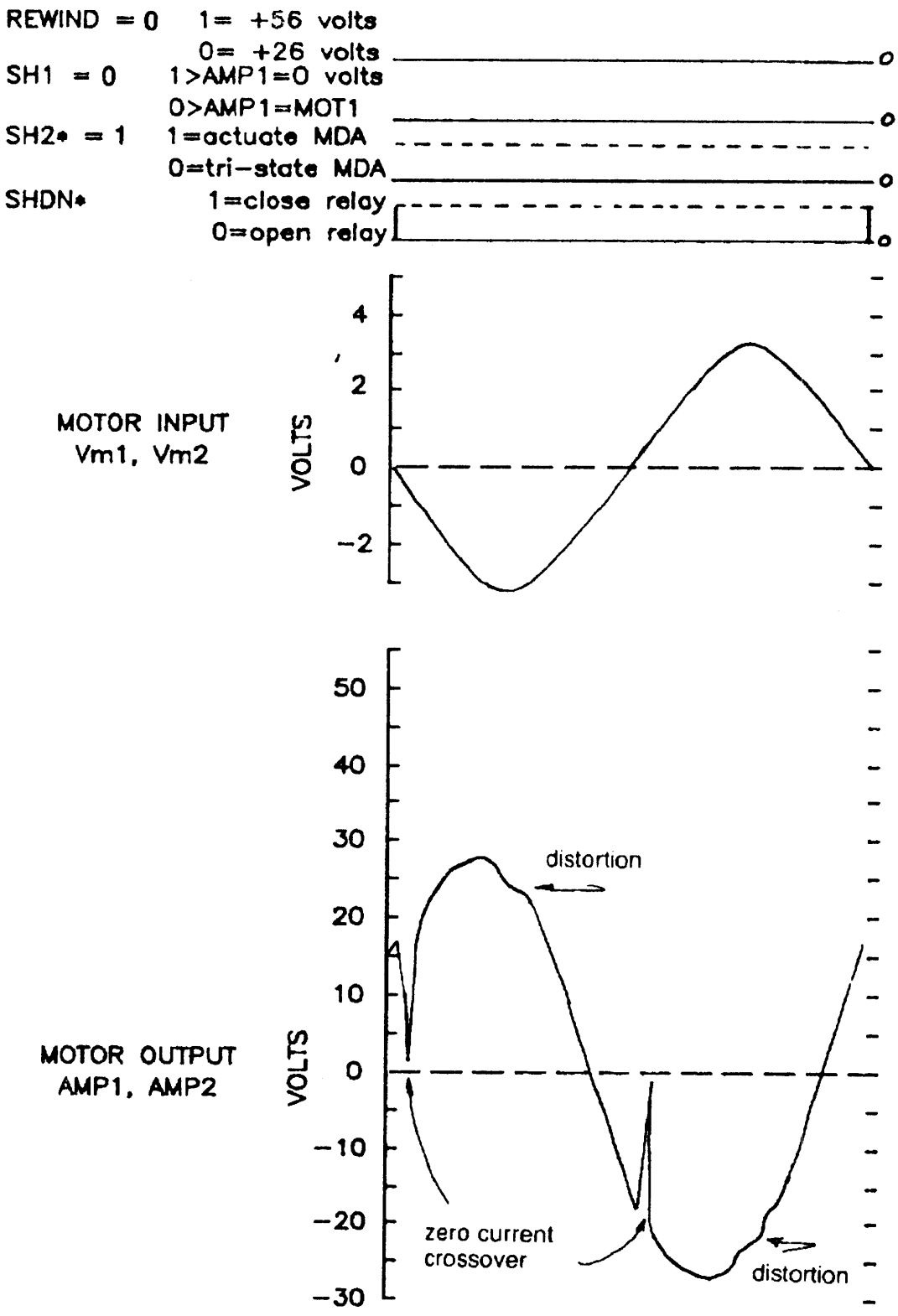


Figure (8) 2-15 Subtest 0D Input Conditions--Output Waveforms

2.2 SKEW

Use of skew tape is being evaluated. No specific procedures available at this time.

2.3 PREAMPLIFIER OUTPUT AMPLITUDE

Procedures for monitoring tape head preamplifier output are being evaluated at this time.

2.4 BOT/EOT SENSOR

The BOT and EOT sensors may be checked by executing Diagnostic Test 56.

Mount two strips of reflective tape marker on each side of a short piece of half-inch tape. The two strips should be offset along the length of the test tape so that both sensors will not be seeing a tape marker at the same time.)

When the tape is placed in front of the sensors (in the tape path slot), an OB (over BOT) will show in the display when the BOT sensor detects a reflective strip on the BOT-side of the tape. An OE (over EOT) will show in the display when the EOT sensor detects a reflective strip on the EOT-side of the tape.

If reflective strips are placed on both sides of the tape (not offest), the display will show BE (for both BOT and EOT).

The EOT sensor is the one mounted closest to the casting.

2.5 AUTO-GAIN

DESCRIPTION OF THE PROCEDURE

During the Auto-Gain, three readings are taken for each of the nine tracks for both PE and GCR. From these readings 18 Auto-Gain values are computed and stored in EEPROM; nine used in PE reads and nine for GCR reads.

HP-certified tape is used to supply a "medium amplitude" tape. The tape is first written with a known pattern for PE; the tape is read and Auto-Gain values are computed for PE. The tape is then overwritten with the GCR test format; the tape is read and Auto-Gain values are computed for GCR.

To compute proper gain values, the The read electronics are initially loaded with a "0" gain value. When the tape is read, a comparison is made between the output from "0" gain and the desired output (midpoint between upper and lower allowable boundaries). A check is made to determine if the gain loaded into the read electronics is too high or too low (the first check with "0" is obviously too low). Depending on whether the gain is too high or too low, a new value is loaded into the read electronics which is halfway between the present gain value and the gain value farthest away that has not been used (in either an increasing or decreasing direction). In the first test, a value halfway between the present ("0") setting and the maximum

setting in the desired direction (towards higher gain - "255") is "127". This resetting and comparing is done until a gain value is established that is closest to the "norm".

The above sequence of setting an initial gain value, reading the tape, comparing output to the "norm", resetting the gain value, reading, etc. is done three times for each of the nine tracks. The 27 values are then divided by nine to average them for all the tracks. Values for both PE and GCR are found during one execution of the Auto-Gain procedure.

Execution of Auto-Gain

NOTE

AN HP-certified tape provides the proper amplitude and quality for use in this procedure.

1. Mount and load the tape. Refer to Section III for a review of mounting and loading tape.

2. Select Test #24 (Auto-Gain) using the ENTER and TEST/ADDRESS Buttons. Refer to the beginning of this Section if review is needed in selecting diagnostic tests.

3. After Test #24 is selected, there is a 5-second period in which a specific sequence buttons must be pressed to initiate the Auto-Gains procedure. Press the following buttons in order:

    1. REWIND Button
    2. RESET Button
    3. TEST/ADDRESS Button.

The tape will start moving at this time to start the PE sequence. A pattern of all 1's is written on the tape. The tape then rewinds and reads the pattern, computing three gain values per track. During the read, the PE Density light is lit.

When the tape read and computation operation is over, the tape is rewound. The Status light should come on amber and the average gain value computed is shown in the hexadecimal display. If the Status light comes on red, that means that all three gain values computed for at least one track are outside of the allowable boundaries. THE VALUE, HOWEVER, WILL BE LOADED INTO EEPROM, REGARDLESS OF WHETHER IT IS WITHIN BOUNDS OR NOT. An two-byte error code will cycle in the hexadecimal display.

Even if there has been a track found out-of-limits, the procedure automatically continues.

The PE Density light goes out. The tape is then rewritten with the GCR test pattern, rewound, read (with GCR Density light lit), and the same indications of results as previously explained are shown in the Status light and the hexadecimal display.

A log is kept of an errors in this procedure. The log shows which tracks were out of bounds and whether these tracks were too high or too low. To view the log, run Test #01.

The interpretation of the error code is covered in Subsection 1.0.0 and repeated here.

8xx0H Read Electronics board FRU.

8abcH Auto-gain error code. Parameter 0 indicates which tracks are bad by putting a '1' in the track fields. Parameter 1 indicates low or high amplitude by putting a '0' or '1' in the indicated tracks for low or high, respectively. Note: The high order bit is 15, while the low order bit is 0.

a Bit 11 contains the parameter. Bits 10-9 contain the density. (PE=2,GCR=3) Bit 8 contains track 9 data.

b Bits 7-4 contain tracks 8-5.

c Bits 3-0 contain tracks 4-1.

IX REPLACEABLE PARTS

[1] ORIGINAL TO REPLACEMENT PARTS
- 1.1 SPARES
- 1.2 SPECIAL PARTS
- 1.3 ILLUSTRATED PARTS BREAKDOWN

Replaceable parts are noted on Removal and Replacement pictures in Section VI, REMOVAL AND REPLACEMENT.

NONE DESIGNATED AT THIS TIME

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PRODUCT HISTORY

SECTION XI

NOT APPLICABLE AT PRESENT TIME

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DIAGRAMS

THIS SECTION TO HOLD GRAPHICS NOT YET IN ELECTRONIC FORM

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