HP 250

PRELIMINARY

ON-SITE SERVICE MANUAL

Hewlett-Packard Company
Fort Collins Division
3400 East Harmony Road
Fort Collins, Colorado 80525

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PRINTING HISTORY

New editions of this manual will incorporate all material updated since the previous edition. Update packages may be issued between editions and contain replacement and additional pages to be merged into the manual by the user. Each update page will be indicated by a revision date at the bottom of the page, and a black bar in the page margin adjacent to the change on the page. Note that pages which are rearranged due to changes on a previous page are not considered revised.

The manual printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates which are incorporated at reprint do not cause the date to change.) The manual part number changes when extensive technical changes are incorporated.

Preliminary February 1979 p/n 45251-90030

NOTICE

MANUAL SCOPE

The On-Site Service Manual has been designed to aid the HP Customer Engineer in installing, troubleshooting and repairing the HP 250 System at the customer's location. Because normal repair at the customer's sight is circuit board replacement, detailed theory of operation is not included in this manual.

The Preliminary On-Site Service Manual replaces the Customer Engineering Training Manual. Many of the procedures contained in the training manual have changed extensively, and are now obsolete. If any conflict exists between the procedures contained in this manual and any other manual, the procedures herein will take precedence.

If you have any suggestions or find any errors in this material, please bring them to the attention of:

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System Turn-On

Even though the turn-on procedures for the HP 250 are very simple, a few checks should be made prior to turning the key-switch for the first time.

Printer Checks

1. Is the printer plugged in?

2. Is the Peripheral Interface (HP-IB) cable connected?

3. Is the desired select code set? (0 or 1)

4. Is there paper in the printer?

5. Is the printer turned on?

6. Additional checks for the HP 2631:
   -Press the RESET button.
   -Press the ON-LINE button: If the HP 2631 is not on-line when an output to the printer is attempted, the system will hang-up in an output mode waiting for the printer to come on-line.
   -Is the printer grounded to the printer stand?
   -Is the paper basket grounded?
   -Is tinsel installed on the paper path?

HP 250 Checks

1. Is the system plugged in and the keyswitch set to off?

2. Are all the boards in place and connections secure?

3. Check the Memory Board Switch settings.

NOTE

The following two steps represent the minimum requirements for a standard HP 250 System. For test purposes, two 64k byte Memory Boards can be used to load the Operating System and provide 16k bytes of user memory. One board must be designated Block 1, upper and lower. The other board must be designated Block 2, upper and Block 16, upper.

-Two 64k Memory Boards must be installed and be designated as Blocks 1 and 2, both upper and lower. This is the minimum Operating System memory.
-At least one 32K Memory Board must be installed and designated as an upper block from 3 thru 16. This is the minimum user memory.

4. Check the Processor Thumbwheel Switch settings. For normal operation, the switch should be in a position from 0 thru 3. See Tests and Procedures for switch position definitions.

Turn-on Procedure

1. Install the user's Operating System disc.
   -Slide the disc into the top drive.
   -Close the disc drive door.

2. Turn the keyswitch to the ON position.
   -The ROM stored hardware self-test is automatically performed.
   -If the self-test passes, a ROM stored loader routine loads the Operating System and DROMs from the Operating System disc.
   -A flashing cursor on the display indicates that the Operating System is loaded and available for use.

3. If necessary, the Operating System can be modified to suit the needs of the user and requirements of the system hardware. The CONFIG program is used for this purpose.

4. Finally, a total test of the system to verify operation must be performed. The TEST program is used for this purpose.

The remainder of this section deals with previous subjects by providing greater detail and step-by-step procedures.

The self-test and loader routines are initiated automatically when the keyswitch is turned on. The system user has no other means to initiate these routines. The Customer Engineer can repeat the self-test and loader routines without powering down and back up by pressing the POP Switch located on the Processor Board. See the Hardware section of this manual.

Self Test

The self-test begins each time the keyswitch is turned on or the POP Switch is pressed. As the self-test is being conducted, the following results are displayed. Also shown is the hardware tested by each test. If a failure occurs, refer to the Tests and Procedures section of this manual. Any test that fails during the self-test halts the routine, prevents system loading and displays FAIL opposite the corresponding test.

```
SELF-TEST  A
 1 BPC            PASS      (Processor Board)
 2 BLKSW          PASS      (Block Switch Board)
 3 RWFIND         PASS      (Processor and Block Switch)
 4 IOC            PASS      (Processor Board)
 5 EMC            PASS      (Processor Board)
 6 BLKSW2         PASS      (Block Switch Board)
 7 PROC BD        PASS      (Processor Board)
 8 MEMTABLE       PASS      (Memory Board)
 9 HPIB                     (Peripheral Interface Board)
     I O          PASS
     INT          PASS
     DMA          PASS
     IO INIT      PASS
10 FLOPPY         PASS      (Disc Controller)
```

Loader

After all hardware successfully passes its self-test, the ROM loader routine begins loading the Operating System and any DROMs configured to load.

Once the Operating System is loaded, it can be reconfigured to load the desired DROMs by running the CONFIG program, editing the DROM list, and reloading the system so that the change will become effective. The following list briefly describes the DROMs available. More detail concerning the capabilites provided by each DROM may be found in the System Software and BASIC Programming manuals.

-DROM-	-Description-
EUROPE	Determines the sorting order for alpha characters. The sequence is determined by which keyboard is loaded at system turn-on.
PACK	Provides a convenient means of transferring string and numeric data to and from a string variable.
IMAGE	Provides a data base management system for the HP 250. IMAGE/250 is modeled after IMAGE/3000.
SORT	Adds a collection of BASIC statements and functions to facilitate retrieving information from an IMAGE/250 data base.
REPORT	REPORT WRITER/250 is a collection of statements and functions which aid the programmer in producing reports.
TIO	Combining this DROM with the HP 45120A provides a means to connect up to five RS-232 asynchronous devices to the HP 250.
RIO	Combining this DROM with the HP 45120A provides a means to connect up to five remote consoles to the HP 250.
TRACE	This DROM is a debug tool used to trace the logic flow and variable assignments within a program.
TRIG	Adds trigometric statements and functions to the HP 250 BASIC language.
FORMS	Provides a means to draw a form image on the display screen and store it in a file for future use.
EUR71	This DROM should be loaded when using an HP 9871A with the European Character disc.
XDISC	This DROM is only found on the System Support disc, and must be loaded to use the FALIGN program.

Self-Test and Loader CRT Indications

After the self-test has been completed and the loader either loads or attempts to load the Operating System, several possible indicators may appear on the CRT.

-Indication-	-Meaning-
Failed part of Self-Test	-See Diagnostic Tests and Procedures
Flashing Cursor (no errors)	-Self-Test passed -Configured DROMs loaded -System ready for use
Error Message followed by Flashing Cursor	-Hardware and at least one full block and two upper half blocks of memory passed self-test -Operating System loaded successfully -There is at least 32 bytes of memory for the user and/or additional DROMs -BASIC Operating System is available but some programs may not execute if a required DROM is not loaded -See Codes and Messages
Error Message (no cursor)	-Operting System did not load -See Codes and Messages Codes
Blank CRT	-See Diagnostic Tests and Procedures

Configuration Program

The HP 250 System Configuration Program, CONFIG, is a utility program providing a means to access a collection of programs which allow the operator to define or check the status of various functions within the system.

Both the Operating System disc and the System Support disc contain the CONFIG program. The following list shows the options available when CONFIG is run.

1	DROM list	6	Keyboard edit
2	DROM edit	7	Auto start
3	Peripheral list	8	Memory configuration
4	Peripheral edit	9	Remote I/O configuration
5	Keyboard list	10	Set printer

DROM list: Lists all DROMs configured to auto-load and those which are currently loaded as part of the Operating System.

DROM edit: Allows the operator to select the DROMs that will auto-load when the Operating System loads at turn-on.

Peripheral list: List peripheral device, driver, and select code for devices using the Peripheral Interface Channel.

Peripheral edit: Not currently available. Will allow the operator to specify non-standard devices to be used on the Peripheral Channel.

Keyboard list: List the main and auxillary keyboards configured to auto-load at turn-on and others that are available.

Keyboard edit: Allows the operator to select the main and auxillary keyboards to auto-load at system turn-on.

Auto start: Allows a specific statement to automatically be executed or displayed at turn-on.

Memory configuration: Allows the operator to designate which memory boards the Operating System will see at turn-on. This program also allows the operator to assign user memory space to be used to store additional DROMs at turn-on.

Remote I/O configuration: Allows the operator to define the device class/type, format, and priority for each of the asynchronous data communication ports.

Set printer: Allows the user to specify the default output device for the DROM list, Peripheral list, and Keyboard list routines.

Running the Program

Perform the following steps to run the HP 250 System Configuration program.

1. Insert an Operating System or System Support disc.
2. Type: RUN "CONFIG" 
3. Follow program directions.

After all options have been selected and stored using the System Configuration program, the HP 250 must be powered down and then back up for the changes to become effective in the Operating System. For more details on the CONFIG program, see Appendix C of the BASIC Programming manual.

The HP 250 System Test Program, TEST, is a utility program providing a means to access four test routines used to verify proper operation of the system hardware and software.

Both the Operating System disc and System Support disc contain the TEST program. The following list shows the tests that are available.

DISPLAY TEST
PRINTER TEST
MASS MEMORY TEST
SYSTEM VERIFICATION TEST

DISPLAY TEST: This test displays all character sets and display enhancements configured to load. Also included is an Alignment and Focus test pattern used for CRT maintenance.

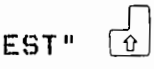
PRINTER TEST: This test checks the selected printer. The printout should be compared with the original printout made during system installation.

MASS MEMORY TEST: This is a series of tests to check the operation of the selected disc drive.

SYSTEM VERIFY: This test checks the Operating System. These DROMS must be loaded for the test: IMAGE, SORT, FORMS, and REPORT WRITER.

Running the Program

Perform the following steps to run the Hp 250 System Test program.

1. Insert an Operating System or System Support disc
2. Type: RUN "TEST" 
3. Follow program directions.

Additional information on the System Test can be found in the System Operators Guide.

CHAPTER 2

Installation

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HP Responsibilities

The purchase price of the HP 250 includes the following customer services. The Hewlett-Packard Customer Engineer is responsible for performing each of the tasks listed.

1. Conducting site preparation visit
2. Supervising uncrating and system positioning
3. Inventorying shipment against the packing list
4. Inter-connecting system modules
5. Executing turn-on procedures
6. Verifying system operation
7. Loading specified software
8. Instructing operator on daily care and proper use of system
9. Completing "System Installation Report"

The purchase price of the HP 250 system includes a site planning and preparation consultation visit by the Customer Engineer. A pre-installation site verification visit is NOT included.

The site planning and preparation visit aids the Customer Engineer as much as it does the customer, so the following items should be given careful attention.

1. The receiving and unpacking area should be at least 9 square metres because the system is shipped in a large wooden crate and several smaller cartons.

2. All doors, elevators, and passageways enroute to the installation site should be checked to ensure that the crate has adequate passage.

3. The following physical constraints affect the placement of the HP 250.
   -A clearance of at least 1 metre is required in front and back of the console for servicing.
   -The system printer must be within 838 mm (33 in.) or less of the console to accomodate the standard length cable.
   -A space of 692 mm (27 in.) must be provided behind the printer stand enclosure to open the rear door.

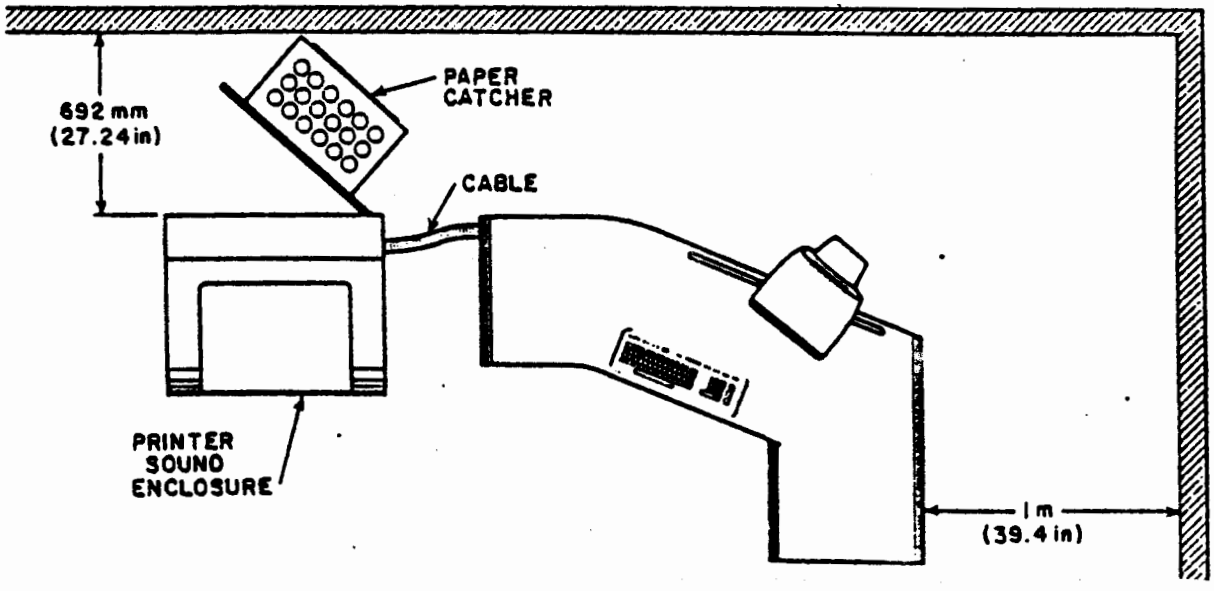


Figure 2-1: Required Servicing Area

4. The ac power outlet to be used with the HP 250 system should be within 2 metres of the console, and must have a ground connection. (The system power cord is a three-conductor cord, 3 metres in length.)

5. The system ac power requirement is 100V, 120V, 220V, or 240V. The line frequency must be 50Hz or 60Hz, + or - 3%.

6. The customer should be reminded that local laws, codes, and regulations may exist that affect the installation of his system. It is the customer's responsibility to check on these.

7. Floor coverings for the system installation location should have a minimum of static discharge. If necessary anti-static mats or anti-static spray should be used.

8. Areas of high particle contamination should be avoided when selecting a system installation location.

9. For the console and optional peripheral equipment, these component positions are recommended:

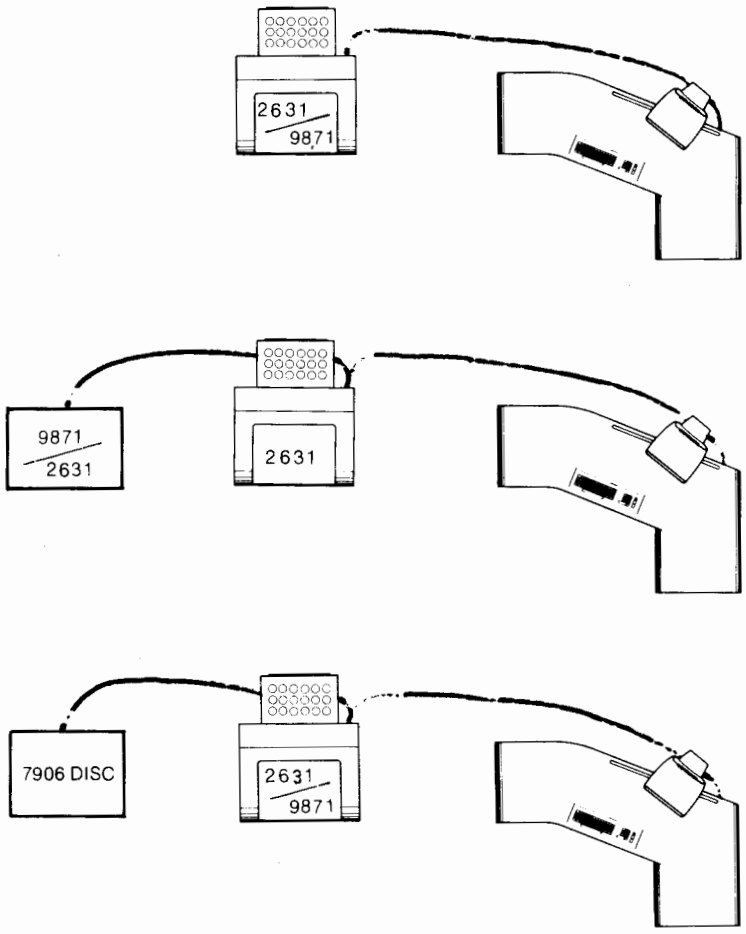
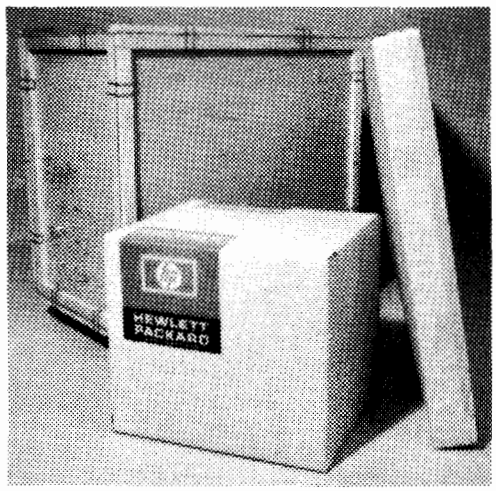


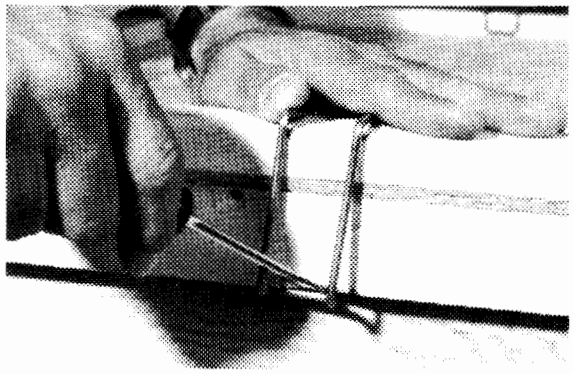
Figure 2-2: Recommended Component Positioning

System Unpacking

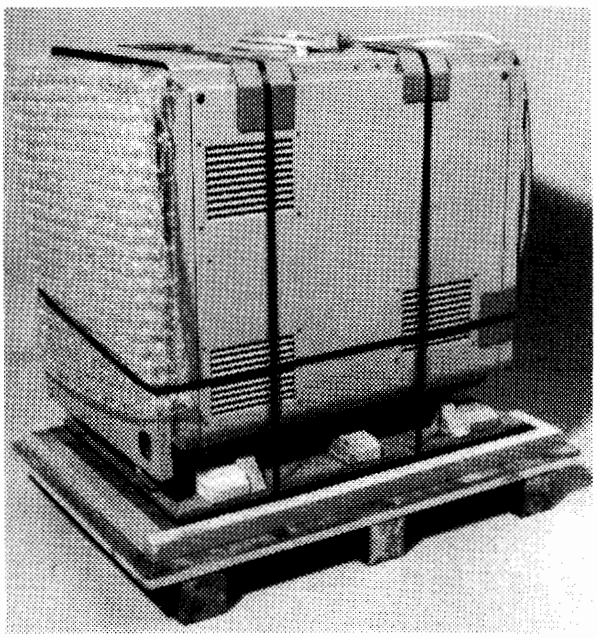
1. Check that all boxes are at the installation site.



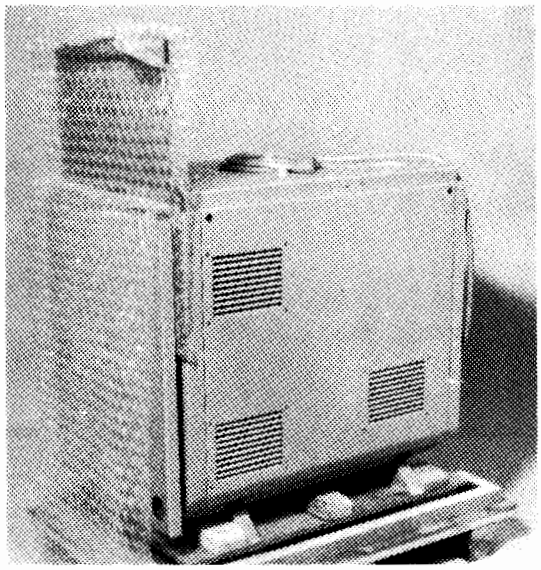
2. Remove the packing hooks from the mainframe crate.



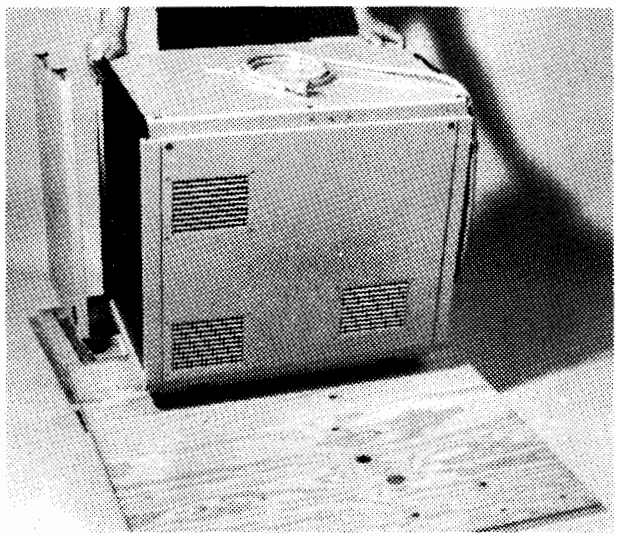
3. Remove the top and sides of the mainframe.



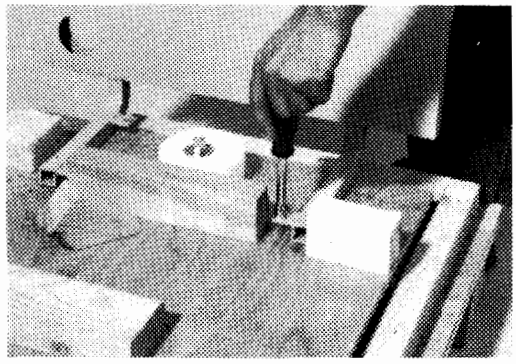
4. Cut the shipping bands and remove the accent panel.



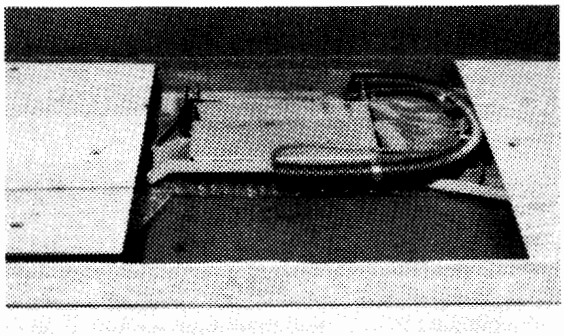
5. Using the side of the mainframe crate as a ramp, slowly roll the mainframe off the pallet.



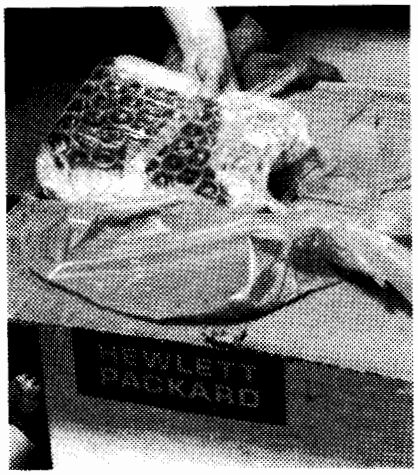
6. Remove the leg assembly from the pallet. Set the pallet aside.



7. Position the console-top box upside down, then cut the tape and remove the bottom. Set all manuals and accessories aside leaving the console top in the box.



8. Open the CRT box. Set the copy stand aside and inspect the CRT for damage.



9. Unpack any optional peripherals (printers, terminals, disc, etc.) and check for damage.

10. Check the acessories packaged with the console top and with each peripheral device.

Packaged with console top:

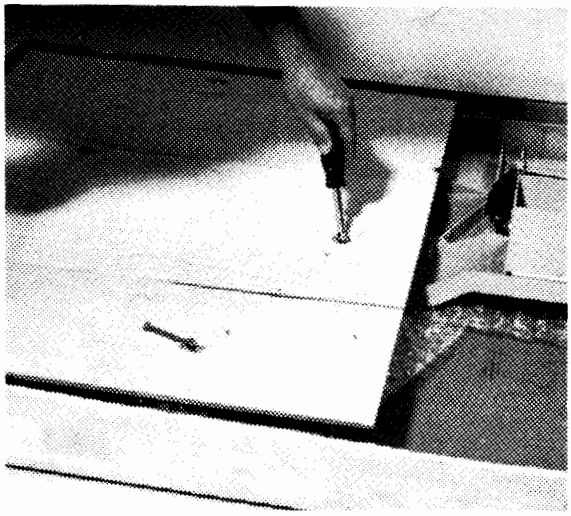
blank disc(initialized)	2ea	45251-10100
Operating System disc	2ea	45251-13000
on/off keys	2ea	
SFK overlays	5ea	7120-7497
Peripheral Interface Cable	1ea	8120-2720
Documentation Kit	1ea	45251-87901

Peripheral devices:

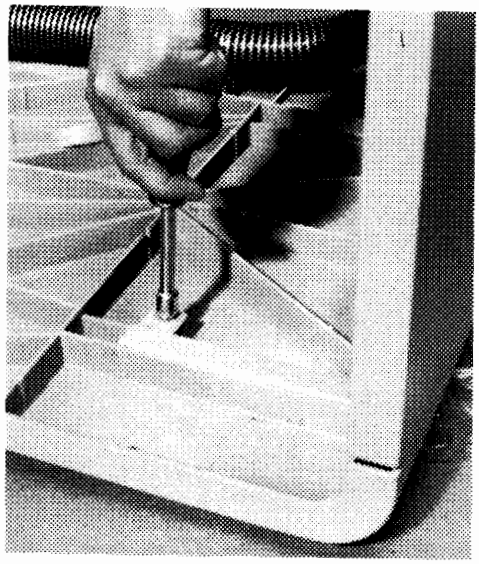
Check the documentation shipped with each peripheral.

System Assembly

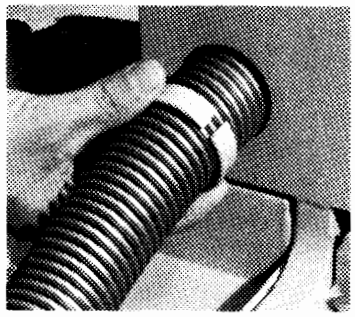
1. Remove the shipping boards from the console top.



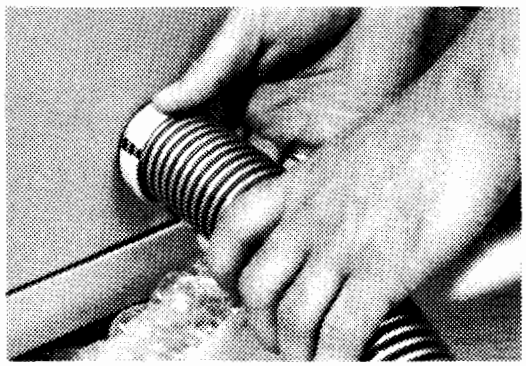
2. Attach the console leg to the top using four bolts.



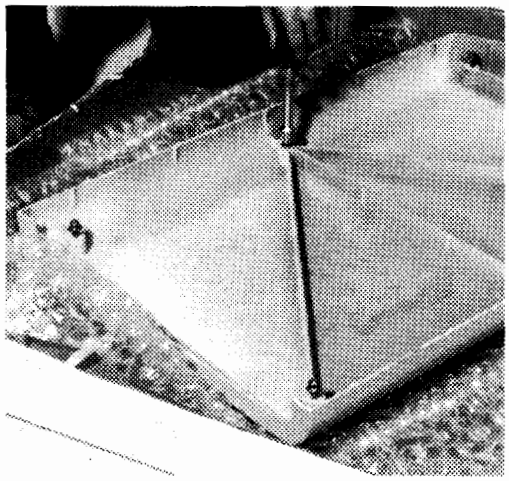
3. Feed the cable manager (tube) through the leg.



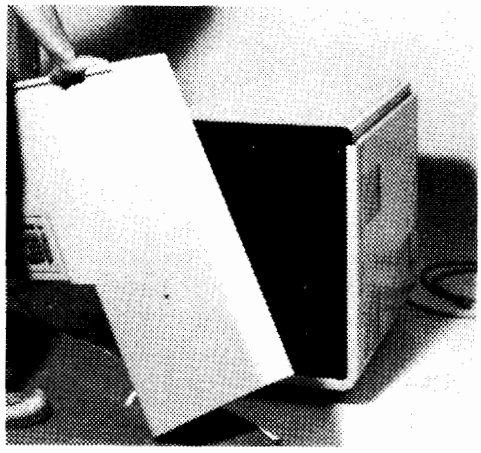
4. Install the cable manager locking collars: snap one collar on the inside of the tube, pull the tube tight, snap the other collar on the outside and screw the collar into place.



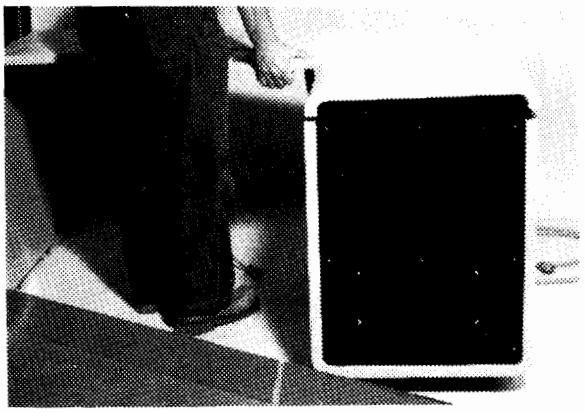
5. Screw in the five mounting studs on the console top.



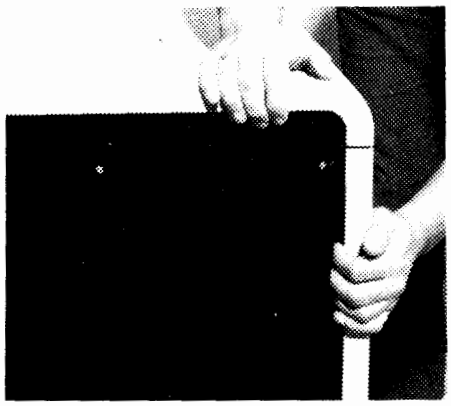
6. Position the mainframe next to the top/leg assembly.



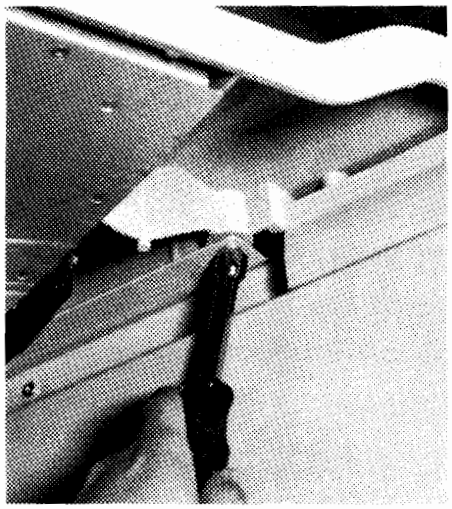
7. Lift the top/leg assembly and position it on the mainframe.



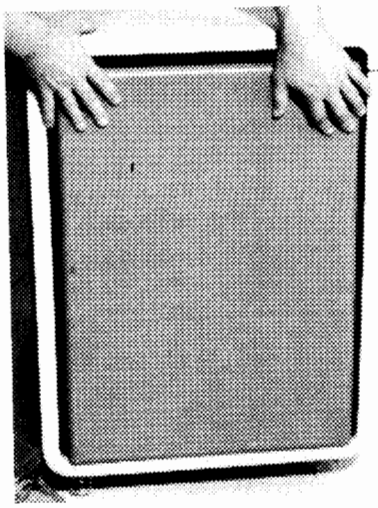
8. Slide the console top back until it is flush with the mainframe.



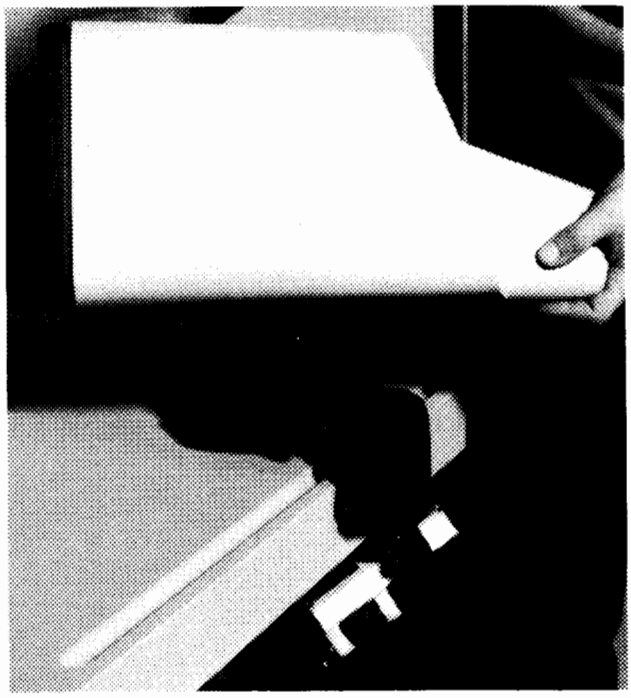
9. Secure the top with two allen head bolts then adjust the leg and tub feet until the console is level and stable.



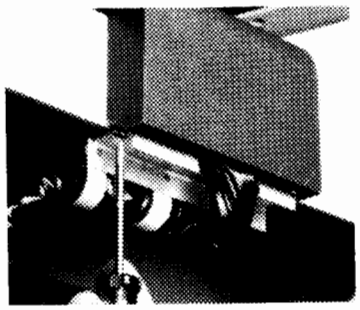
10. Install the accent panel on the main-frame.



11. Place the CRT in the center of its track.

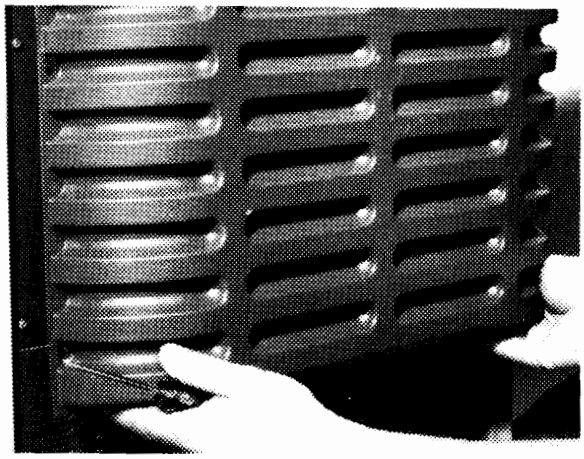


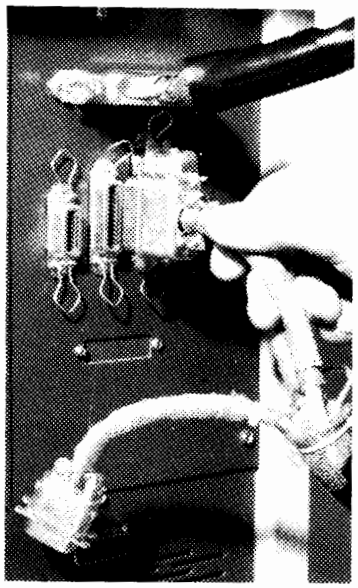
12. Secure the CRT retainer with two 6-32 machine screws.



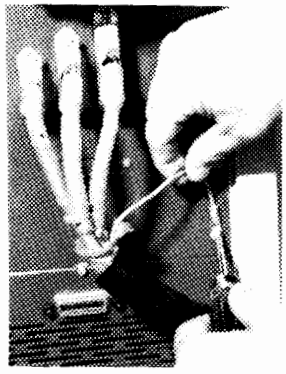
13. Form the CRT cable into a loop and place it behind the keyboard lower sheet-metal panel. Check that the CRT travels the full limit of the console-top groove.

14. Remove the mainframe cable cover by loosening the four mounting screws.





15. Connect the CRT and keyboard cables, and secure the cables under the console top.



16. Attach the ground-wire.

Component Positioning

The component positions shown in Figure 2-2 have been tested and are recommended for use.

Memory Board Switches .

Each memory board has either one or two Block Select Switches. The 32k byte board has one, and the 64k byte has two. These switches are used to give each 32k byte block of memory an address that is used by the Block Switch Board when addressing memory.

The following table shows the position of the switches that correspond to each particular memory block. See Chapter 3, Figure 3-21: Memory Board for picture and location of switches.

L=lower block
U=upper block

S 3	S 2	S 1	S 0	IDA 14	DECIMAL BLOCK #	OCTAL BLOCK #	S 3	S 2	S 1	S 0	IDA 14	DECIMAL BLOCK #	OCTAL BLOCK #
0	0	0	0	0	resrv*	resrv*	1	0	0	0	0	L 8	L 10
0	0	0	0	1	resrv*	resrv*	1	0	0	0	1	U 8	U 10
0	0	0	1	0	L 1	L 1	1	0	0	1	0	L 9	L 11
0	0	0	1	1	U 1	U 1	1	0	0	1	1	U 9	U 11
0	0	1	0	0	L 2	L 2	1	0	1	0	0	L 10	L 12
0	0	1	0	1	U 2	U 2	1	0	1	0	1	U 10	U 12
0	0	1	1	0	L 3	L 3	1	0	1	1	0	L 11	L 13
0	0	1	1	1	U 3	U 3	1	0	1	1	1	U 11	U 13
0	1	0	0	0	L 4	L 4	1	1	0	0	0	L 12	L 14
0	1	0	0	1	U 4	U 4	1	1	0	0	1	U 12	U 14
0	1	0	1	0	L 5	L 5	1	1	0	1	0	L 13	L 15
0	1	0	1	1	U 5	U 5	1	1	0	1	1	U 13	U 15
0	1	1	0	0	L 6	L 6	1	1	1	0	0	L 14	L 16
0	1	1	0	1	U 6	U 6	1	1	1	0	1	U 14	U 16
0	1	1	1	0	L 7	L 7	1	1	1	1	0	----	----
0	1	1	1	1	U 7	U 7	1	1	1	1	1	----	----

*block 0, upper and lower is
the self-test and loader ROM

Figure 2-3: Block Select Switch positions

-The Operating System requires Blocks 1 and 2, upper and lower.

-The User requires Block 16, upper as a minimum: Block 16, upper and lower is optional.

-Remote consoles and terminals require an upper Block as a minimum for each device: Upper and lower Blocks per device are optional. Use block numbers 3 thru 15 (octal).

-Block 17 (octal) is default--do not use this block address.

Self-test Switch

Set the self-test switch to position 0-3 as required.

-Position-	-Function-
0	Auto-start with flexible disc and hard disc self-test
1	Auto-start without flexible disc or hard disc self-test
2	Auto-start with flexible disc self-test
3	Auto-start with hard disc self-test

Operating System

The customer's Operating System disc should be configured to match the system hardware. The Configuration Program section of Chapter 1, Operation, explains the use of the CONFIG program.

NOTE

The CONFIG program requires a minimum of 28k bytes of user memory to run. It is possible to configure enough of the user memory for loading additional DROMs that the CONFIG program will not load. An ERROR 2, Memory Overflow will occur.

Should this happen, running the MFIG program will allow the Memory Configuration to be reconfigured without running CONFIG.

System Operation Verification

After all peripheral devices are connected to the HP 250 system and the Operating System loads, a System Operation Verification should be performed. This is accomplished by running the TEST program and performing each of the available routines. The System Test section of Chaper 1, Operation, gives instructions in using the TEST program.

NOTE

The printout of the PRINTER TEST should be maintained by the customer. This will act as a standard for comparison with printouts of PRINTER TEST run during the life of the system.

Customer Training

Customer training will help prevent unnecessary service calls. The following subjects should be discussed with the customer as the final step of the system installation.

- -normal turn-on indications
- -use of the following configuration programs
  - CONFIG
  - MFIG
  - RFIG
- -use of the following test programs
  - Display Test
  - Printer Test
  - Mass Storage Test
  - System Verify
- -proper flexible disc storage and handling techniques
- -importance of system back-ups
- -who to call for assistance
  - CE Support Services
  - SE Support Services
  - FE Support Services

Disc Drive Installation

The HP 250 system comes standard with one 1.2M byte disc drive. Up to two additional drives may be added to the system. These procedures cover the installation of a second and third drive to the base system.

1. Set the Drive Select Code Switch to position 1 for the second drive or 2 for the third drive.

2. Instal the AC Power Cable (W5) and the DC Power Cable (W6), as shown in Chapter 3, Figure 3-2: Condensed Wiring Diagram, to the AC and DC Power Bus respectively.

3. Push the Disc Drive cover-door down as far as it will go. Pull out slightly on the door handle and continue to push the cover-door down. This will expose the door-stop sheet-metal for the second or third drive.

4. Remove the four (4) screws securing the door-stop sheet-metal to the Tub Assembly, and remove the door-stop sheet-metal.

NOTE

Each drive is identified by setting the positon of the Drive Select Code Switch. The drives should be numbered sequentially from top to bottom starting with 0 and ending with 2 if three drives are used.

5. Slide the desired drive(s) into the opening in the Tub Assembly. Secure the drive(s) to the tub with four (4) allen head screws.

6. Connect the AC Power Cable, DC Power Cable, and Disc Interconnect Cable to the drive(s). See Chapter 3, Figure 3-2: Condensed Wiring Diagram for cabling information.

7. Test each drive by sequentially installing an Operating System disc an power down then back up. Check that the disc drive passes self-test and that the Operating System will load from each disc drive.

Memory Board Installation

Due to power limitations on the HP 250 power supply, the maximum number of memory boards, either 32k or 64k, that can be installed in the card cage is five.

Perform the following steps to add additional memory.

1. Turn the HP 250 power OFF.

2. Set the new memory board Block Select Switch to an unused block. See Figure 2-3: Block Select Switch positions.

3. Insert the new memory board into a card cage slot designated for memory boards. See Figure 3-3: Card Cage Configuration in Chapter 3, Hardware.

4. Insert an Operating System disc and turn the HP 250 power on. Run the CONFIG program and reconfigure the Memory Configuration for the new memory block number(s).

CHAPTER 3

Hardware

Table of Contents

The HP 250 is an integrated system consisting of a CRT Assembly, Flexible Disc Drive Unit(s), roll-out Card Cage, Power Supply, optional HP 7910K Fixed Disk, and option data communication I/O ports. These sub-systems are linked together by a network of internal buses.

Here is a brief functional description of each of the HP 250 system components. A more detailed discussion can be found in the section pertaining to the particular board or device.

The CRT and SOFTKEYS are part of the CRT Assembly. The CRT converts three logic level input signals into the required drive currents to operate the display. The SOFTKEYS are eight mechanical switches whose functions are program controlled.

The KEYBOARD is an 8x16 matrix of inductive switches. No scanning or decoding of the matrix occurs at KEYBOARD. These logic operations occur within the card cage.

The DISC DRIVEs function primarily as a controller for the mechanical mechanisms of the drive units. Logic operations occur within the card cage.

The DISC CONTROLLER performs all logical operations required by the disc drive to perform read/write operations. All commands to the controller from the processor travel via the Peripheral Interface Channel.

The HP 7910K is internal to the HP 250 system, and provides 10-megabytes of fixed disk storage space. It is totally independent of the system except for its connection via the Peripheral Interface Channel.

The READ/WRITE MEMORY consists of a minimum of 160k-bytes of dynamic RAM, expandable to 192k-bytes. 128k-bytes are reserved for the operating system with the remainder available to the user. Additional memory may be added when required by certain peripheral devices.

The DISPLAY LOGIC provides video, horizontal, and vertical drive signals to the CRT; read/write storage for characters displayed on the screen; and the interface between the memory bus of the processor and the screen refresh read/write memory.

The PROCESSOR performs several functions: It generates timing to refresh dynamic memory, generates memory cycle completion signal, generates and checks parity information, provides timing and data/address control to ROMs, and controls its own input/output port.

The PERIPHERAL INTERFACE provides the capability for the system processor, via its I/O bus, to communicate with peripherals such as printers and discs, via the peripheral interface channel. Communications to peripheral devices is conducted using HP-IB protocol.

The POWER SUPPLY provides six different regulated voltages, one unregulated voltage, and the power on pulse (POP).

The BLOCK SWITCH allows the system to address more than 64k-words of memory. This additional addressing capability permits addressing of sixteen 32k-word memory blocks.

The ASYNCHRONOUS SERIAL INTERFACE provides data communication capabilites for the HP 250 using RS-232C. Direct, modem, and 20-mA current loop connections are available.

The SYNCHRONOUS SERIAL INTERFACE is not currently available.

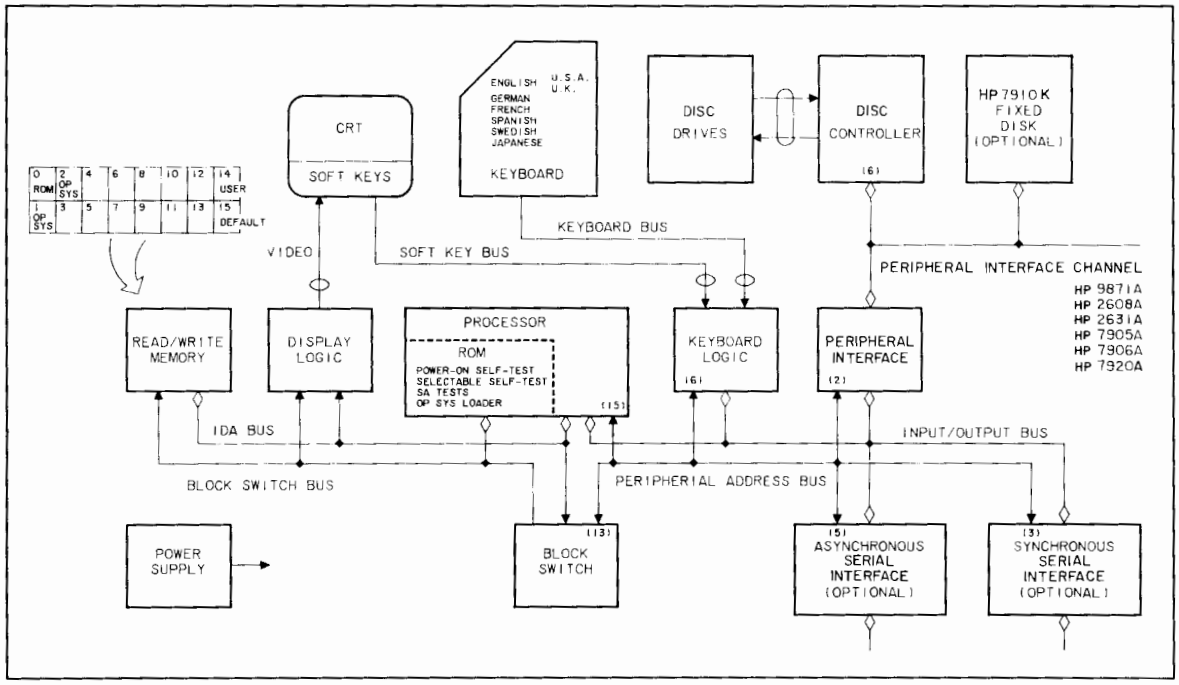
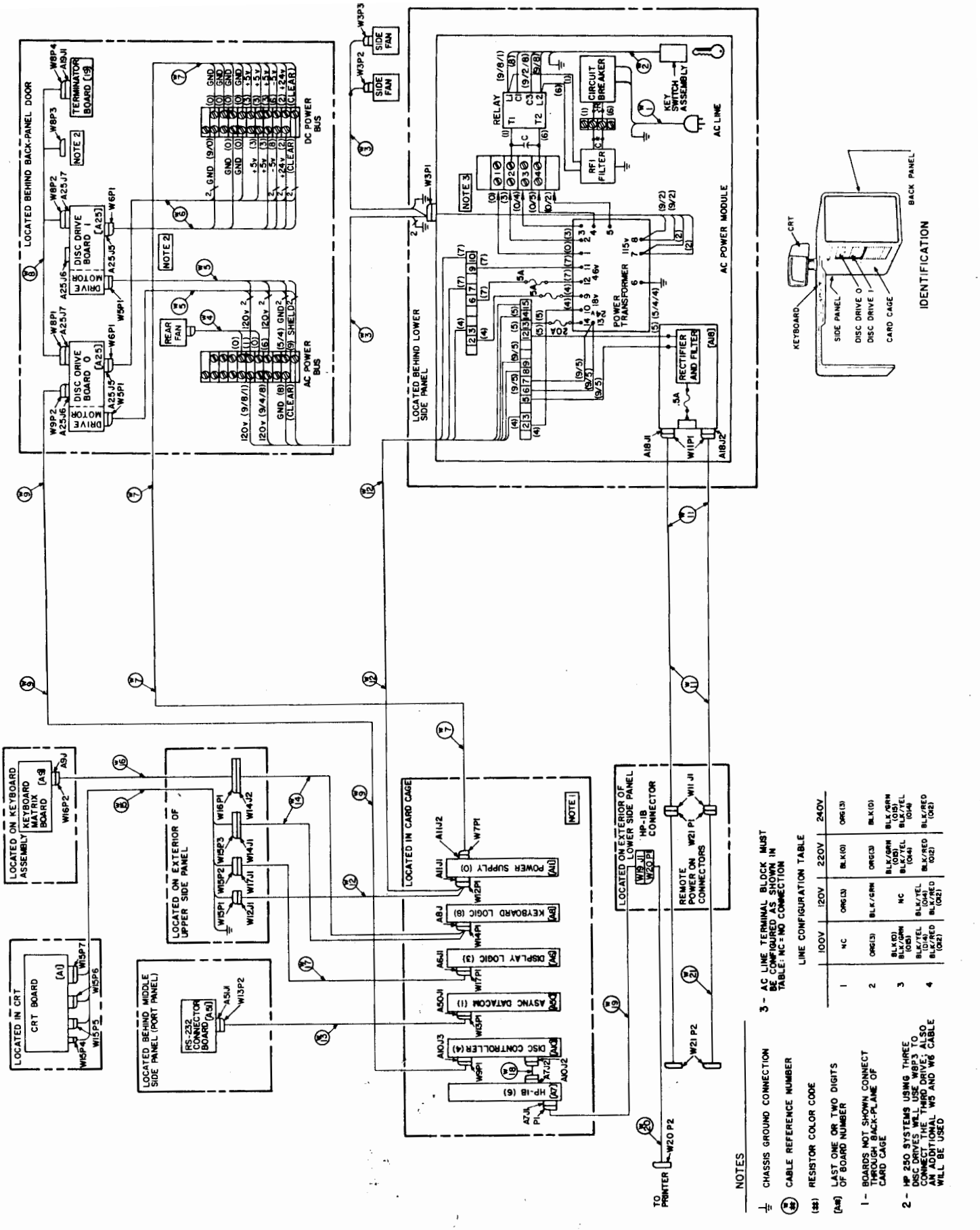


Figure 3-1: System Block Diagram



NOTES

⏚ CHASSIS GROUND CONNECTION

(*) CABLE REFERENCE NUMBER

(##) RESISTOR COLOR CODE

[A##] LAST ONE OR TWO DIGITS OF BOARD NUMBER

1 - BOARDS NOT SHOWN CONNECT THROUGH BACK-PLANE OF CARD CAGE

2 - HP 250 SYSTEMS USING THREE DISC DRIVES WILL USE W8P3 TO CONNECT THE THIRD DRIVE; ALSO AN ADDITIONAL W5 AND W6 CABLE WILL BE USED

3 - AC LINE TERMINAL BLOCK MUST BE CONFIGURED AS SHOWN IN TABLE: NC = NO CONNECTION

LINE CONFIGURATION TABLE

	100V	120V	220V	240V
1	N/C	ORG(3)	BLK(0)	ORG(3)
2	ORG(3)	BLK/GRN	ORG(3)	BLK(0)
3	BLK(0) BLK/GRN (015)	N/C	BLK/GRN (015) BLK/YEL (044)	BLK/GRN (015) BLK/YEL (014)
4	BLK/YEL (044) BLK/RED (012)	BLK/YEL (044) BLK/RED (012)	BLK/RED (012)	BLK/RED (012)

Figure 3-2: Condensed Wiring Diagram

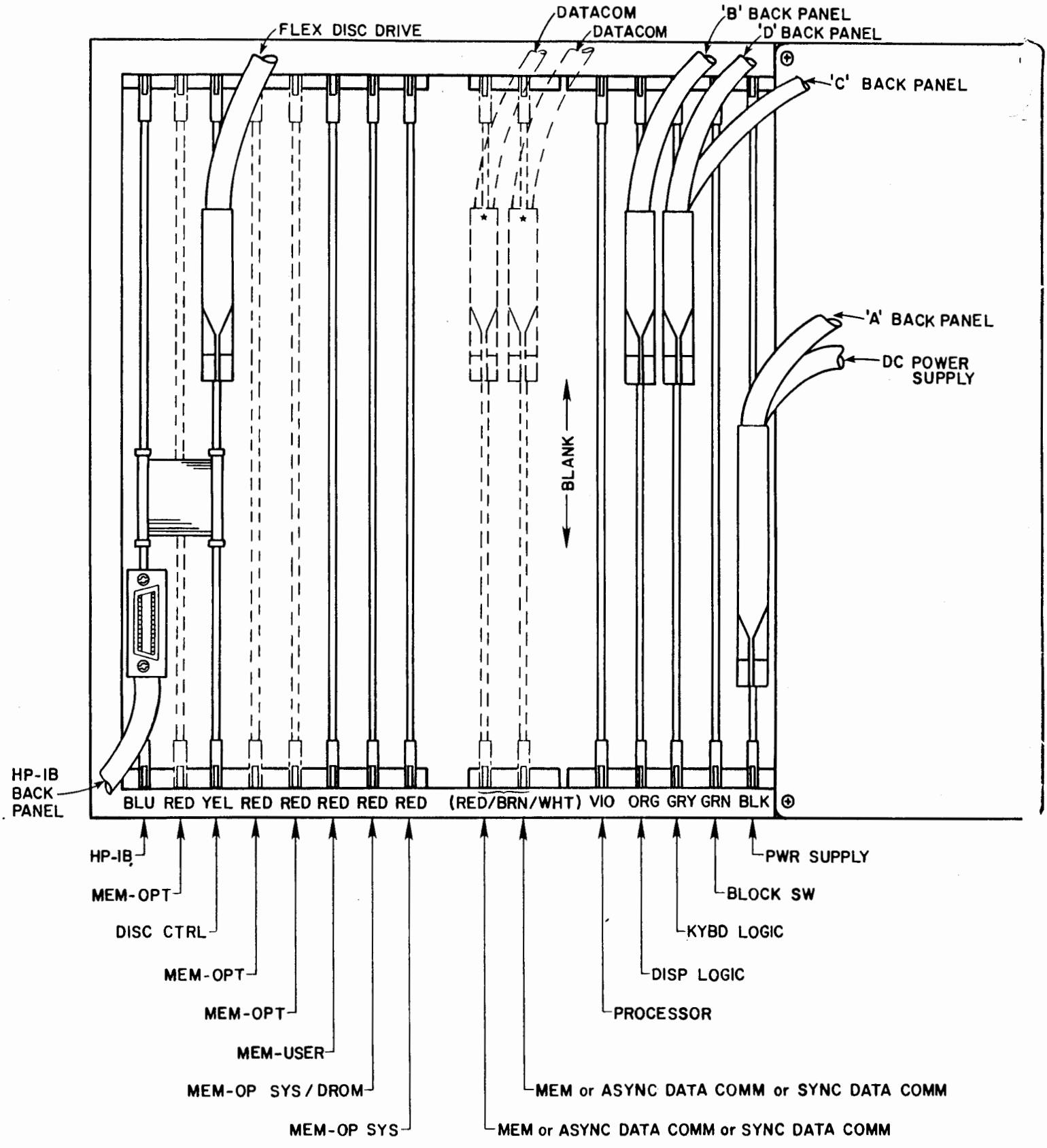
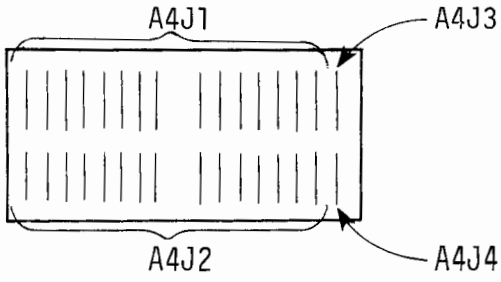


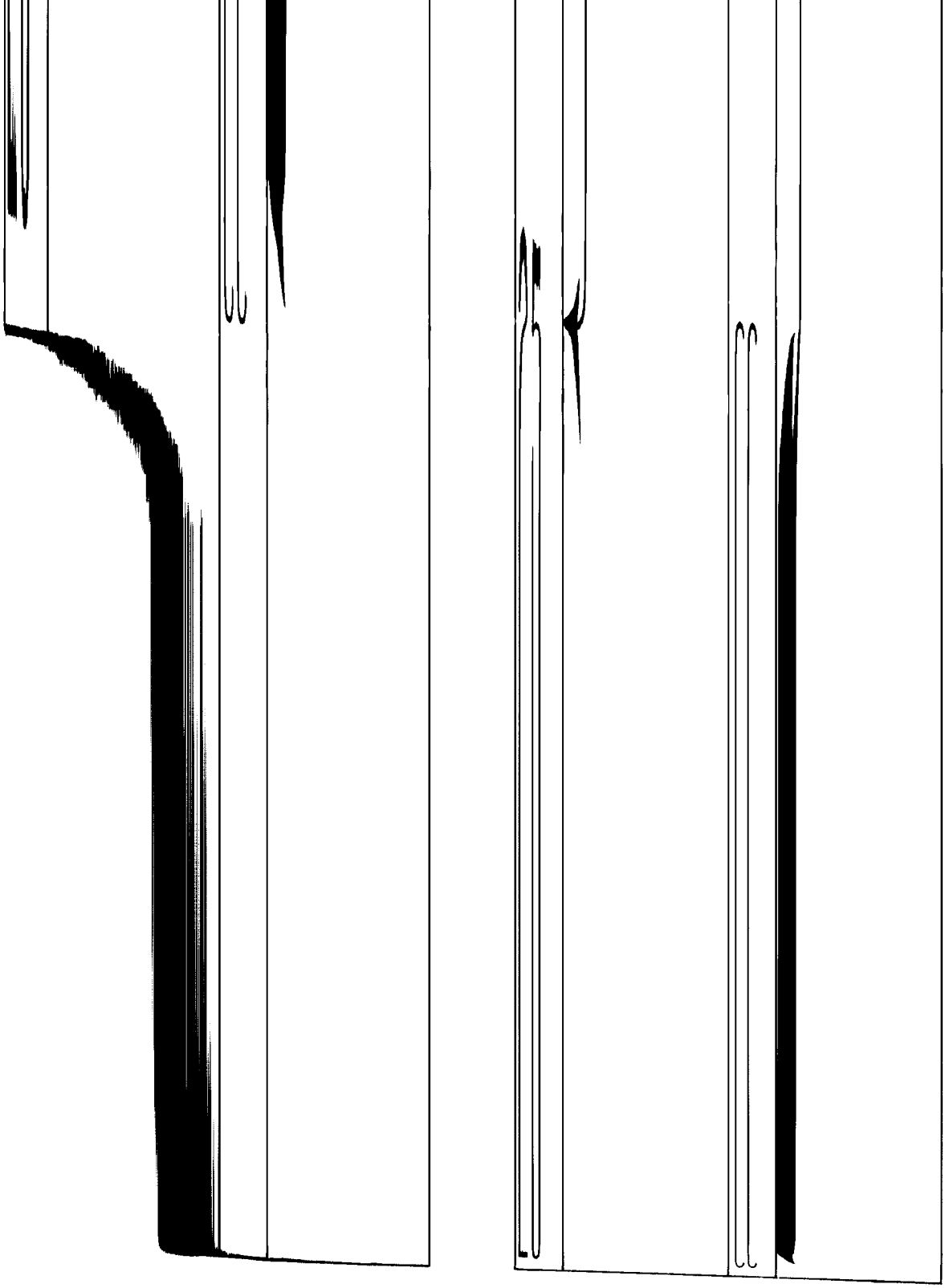
Figure 3-3: Card-Cage Configuration

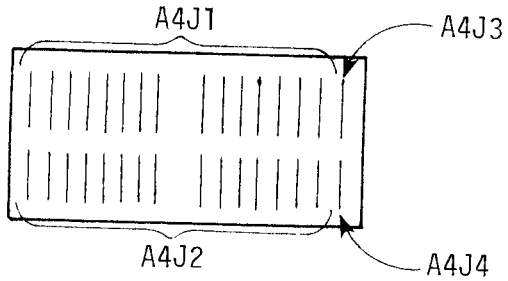
Table 3-1: Mother Board (A4) Connector Signals (backplane)

A4J1 Backplane			
Pin	Signal	Pin	Signal
1	+7V	A	+7V
2	Gnd	B	Gnd
3	Gnd	C	Gnd
4	$\overline{\text{IDA}}$ 9	D	$\overline{\text{IDA}}$ 8
5	$\overline{\text{IDA}}$ 11	E	$\overline{\text{IDA}}$ 10
6	$\overline{\text{IDA}}$ 13	F	$\overline{\text{IDA}}$ 12
7	$\overline{\text{IDA}}$ 15	H	$\overline{\text{IDA}}$ 14
8	$\overline{\text{IDA}}$ 6	J	$\overline{\text{IDA}}$ 7
9	$\overline{\text{IDA}}$ 4	K	$\overline{\text{IDA}}$ 5
10	$\overline{\text{IDA}}$ 2	L	$\overline{\text{IDA}}$ 3
11	$\overline{\text{IDA}}$ Ø	M	$\overline{\text{IDA}}$ 1
12	$\overline{\text{IDA}}$ 6	N	$\overline{\text{IDA}}$ 7
13	$\overline{\text{IOD}}$ 4	P	$\overline{\text{IOD}}$ 5
14	$\overline{\text{IOD}}$ 2	R	$\overline{\text{IOD}}$ 3
15	$\overline{\text{IOD}}$ Ø	S	$\overline{\text{IOD}}$ 1
16	$\overline{\text{IOD}}$ 14	T	$\overline{\text{IOD}}$ 15
17	$\overline{\text{IOD}}$ 12	U	$\overline{\text{IOD}}$ 13
18	$\overline{\text{IOD}}$ 10	V	$\overline{\text{IOD}}$ 11
19	$\overline{\text{IOD}}$ 8	W	$\overline{\text{IOD}}$ 9
20	$\overline{\text{SYNC}}$	X	BG
21	$\overline{\text{MEB}}$	Y	$\overline{\text{SMC}}$
22	$\overline{\text{STM}}$	Z	not used
23	Gnd	AA	Gnd
24	-5V	BB	-5V
25	+12V	CC	+12V

A4J2 Backplane			
Pin	Signal	Pin	Signal
1	+12V	A	+12V
2	-12V	B	-12V
3	Gnd	C	Gnd
4	$\overline{\text{IRH}}$	D	SØ
5	S1	E	$\overline{\text{IRL}}$
6	$\overline{\text{DMAR}}$	F	S2
7	S3	H	$\overline{\text{FLG}}$
8	$\overline{\text{STS}}$	J	$\overline{\text{HLT}}$
9	BYTE	K	BL
10	RFC	L	$\overline{\text{RFS}}$
11	$\overline{\text{ØIT}}$	M	$\overline{\text{SOB}}$
12	$\overline{\text{WRIT}}$	N	$\overline{\text{PA2}}$
13	$\overline{\text{PSB}}$	P	$\overline{\text{PAØ}}$
14	$\overline{\text{PAT}}$	R	$\overline{\text{IOSB}}$
15	$\overline{\text{STMR}}$	S	$\overline{\text{RAL}}$
16	$\overline{\text{DOUT}}$	T	$\overline{\text{IC2}}$
17	$\overline{\text{ICT}}$	U	$\overline{\text{Ø2T}}$
18	$\overline{\text{PBL}}$	V	$\overline{\text{PBU}}$
19	$\overline{\text{PA3}}$	W	$\overline{\text{INT}}$
20	not used	X	not used
21	$\overline{\text{BSI}}$	Y	$\overline{\text{POP}}$
22	Gnd	Z	Gnd
23	Gnd	AA	Gnd
24	+5V	BB	+5V
25	+5V	CC	+5V






A4J1
A4J3
A4J2
A4J4

CRT Board, A1

The CRT Board converts its three logic level input signals into the required drive currents to operate the CRT. The input signals are Video, Vertical Drive, and Horizontal Drive.

VIDEO--unblanks (turns on) the beam VERTICAL DRIVE--amplifies and provides a staircase ramp to the yoke

HORIZONTAL DRIVE--is used for two functions: It is amplified to drive the beam horizontally (sweep), and is used as an input to the high voltage (anode) generator.

The VIDEO signal is input to a differential amplifier whose gain is controlled by the Intensity Control. The signal then goes through an emitter follower to provide the unblanking signal to the CRT cathode.

The VERTICAL DRIVE signal is input to a staircase ramp generator, the gain of which is controlled by the Height Adjustment. The output of the ramp generator then goes through a vertical drive amplifier whose gain is controlled by the Vertical Centering Adjustment. The output of the amplifier then drives the vertical drive windings of the yoke.

The HORIZONTAL DRIVE signal goes through a compensation network to prevent the display from drifting off the screen. The resultant delayed signal is output to the horizontal drive windings of the yoke, and to the flyback transformer. The high voltage secondary of the transformer is run through a tripler to achieve the 15KV anode voltage. Lower voltage tap outputs are rectified and variably controlled to drive the intensity limit and focus grids of the CRT. A -45 volt tap is used to drive Grid1, and a +30 volt tap generates an internal supply voltage for the video amplifier.

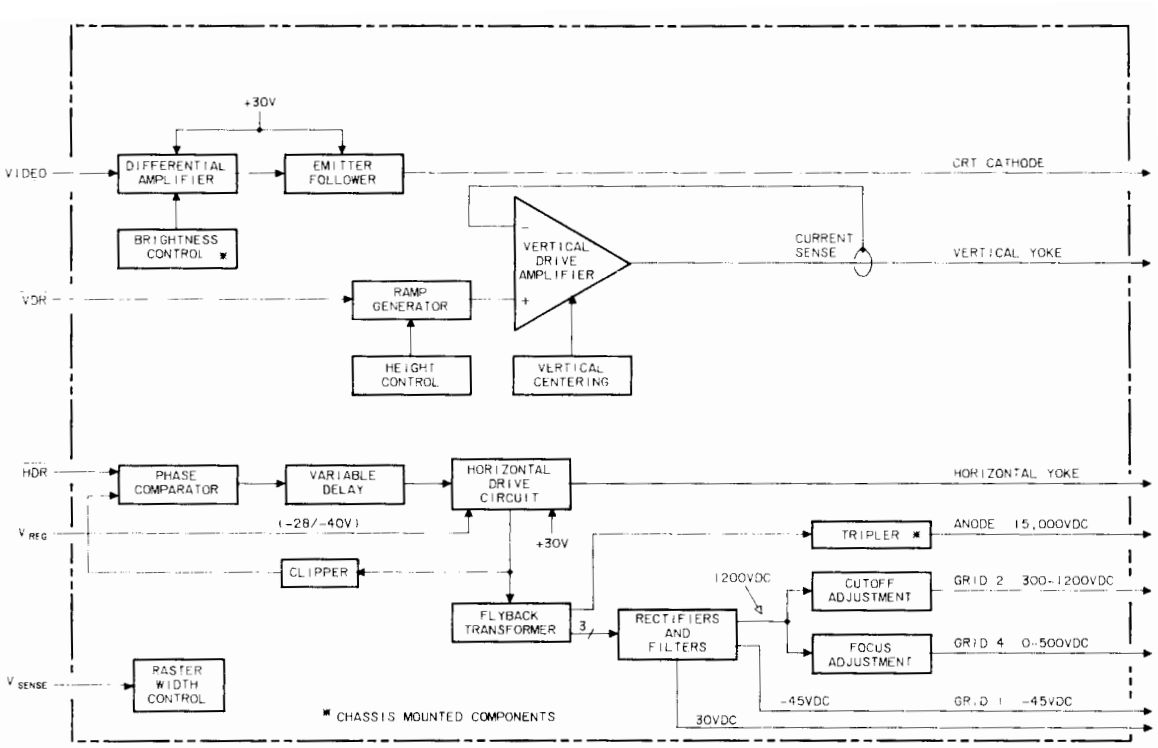


Figure 3-4: CRT Board Block Diagram

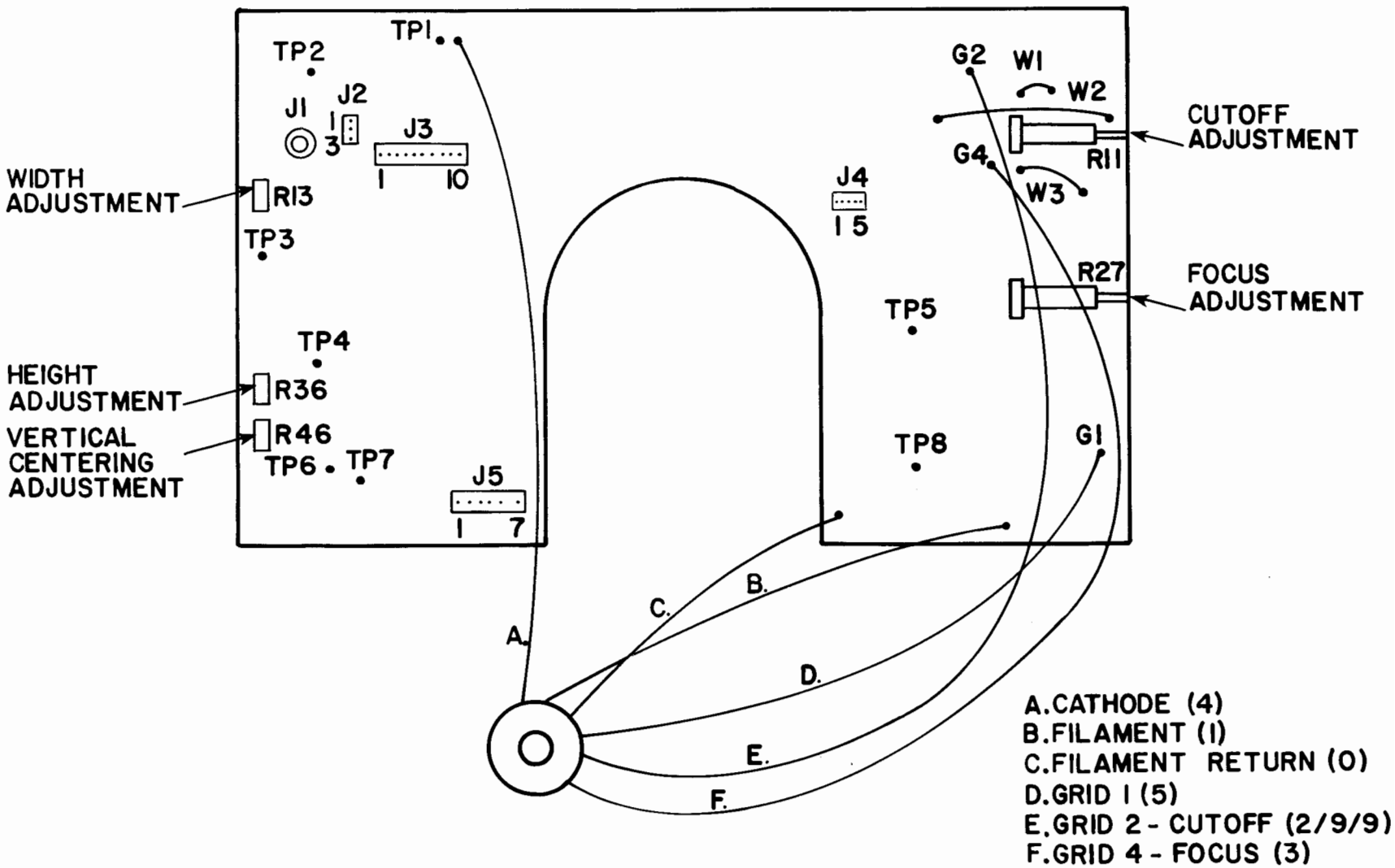


Figure 3-5: CRT Board, A1

Table 3-3: CRT Board (A1) Connector Signals

A1J1 Video Input	
Pin	Signal
1	Video

A1J2 Brightness Control	
Pin	Signal
1	Brightness
2	not used
3	Brightness

A1J3 Power Input	
Pin	Signal
1	VReg
2	not used
3	VSense
4	not used
5	not used
6	Gnd
7	Gnd
8	-12VDC
9	+12VDC
10	+5 VDC

A1J4 Vert/Horiz Inputs	
Pin	Signal
1	not used
2	$\overline{\text{VDR}}$
3	not used
4	not used
5	$\overline{\text{HOR}}$

A1J5 Yoke Outputs		
Pin	Signal	
1	VYoke	(5)
2	Gnd	(Ø)
3	VYoke	(6)
4	VYoke	(3)
5	HYoke	(9)
6	not used	
7	HYoke	(4)

Chart 3-1: CRT Board Controls

-Name-	-Description-	-Adjustment Procedure-
Width Adjustment (1,2)	Used to adjust the 80-character width to fill the display area.	Rotate the width adjustment until the ALIGN & FOCUS pattern fills the screen horizontally.
Height Adjustment (1)	Used to adjust the 24-column height to fill the display area.	The vertical centering adjustment should be made before the height adjustment. Rotate the height adjustment control until the ALIGN & FOCUS pattern fills the screen vertically.
Vertical Centering Adjustment (1)	Used to vertically center the 80 x 24 character display.	Rotate the vertical centering adjustment until the top of the ALIGN & FOCUS pattern is at the top of the display area.
Cutoff Adjustment	Used to limit the brightness intensity so that retrace lines are not visable at maximum brightness.	This adjustment must be made on a cold CRT. Turn the brightness control to maximum intensity and adjust the cutoff control until the retrace lines just disappear.
Focus Adjustment (1)	Used to adjust the focus for a clear sharp display.	The focus adjustment should be made after all other CRT adjustments have been made. Rotate the focus adjustment until the FOCUS & ALIGN pattern is clear and sharp.

(1)Adjustments should be made with the ALIGN & FOCUS pattern displayed on the CRT. Run the DISPLY program to get the pattern.

(2)The horizontal position should be adjusted prior to setting the display width. See the Chart 3-4: Display Logic Board Controls.

Chart 3-2: CRT Board Jumpers

-Name-	-Description-
W1	Normally disconnected--see explanation for W3
W2	Must always be connected--use high voltage wire. HP part number 8150-0138
W3	Normally connected--If cutoff cannot be adjusted properly, try any one of four possible combinations of jumpers W1 and W3 until cutoff can be adjusted. Use high voltage wire. HP part number 8150-0139

The Processor Board controls and buffers signals to and from the NMOS-II Microprocessor, the heart of the system. The microprocessor is a hybrid device consisting of three chips: BPC (Binary Processor Chip), EMC (Extended Math Chip), and IOC (Input/Output Control Chip).

The BPC controls most of the processor timing, and decodes and executes most of the HP 250 system instruction set.

The EMC performs the high accuracy and complicated math functions.

The IOC handles all I/O processing including DMA.

The Self Test and System Loader ROMs are located on the Processor Board. A POP (power on pulse) signal sets the processor to the beginning address of the Self Test routine which if successful, passes control to the System Loader and in turn the system software.

The Processor Board also generates memory cycle and refresh timeing, parity generation and checking, and system control signals.

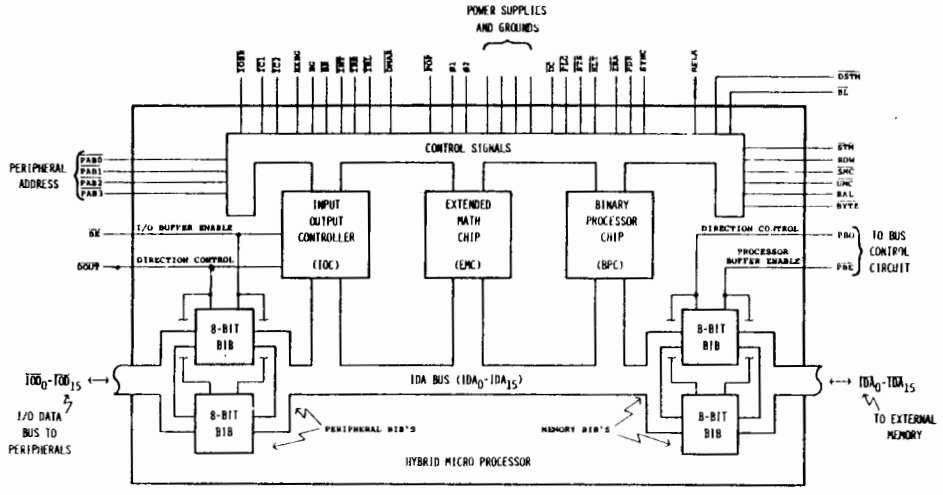


Figure 3-6: Hybrid Processor Block Diagram

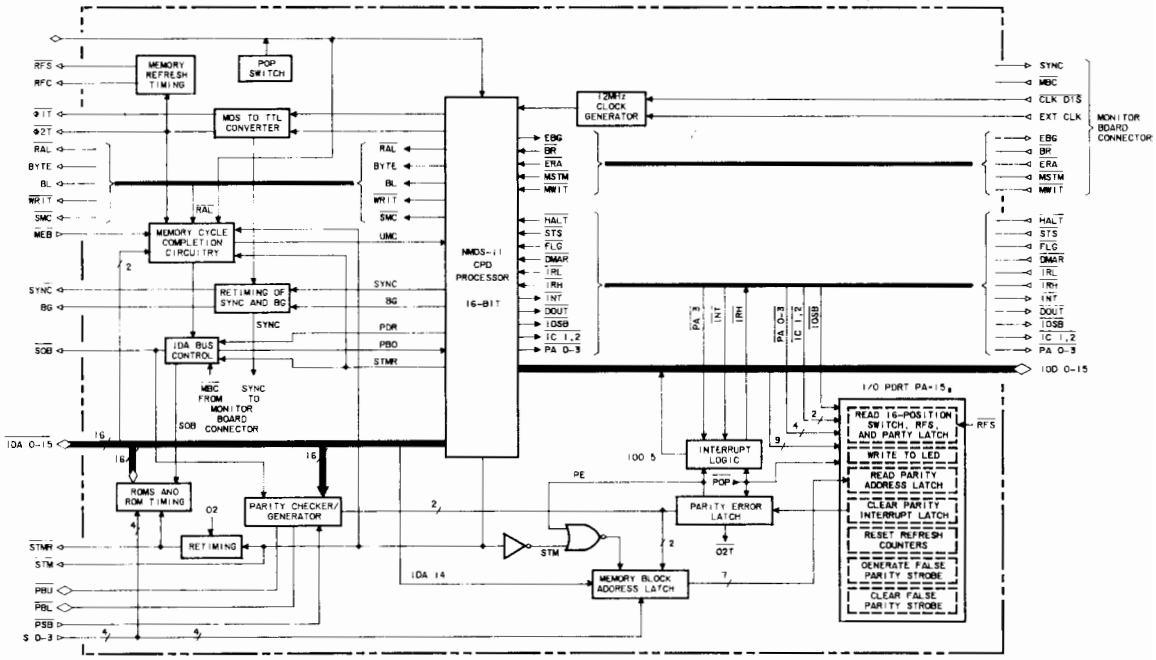


Figure 3-7: Processor Board Block Diagram

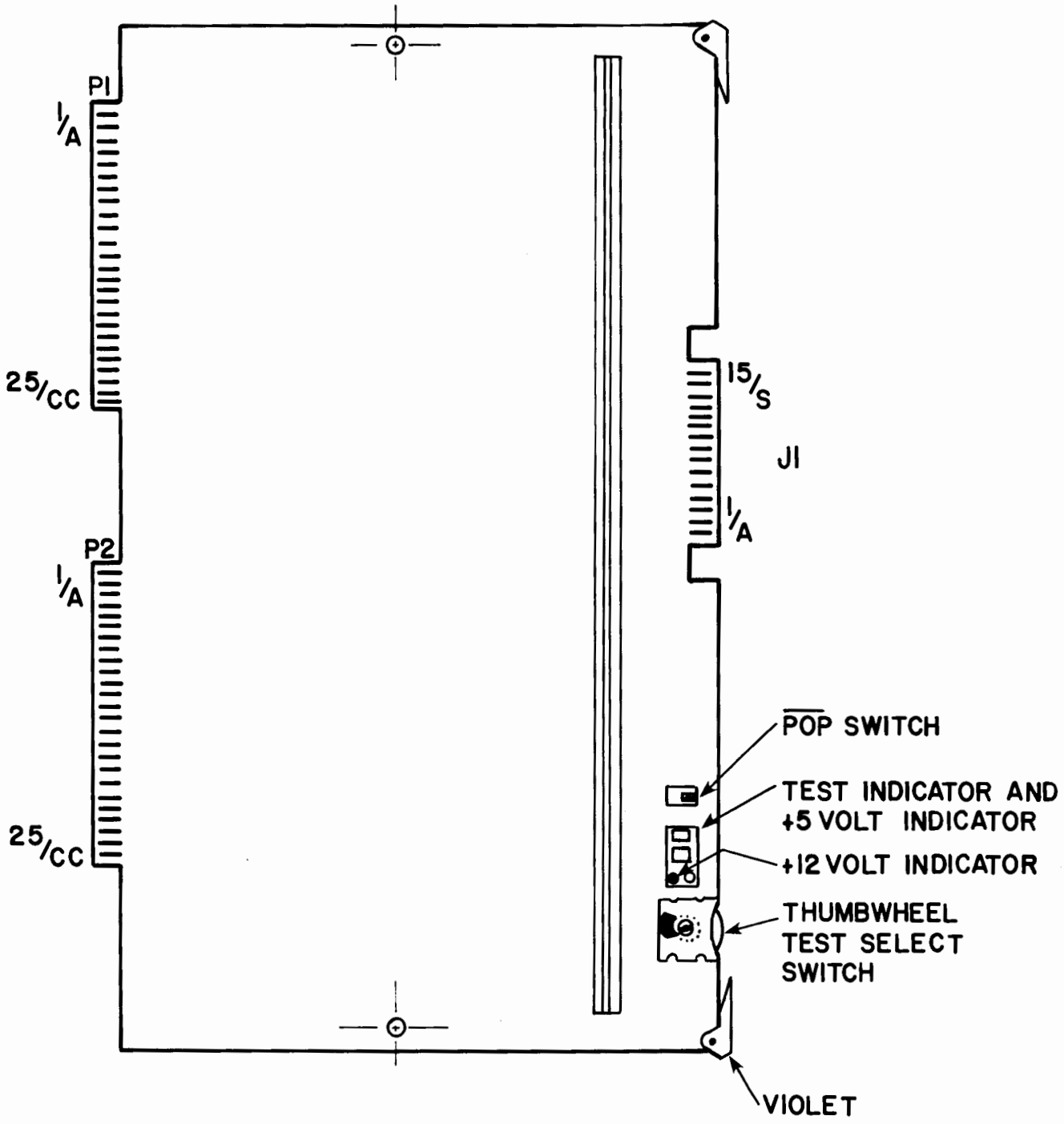


Figure 3-8: Processor Board, A5

Table 3-4: Processor Board Connector Signals

A5P1 Backplane			
Pin	Signal	Pin	Signal
1	+7V	A	+7V
2	Gnd	B	Gnd
3	Gnd	C	Gnd
4	$\overline{\text{IDA9}}$	D	$\overline{\text{IDA8}}$
5	$\overline{\text{IDA11}}$	E	$\overline{\text{IDA10}}$
6	$\overline{\text{IDA13}}$	F	$\overline{\text{IDA12}}$
7	$\overline{\text{IDA15}}$	H	$\overline{\text{IDA14}}$
8	$\overline{\text{IDA6}}$	J	$\overline{\text{IDA7}}$
9	$\overline{\text{IDA4}}$	K	$\overline{\text{IDA5}}$
10	$\overline{\text{IDA2}}$	L	$\overline{\text{IDA3}}$
11	$\overline{\text{IDA0}}$	M	$\overline{\text{IDA1}}$
12	$\overline{\text{IOD6}}$	N	$\overline{\text{IOD7}}$
13	$\overline{\text{IOD4}}$	P	$\overline{\text{IOD5}}$
14	$\overline{\text{IOD2}}$	R	$\overline{\text{IOD3}}$
15	$\overline{\text{IOD0}}$	S	$\overline{\text{IOD1}}$
16	$\overline{\text{IOD14}}$	T	$\overline{\text{IOD15}}$
17	$\overline{\text{IOD12}}$	U	$\overline{\text{IOD13}}$
18	$\overline{\text{IOD10}}$	V	$\overline{\text{IOD11}}$
19	$\overline{\text{IOD8}}$	W	$\overline{\text{IOD9}}$
20	$\overline{\text{Sync}}$	X	BG
21	$\overline{\text{MEB}}$	Y	$\overline{\text{SMC}}$
22	$\overline{\text{STM}}$	Z	not used
23	Gnd	AA	Gnd
24	-5V	BB	-5V
25	+12V	CC	+12V

A5P2 Backplane			
Pin	Signal	Pin	Signal
1	+12V	A	+12V
2	not used	B	not used
3	Gnd	C	Gnd
4	$\overline{\text{IRH}}$	D	S0
5	S1	E	$\overline{\text{IRL}}$
6	$\overline{\text{DMAR}}$	F	S2
7	S3	H	$\overline{\text{FLG}}$
8	$\overline{\text{STS}}$	J	$\overline{\text{HLT}}$
9	Byte	K	BL
10	RFC	L	$\overline{\text{RFS}}$
11	01T	M	$\overline{\text{SOB}}$
12	$\overline{\text{WRIT}}$	N	$\overline{\text{PA2}}$
13	$\overline{\text{PSB}}$	P	$\overline{\text{PA0}}$
14	$\overline{\text{PA1}}$	R	$\overline{\text{IOSB}}$
15	$\overline{\text{STMR}}$	S	$\overline{\text{RAL}}$
16	$\overline{\text{DOUT}}$	T	$\overline{\text{IC2}}$
17	IC1	U	$\overline{\text{02T}}$
18	$\overline{\text{PBL}}$	V	$\overline{\text{PBU}}$
19	$\overline{\text{PA3}}$	W	$\overline{\text{INT}}$
20	not used	X	not used
21	$\overline{\text{BSI}}$	Y	$\overline{\text{POP}}$
22	Gnd	Z	Gnd
23	not used	AA	not used
24	+5V	BB	+5V
25	+5V	CC	+5V

A5J1 Monitor Test-Connection			
Pin	Signal	Pin	Signal
1	Ext CLK	A	Gnd
2	CLK Disable	B	Gnd
3	not used	C	not used
4	not used	D	not used
5	not used	E	not used
6	not used	F	not used
7	$\overline{\text{SMC}}$	H	not used
8	$\overline{\text{POP}}$	J	not used
9	$\overline{\text{BR}}$	K	EBG
10	not used	L	not used
11	$\overline{\text{ERA}}$	M	$\overline{\text{MBC}}$
12	$\overline{\text{SYNC}}$	N	not used
13	$\overline{\text{MSTM}}$	P	not used
14	$\overline{\text{MWRIT}}$	R	not used
15	not used	S	not used

Chart 3-3: Processor Board Controls and Indicators

-Name-	-Description-	-Adjustment Procedure-
Test Indicator	Is a 7-segment LED with decimal point. The decimal point, when lit, indicates the presence of +12V. Any segment lit indicates the presence of +5V. The number displayed by the LED indicates the last self-test that was passed. See Card-Cage Board Build-up procedures in Chapter 5 for LED test number information.	none
POP Switch	This switch initializes all system circuits and initiates self-test and loader routines.	none
Thumbwheel Test Select Switch	This is a 16-position rotary switch used to select the desired ROM self-test to be initiated at turn-on or with the POP switch. Not all switch positions are available for use.	See Chapter 5 for details on the tests available for each switch position.

Display Logic Board, A6

The Display Logic Board has three primary functions. They are:

To provide video, horizontal, and vertical drive signals to the CRT analog electronics.

To provide read/write storage for characters displayed on the screen so that screen refresh is automatically provided.

To provide an interface between the memory bus of the processor and the screen refresh read/write memory.

The basic timing for the board is derived from a 23.690 Mhz crystal clock, the duty cycle of which is 60%. The clock is divided down many times to provide the necessary timing.

The sequential address counter serves the function of incrementing through the screen refresh memory locations at the proper time. This counter is enabled during the 80 character sweep of the display, and disabled during the 37 character retrace time. During normal refresh operation, the output of the sequential address counter passes through multiplexers before going to the even and odd RAMs.

The RAMs are addressed, then they are enabled by the chip select signal. The output multiplexer alternately looks at the odd and even RAMs at the appropriate time. The output multiplexer also retimes the multiplexed output data with the character clock.

The accessed data from RAM is then converted to character forms by addressing character ROMs. Each ROM contains 128 character forms, and the board can hold up to four ROMs. The parallel output of the ROMs is converted to serial data and then goes through the video enhancement logic. The resulting video signal input to the 75 ohm line driver, and then output as the video signal to the CRT Board.

Address decoding circuits continually monitor the IDA bus and the Block Switch bus. When address 74000 through 77777 occur for block 0, the address and data are stored in the one word registers. Write timing logic th then determines the appropriate time to write into the screen refresh RAM. The time to write into the even RAM is when the odd RAM is being read and the time to write into the odd RAM is when the even RAM is being read. This prevents the screen display from being disturbed during the time the refresh RAM is being updated.

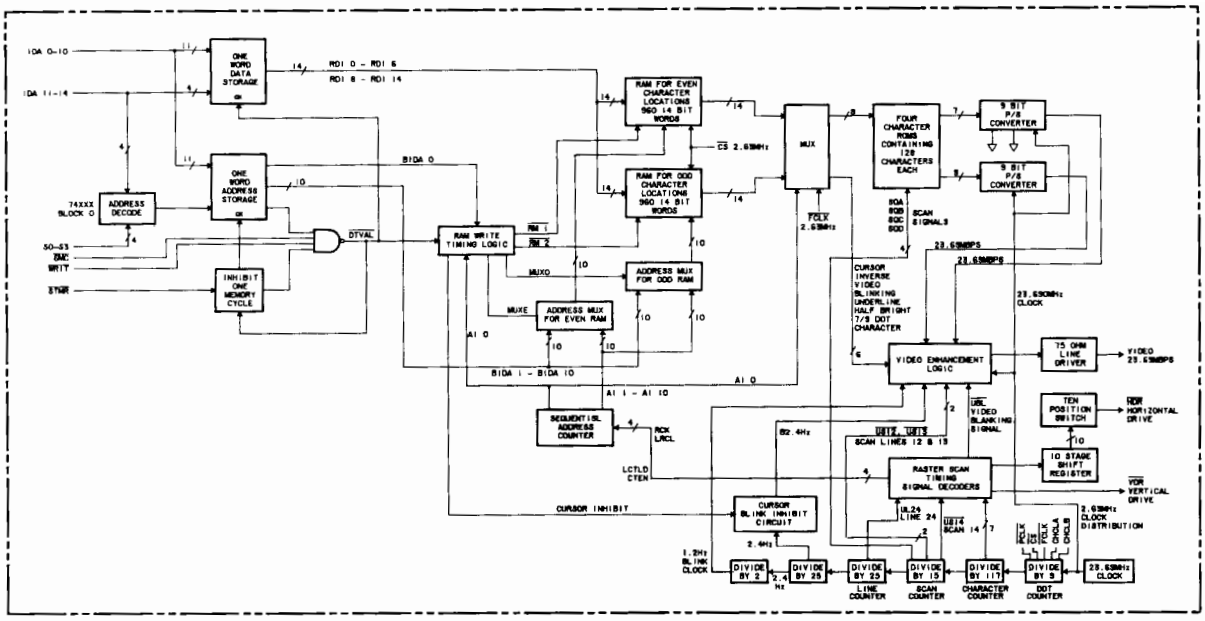


Figure 3-9: Display Logic Board Block Diagram

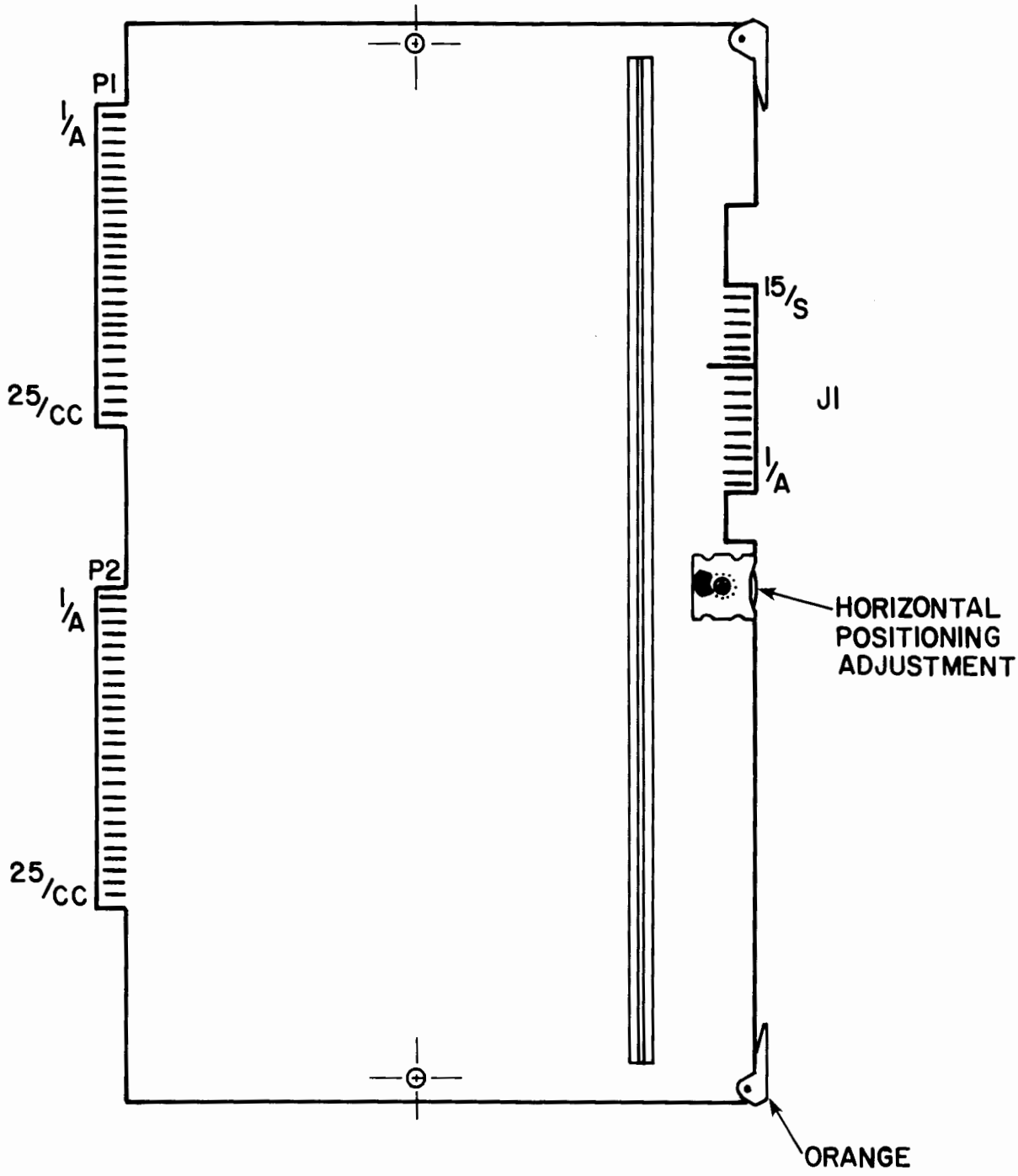


Figure 3-10: Display Logic Board, A6

Table 3-5: Display Logic Board Connector Signals

A6P1 Backplane			
Pin	Signal	Pin	Signal
1		A	
2		B	
3		C	
4	$\overline{IDA}$ 9	D	$\overline{IDA}$ 8
5	$\overline{IDA}$ 11	E	$\overline{IDA}$ 1Ø
6	$\overline{IDA}$ 13	F	$\overline{IDA}$ 12
7	$\overline{IDA}$ 15	H	$\overline{IDA}$ 14
8	$\overline{IDA}$ 6	J	$\overline{IDA}$ 7
9	$\overline{IDA}$ 4	K	$\overline{IDA}$ 5
10	$\overline{IDA}$ 2	L	$\overline{IDA}$ 3
11	$\overline{IDA}$ Ø	M	$\overline{IDA}$ 1
12		N	
13		P	
14		R	
15		S	
16		T	
17		U	
18		V	
19		W	
20		X	
21		Y	$\overline{SMC}$
22		Z	
23		AA	
24	-5V	BB	-5V
25	+12V	CC	+12V

A6P2 Backplane			
Pin	Signal	Pin	Signal
1	+12V	A	+12V
2		B	
3		C	
4		D	SØ
5	S1	E	
6		F	S2
7	S3	H	
8		J	
9		K	
10		L	
11		M	
12	$\overline{WRIT}$	N	
13		P	
14		R	
15	$\overline{STMR}$	S	
16		T	
17		U	
18		V	
19		W	
20		X	
21		Y	
22		Z	
23		AA	
24	+5V	BB	+5V
25	-5V	CC	-5V

A6J1 CRT Assembly			
Pin	Signal	Pin	Signal
1	Gnd	A	
2	Gnd	B	Video
3		C	
4	Gnd	D	$\overline{HDR}$
5		E	
6	Gnd	F	$\overline{VDR}$
7		H	
8		J	
9		K	
10		L	
11		M	
12		N	
13		P	
14		R	
15		S	

Chart 3-4: Display Logic Board Controls

-Name-	-Description-	-Adjustment Procedure-
Horizontal Positioning Adjustment	Used to horizontally center the 80x24 character display	Rotate the Horizontal Positioning Adjustment until the ALIGN & FOCUS pattern is centered left and right on the display. If the pattern is too wide, see the Width Adjustment procedures in Chart 3-1: CRT Board Controls. (1)

(1)Adjustments should be made with the ALIGN & FOCUS pattern displayed on the CRT. Run the DISPLY program to display the pattern.

Peripheral Interface Board, A7

The Peripheral Interface Board uses a Processor-to-HPIB Interface Chip (PHI). The PHI chip is responsible for driving the Peripheral Interface Channel control lines in a manner consistant with HP-IB protocol. The processor is therefore not burdened with details such as handshake timing. The remaining hardware on the interface board provides the processor with a means of accessing the PHI chip's registers for data transfer. Data transfer via programmed I/O or DMA is permitted as well as interrupt capabilities.

The processor initiates data transfers to or from the PHI's registers via the Instruction Latch/Decoder on the interface board. Information stored in the instruction latch indicates which register the processor wants to access, whether a read or a write is desired, and whether the transfer is to be done via DMA.

The PHI register data passes through the Data Latch. During DMA, a first-in/first-out (FIFO) buffer is switched in between the Data Latch and the PHI chip: It helps to synchronize data flow. During programmed I/O, data passes directly between the Data Latch and the PHI chip.

Once an instruction has been received by the interface, the data transfer is controlled by the PHI Access Control (ASM). During DMA transfers, a second ASM called the Byte-Packing Control is also used. The Byte-Packing Control is responsible for data transfer between the FIFO and the Data Latch, and between the Data Latch and the processor. Data transfer between the FIFO and the PHI chip is handled by the PHI Access Control.

The Fullness Counter keeps track of the FIFO's status and informs the two state machines. The counter as well as the state machines are driven by a clock internal to the Peripheral Interface Board.

The Bus Cycle Logic decodes the interface's peripheral address and determines whether a given I/O bus cycle accesses the Instruction Latch/Decoder or the Data Latch.

The Interrupt Request Logic accepts a request for interrupt from the PHI chip or the Byte-Packing Control. The request is then set to the IOC through the I/O bus of the processor.

The DMA Request Logic, driven by the Byte-Packing Control and the Fullness Counter, drives the I/O bus DMA request line.

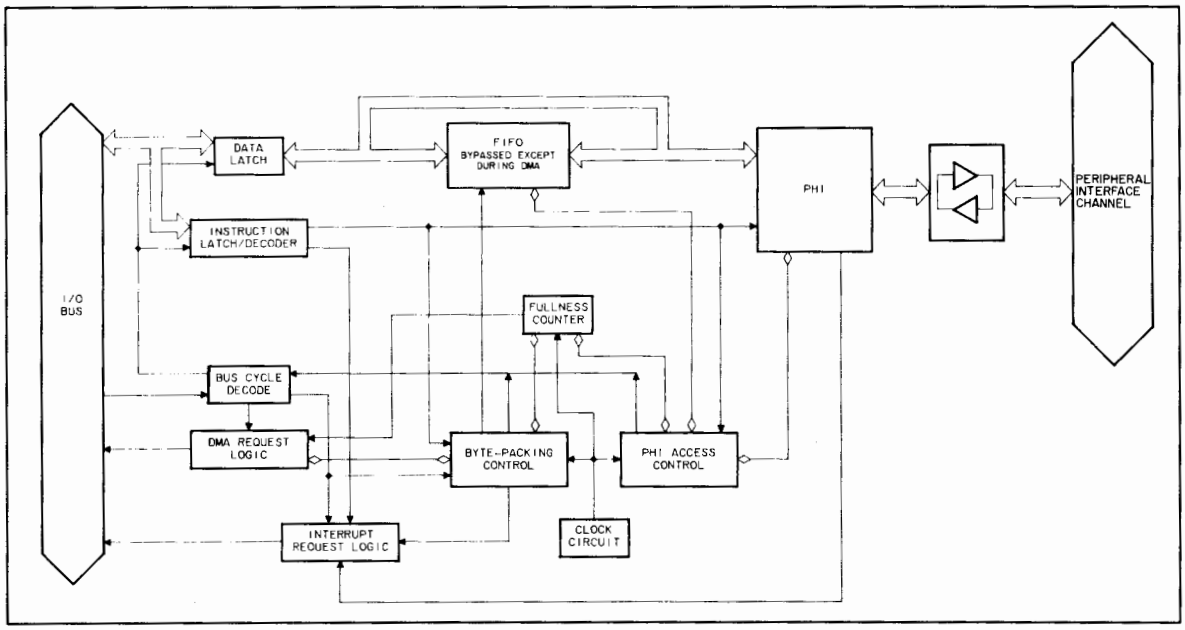


Figure 3-11: Peripheral Interface Board Block Diagram

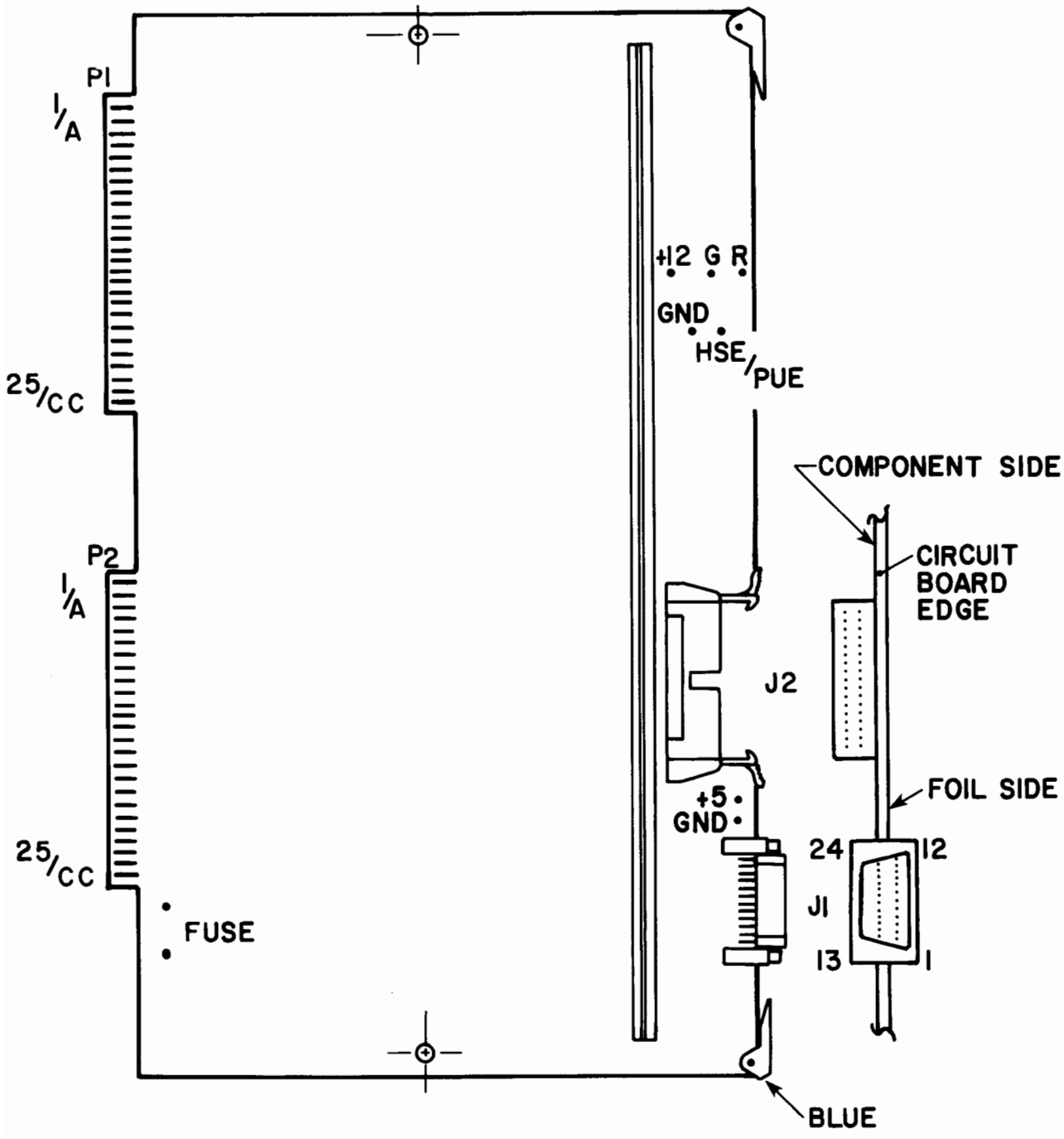


Figure 3-12: Peripheral Interface Board, A7

Table 3-6: Peripheral Interface Board Connector Signals

A7J1 Back Panel-Peripheral Interface Chnl			
Pin	Signal	Pin	Signal
1	$\overline{\text{DIO}}$ 1	13	$\overline{\text{DIO}}$ 5
2	$\overline{\text{DIO}}$ 2	14	$\overline{\text{DIO}}$ 6
3	$\overline{\text{DIO}}$ 3	15	$\overline{\text{DIO}}$ 7
4	$\overline{\text{DIO}}$ 4	16	$\overline{\text{DIO}}$ 8
5	$\overline{\text{EOI}}$	17	$\overline{\text{REN}}$
6	$\overline{\text{DAV}}$	18	
7	$\overline{\text{DRFD}}$	19	
8	$\overline{\text{NDAC}}$	20	
9	$\overline{\text{IFC}}$	21	Gnd
10	$\overline{\text{SRQ}}$	22	
11	$\overline{\text{ATN}}$	23	
12		24	

A7J2 Disc Controller Board			
Pin	Signal	Pin	Signal
1	$\overline{\text{DIO}}$ 1	2	
3	$\overline{\text{DIO}}$ 2	4	
5	$\overline{\text{DIO}}$ 3	6	
7	$\overline{\text{DIO}}$ 4	8	
9	$\overline{\text{DIO}}$ 5	10	
11	$\overline{\text{DIO}}$ 6	12	
13	$\overline{\text{DIO}}$ 7	14	
15	$\overline{\text{DIO}}$ 8	16	Gnd
17	$\overline{\text{EOI}}$	18	
19	$\overline{\text{DAV}}$	20	
21	$\overline{\text{REN}}$	22	
23	$\overline{\text{ICF}}$	24	
25	$\overline{\text{NRFD}}$	26	
27	$\overline{\text{NDAC}}$	28	
29	$\overline{\text{SRQ}}$	30	
31	$\overline{\text{ATN}}$	32	
33		34	

A7P1 Backplane			
Pin	Signal	Pin	Signal
1		A	
2	Gnd	B	Gnd
3	Gnd	C	Gnd
4		D	
5		E	
6		F	
7		H	
8		J	
9		K	
10		L	
11		M	
12	$\overline{\text{IOD}}$ 6	N	$\overline{\text{IOD}}$ 7
13	$\overline{\text{IOD}}$ 4	P	$\overline{\text{IOD}}$ 5
14	$\overline{\text{IOD}}$ 2	R	$\overline{\text{IOD}}$ 3
15	$\overline{\text{IOD}}$ Ø	S	$\overline{\text{IOD}}$ 1
16	$\overline{\text{IOD}}$ 14	T	$\overline{\text{IOD}}$ 15
17	$\overline{\text{IOD}}$ 12	U	$\overline{\text{IOD}}$ 13
18	$\overline{\text{IOD}}$ 10	V	$\overline{\text{IOD}}$ 11
19	$\overline{\text{IOD}}$ 8	W	$\overline{\text{IOD}}$ 9
20		X	
21		Y	
22		Z	
23		AA	
24		BB	
25	+12V	CC	+12V

A7P2 Backplane			
Pin	Signal	Pin	Signal
1	+12V	A	+12V
2		B	
3		C	
4		D	
5		E	$\overline{\text{IRL}}$
6	$\overline{\text{DMAR}}$	F	
7		H	$\overline{\text{FLG}}$
8	$\overline{\text{STS}}$	J	
9		K	
10		L	
11		M	
12		N	$\overline{\text{PA2}}$
13		P	$\overline{\text{PA}}$Ø
14	$\overline{\text{PA1}}$	R	$\overline{\text{IOSB}}$
15		S	
16	$\overline{\text{DOUT}}$	T	$\overline{\text{IC2}}$
17	$\overline{\text{IC1}}$	U	
18		V	
19	$\overline{\text{PA3}}$	W	$\overline{\text{INT}}$
20		X	
21		Y	$\overline{\text{POP}}$
22	Gnd	Z	Gnd
23	Gnd	AA	Gnd
24	+5V	BB	+5V
25	+5V	CC	+5V

Chart 3-5: Peripheral Interface Board Test Points

-Name-	-Description-	
+5	+5 volts;	spec: +5, + or - 3% range: 4.85V to 5.15V
+12	+12 volts;	spec: +12, + or - 5% range: 11.64V to 12.36V
G	common (ground)	
GND	common (ground)	
R	Delay Stablization (no longer used)	
HSE/PUE	not used	

Keyboard Logic and Matrix Board, A8 and A9

The Keyboard Logic Board, Keyboard Matrix Board, Soft-Key Assembly, and associated cables form the HP 250 Keyboard subsystem. The subsystem communicates with the main system via the I/O bus of the system processor. The keyboard is low-level interrupt device and has peripheral address 6 (PA6).

The Keyboard subsystem provides three major functions to the HP 250 system. These functions are described in the following paragraphs.

1. Detect when any of the main keyboard keys or softkeys have been press, encode the key information, interrupt the main system processor (via the I/O buss), and present the keycode(s) to the processor on the I/O bus when instructed to do so by the processor.

2. Serve as a buffer between the typist and the main system processor. This is accomplished through the use of a 64 characttter FIFO buffer.

3. A user-alert bell circuit is incorporated on the keyboard for the purpose of allowing the main system processor to alert the operator of a particular condition defined by software. This is accomplished with the implementation of a "beeper" circuit which emits a 100 ms, 700Hz audio tone burst under command of the system processor.

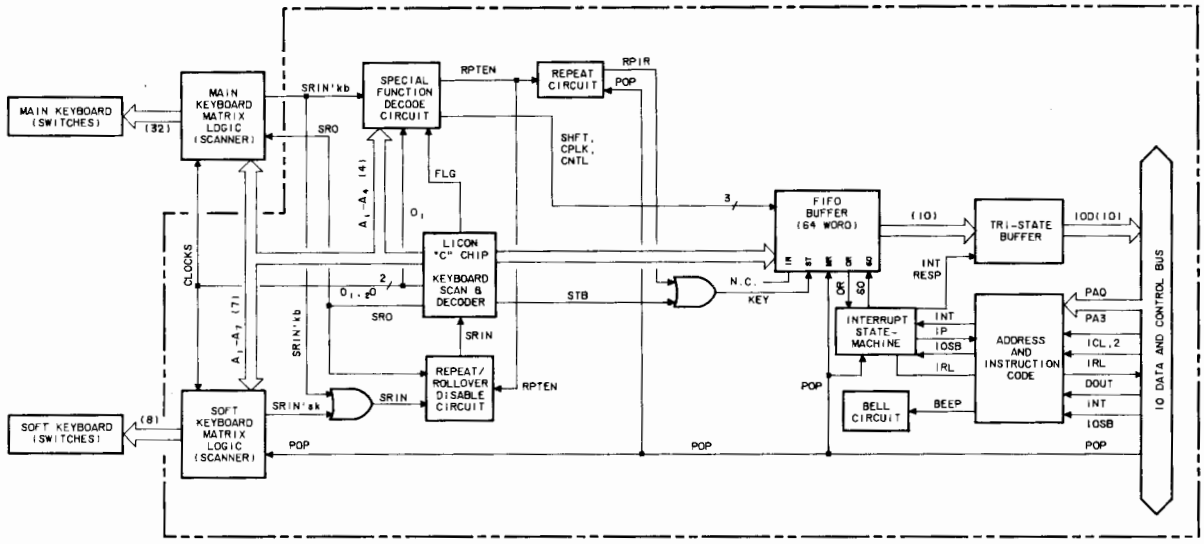


Figure 3-13: Keyboard Logic Board Block Diagram

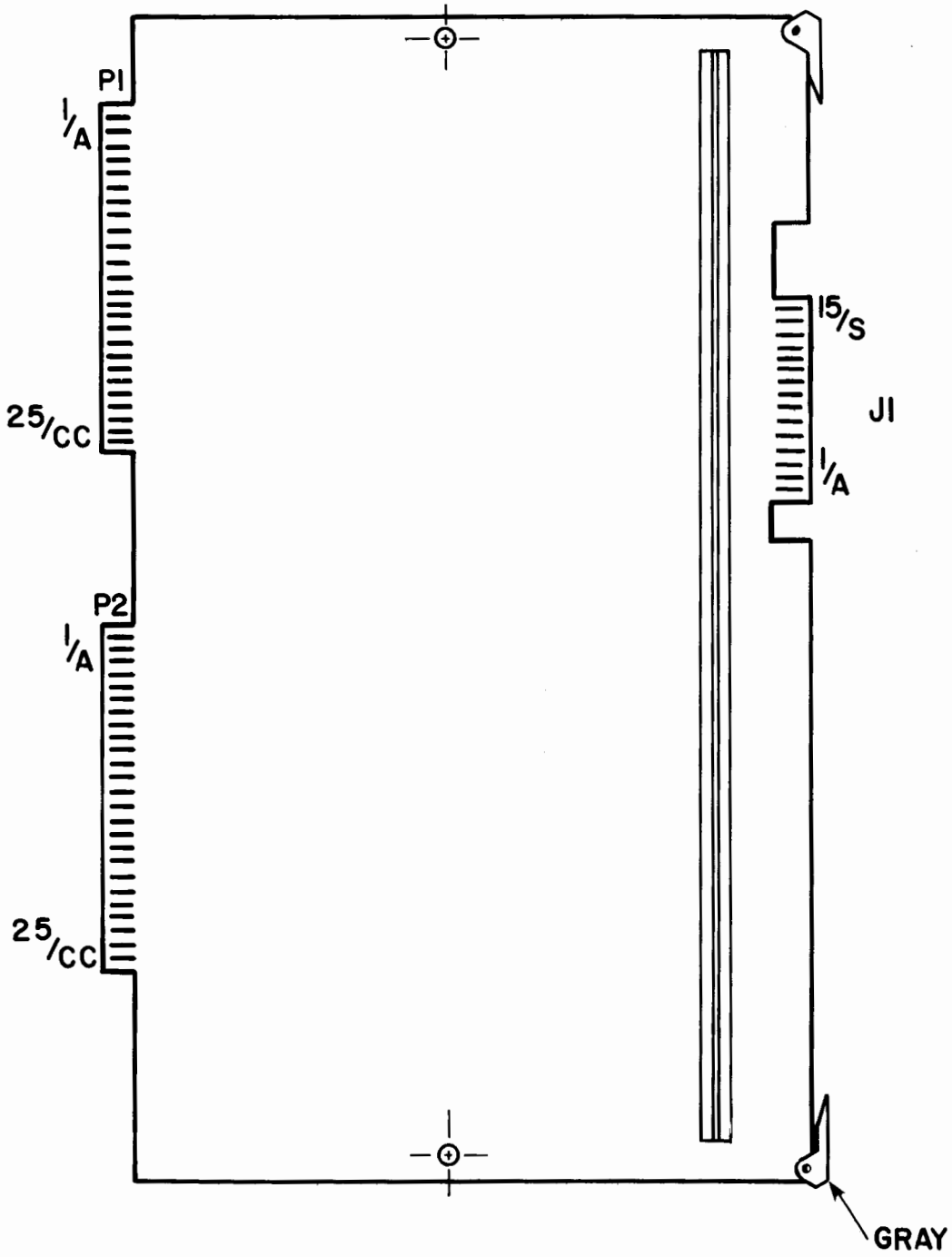


Figure 3-14: Keyboard Logic Board, A8

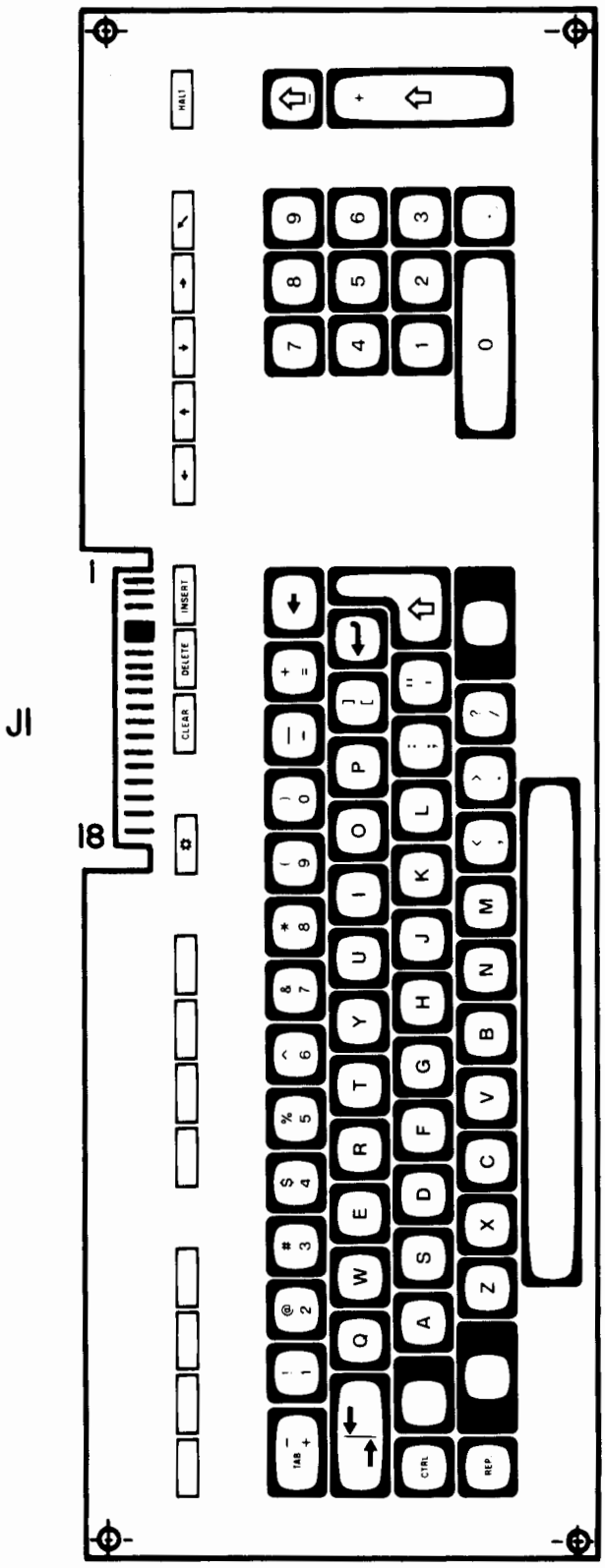


Figure 3-15: Keyboard Matrix Board, A9

Table 3-7: Keyboard Logic Board Connector Signals

A8P1 Backplane			
Pin	Signal	Pin	Signal
1		A	
2	Gnd	B	Gnd
3	Gnd	C	Gnd
4		D	
5		E	
6		F	
7		H	
8		J	
9		K	
10		L	
11		M	
12	$\overline{IOD}$ 6	N	
13	$\overline{IOD}$ 4	P	$\overline{IOD}$ 5
14	$\overline{IOD}$ 2	R	$\overline{IOD}$ 3
15	$\overline{IOD}$ Ø	S	$\overline{IOD}$ 1
16	$\overline{IOD}$ 14	T	$\overline{IOD}$ 15
17		U	$\overline{IOD}$ 13
18		V	
19		W	
20		X	
21		Y	
22		Z	
23		AA	
24		BB	
25		CC	

A8P2 Backplane			
Pin	Signal	Pin	Signal
1	+12V	A	+12V
2	-12V	B	-12V
3		C	
4	$\overline{IRH}$	D	
5		E	$\overline{IRL}$
6		F	
7		H	
8		J	
9		K	
10	$\overline{RFC}$	L	
11		M	
12		N	$\overline{PA2}$
13		P	$\overline{PAØ}$
14	$\overline{PA1}$	R	$\overline{IOSB}$
15		S	
16	$\overline{DOUT}$	T	$\overline{IC2}$
17	$\overline{IC1}$	U	
18		V	
19	$\overline{PA3}$	W	$\overline{INIT}$
20		X	
21		Y	$\overline{POP}$
22	Gnd	Z	Gnd
23	Gnd	AA	Gnd
24	+5V	BB	+5V
25	+5V	CC	+5V

A8J1 Keyboard Matrix & Softkeys			
Pin	Signal	Pin	Signal
1	$\overline{S7}$	A	$\overline{S6}$
2	$\overline{S5}$	B	$\overline{S4}$
3	$\overline{S3}$	C	$\overline{S2}$
4	$\overline{S1}$	D	$\overline{SØ}$
5	Gnd	E	Spkr
6	+12V	F	-12V
7	Gnd	H	Gnd
8	+5V	J	+5V
9	$\overline{SRIN}$	K	$\overline{SRO}$
10	Ø1	L	Ø3
11	Gnd	M	Gnd
12	$\overline{A2Ø1}$	N	$\overline{A4Ø1}$
13	$\overline{A1}$	P	$\overline{A2}$
14	$\overline{A3}$	R	$\overline{A5}$
15	$\overline{A6}$	S	$\overline{A7}$

Table 3-8: Keyboard Matrix Board Connector Signals

A9J1 Keyboard Logic Board	
Pin	Signal
1	-12V
2	Gnd
3	Gnd
4	+5V
5	+5V
6	$\overline{A7}$
7	$\overline{SRO}$
8	$\overline{A6}$
9	$\overline{A5}$
10	$\overline{SRIN}$
11	$\Phi 3$
12	$\overline{\Phi 1}$
13	$\overline{A2}$
14	$\overline{A3}$
15	$\overline{A4\Phi 2}$
16	Gnd
17	$\overline{A4\Phi 1}$
18	$\overline{A1}$

Disc Controller Board, A10

The Disc Controller Board circuits provide an interface between the Peripheral Interface (HP-IB) and up to three 1.2 Mbyte drives. Commands are accepted from the interface channel and interpreted to provide the proper operating sequences for the selected disc drive. This includes providing control and timing signals, sending data to the disc drive, receiving data from the disc drive, and handling all input/output communications.

The controller can be broken down in eight major sections. They are the Peripheral Interface , processor, multiplexer, control logic, write encoder, and I/O.

NOTE

The Soft Logic Processor of the controller communicates with the System Processor via the Peripheral Interface Channel, and only requires DC power and the POP signal from the mother board.

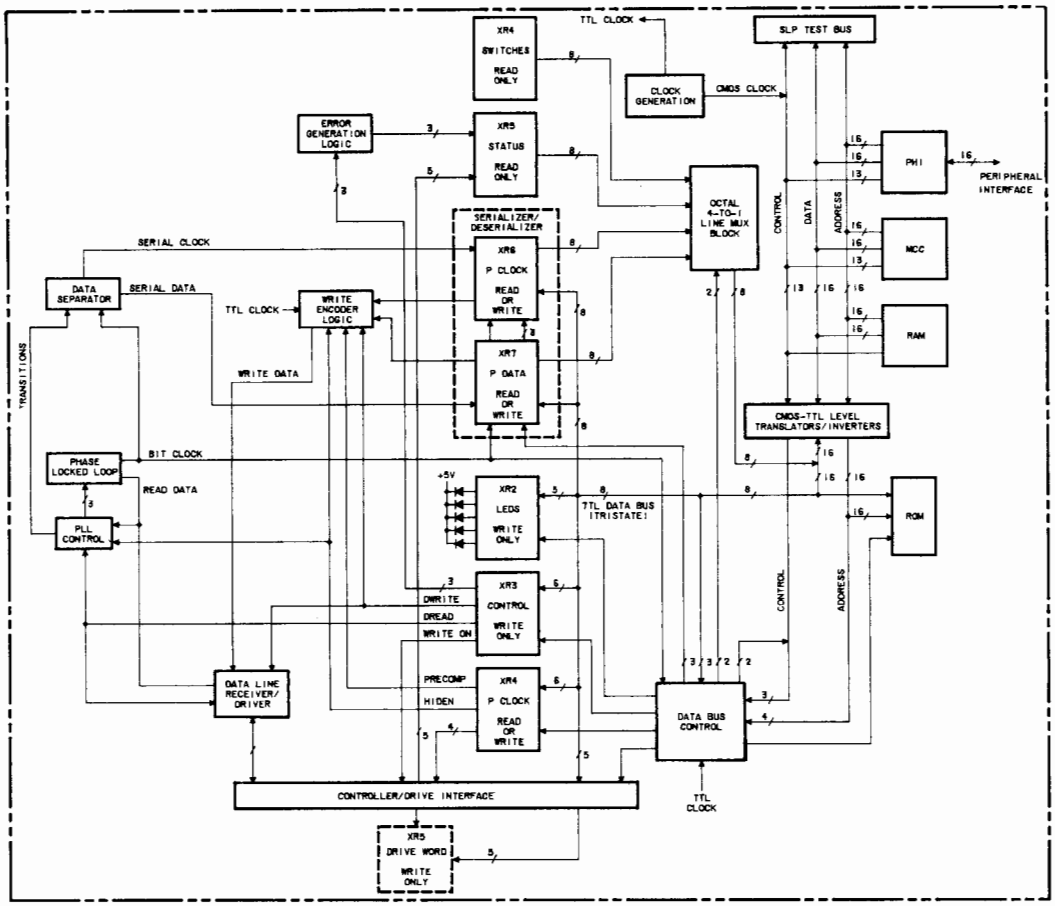


Figure 3-16: Disc Controller Board Block Diagram

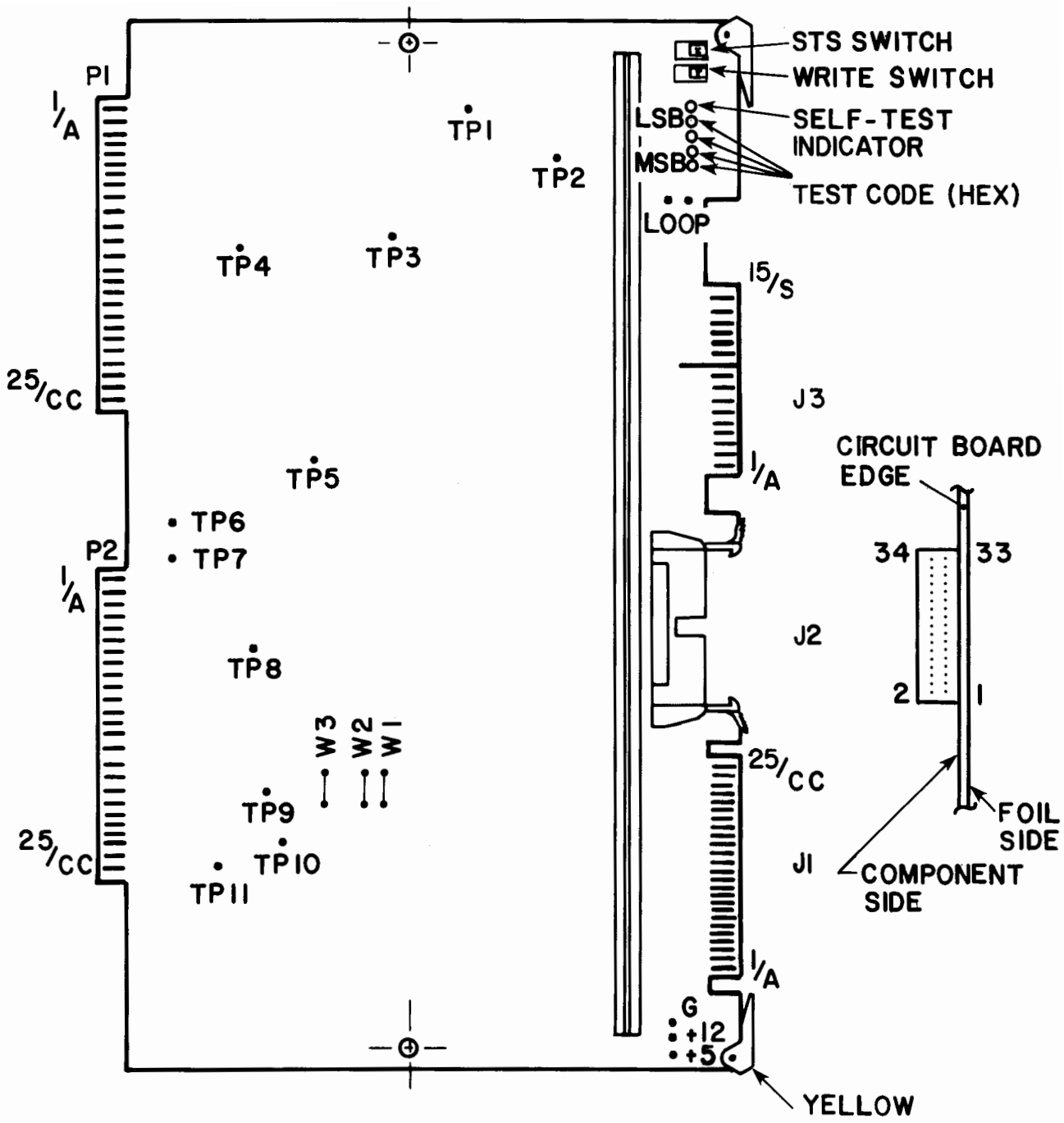


Figure 3-17: Disc Controller Board, A10

Table 3-9: Disc Controller Board Connector Signals

A1ØP1 Backplane

Pin	Signal	Pin	Signal
1		A	
2		B	
3		C	
4		D	
5		E	
6		F	
7		H	
8		J	
9		K	
10		L	
11		M	
12		N	
13		P	
14		R	
15		S	
16		T	
17		U	
18		V	
19		W	
20		X	
21		Y	
22		Z	
23		AA	
24	-5V	BB	-5V
25	+12V	CC	+12V

A1ØP2 Backplane

Pin	Signal	Pin	Signal
1	+12V	A	+12V
2		B	
3		C	
4		D	
5		E	
6		F	
7		H	
8		J	
9		K	
10		L	
11		M	
12		N	
13		P	
14		R	
15		S	
16		T	
17		U	
18		V	
19		W	
20		X	
21		Y	$\overline{\text{POP}}$
22	Gnd	Z	Gnd
23	Gnd	AA	Gnd
24	+5V	BB	+5V
25	+5V	CC	+5V

A1ØJ1 Test Jack

Pin	Signal	Pin	Signal
1	Gnd	A	CWRITE
2	CFETCH	B	CPON
3	$\overline{\text{CINT}}$	C	CIAK
4		D	CGNI
5	$\overline{\text{CIOGO}}$	E	$\overline{\text{CIOEND}}$
6	$\overline{\text{CMGO}}$	F	$\overline{\text{CMEND}}$
7	Gnd	H	$\overline{\text{CIDLE}}$
8	CA14	J	CA15
9	CA12	K	CA13
10	CA1Ø	L	CA11
11	CA8	M	CA9
12	CA6	N	CA7
13	CA4	P	CA5
14	CA2	R	CA3
15	CAØ	S	CA1
16	Gnd	T	Gnd
17	CD1	U	CDØ
18	CD3	V	CD2
19	CD5	W	CD4
20	CD7	X	CD6
21	CD9	Y	CD8
22	CD11	Z	CD1Ø
23	CD13	AA	CD12
24	CD15	BB	CD14
25	$\overline{\text{CLK250}}$	CC	Gnd

A1ØJ2 Peripheral Interface Bd

Pin	Signal	Pin	Signal
1	Gnd	18	$\overline{\text{EOI}}$
2		19	Gnd
3	Gnd	20	$\overline{\text{DIO8}}$
4	$\overline{\text{ATN}}$	21	Gnd
5	Gnd	22	$\overline{\text{DIO7}}$
6	$\overline{\text{SRQ}}$	23	Gnd
7	Gnd	24	$\overline{\text{DIO6}}$
8	$\overline{\text{NDAC}}$	25	Gnd
9	Gnd	26	$\overline{\text{DIO5}}$
10	$\overline{\text{NRFD}}$	27	Gnd
11	Gnd	28	$\overline{\text{DIO4}}$
12	$\overline{\text{IFC}}$	29	Gnd
13	Gnd	30	$\overline{\text{DIO3}}$
14	$\overline{\text{REN}}$	31	Gnd
15	Gnd	32	$\overline{\text{DIO2}}$
16	$\overline{\text{DAV}}$	33	Gnd
17	Gnd	34	$\overline{\text{DIO1}}$

A1ØJ3 Disc Drive Board

Pin	Signal	Pin	Signal
1	LWPRT	A	POP
2	HREDY	B	LTRKØ
3	LSPIN	C	
4	LINDX	D	HRSPIN
5	LDRLK	E	
6	STPHA	F	LSTEN
7	LWRITON	H	
8	STPHB	J	LDSLV
9	HHED1	K	
10	LLDCT	L	HDSL2
11	HDSL1	M	
12	HDSLØ	N	PONR
13		P	
14		R	
15	HDATA	S	LDATA

Chart 3-6: Disc Controller Board Test Points and Jumpers

-Name-	-Description-
LOOP	The two LOOP pins are tied together to repeat portions of the Disc Controller Self-Test. See Disc Controller Self-Test in Chapter 5.
G	Common (ground)
+12	+12 volts: Spec= +12, + or - 3% Range= 11.64V to 12.36V
+5	+5 volts: Spec= +5, + or - 3% Range= 4.85V to 5.15V

Chart 3-7: Disc Controller Board Controls and Indicators

-Name-	-Description-	-Adjustment Procedure-
STS Switch	Self-Test Switch used to initiate all Disc Controller self-test routines.	See Disc Controller Self-Test in Chapter 5.
WRITE Switch	Used to enter special sub-routines to be performed in addition to the normal self-test.	See Disc Controller Self-Test in Chapter 5.
Self-Test Indicator	When this LED is is lit, the disc controller and drive are being controlled by the Controller Self-Test routine. The LED should be off anytime the disc and controller are on-line.	
Test-Code Indicator	This is a four bit code (LSB on top) which when com-combined with the Self-Test Indicator shows the status of the self-test routine.	See Disc Controller Self-Test in Chapter 5 for more details on the indicator and the codes.

Power Supply Board, A11

The outputs of the HP 250 Power Supply consist of six different regulated supplies, one unregulated supply, and a power-on-pulse (POP). These outputs and their specifictions are given in Chart 3-8: Power Supply Board Test-Points.

The power supply has several protection features to prevent damage to itself or to its load in case of faulty operation or incorrect electrical connections. Current limit protection is provided for all regulated supplies. Overvoltage and reverse polarity protection are provided on all but the VREG supply. All negative supplies and the +7V supply are provided thermal protection by shutting down i in case of overheating.

Another feature for the protection of the load is an automatic shutdown of the positive regulators whenever the -5V supply rises above about -3V. This protects any MOS circuits which use -5V as a back-bias supply.

NOTE

If the power supply shuts itself off, it will remain off until the power is turned off and then on again.

A 10k ohm resistor is connected between each test point and the circuit board edge connector. This provides protection against inadvertant shorts triggering any of the protection circuits while probing.

There are three small support circuits on the power supply which provide an auxillary supply, a 23 khz clock, and a +5.4 volt reference.

The auxillary supply is a +9.3 volt supply used to supplying power to the oscillator and the reference.

The clock circuit consists of a square wave oscillator, an integrator for converting to a triangle wave, and an inverter for generating an inverted phase of the clock.

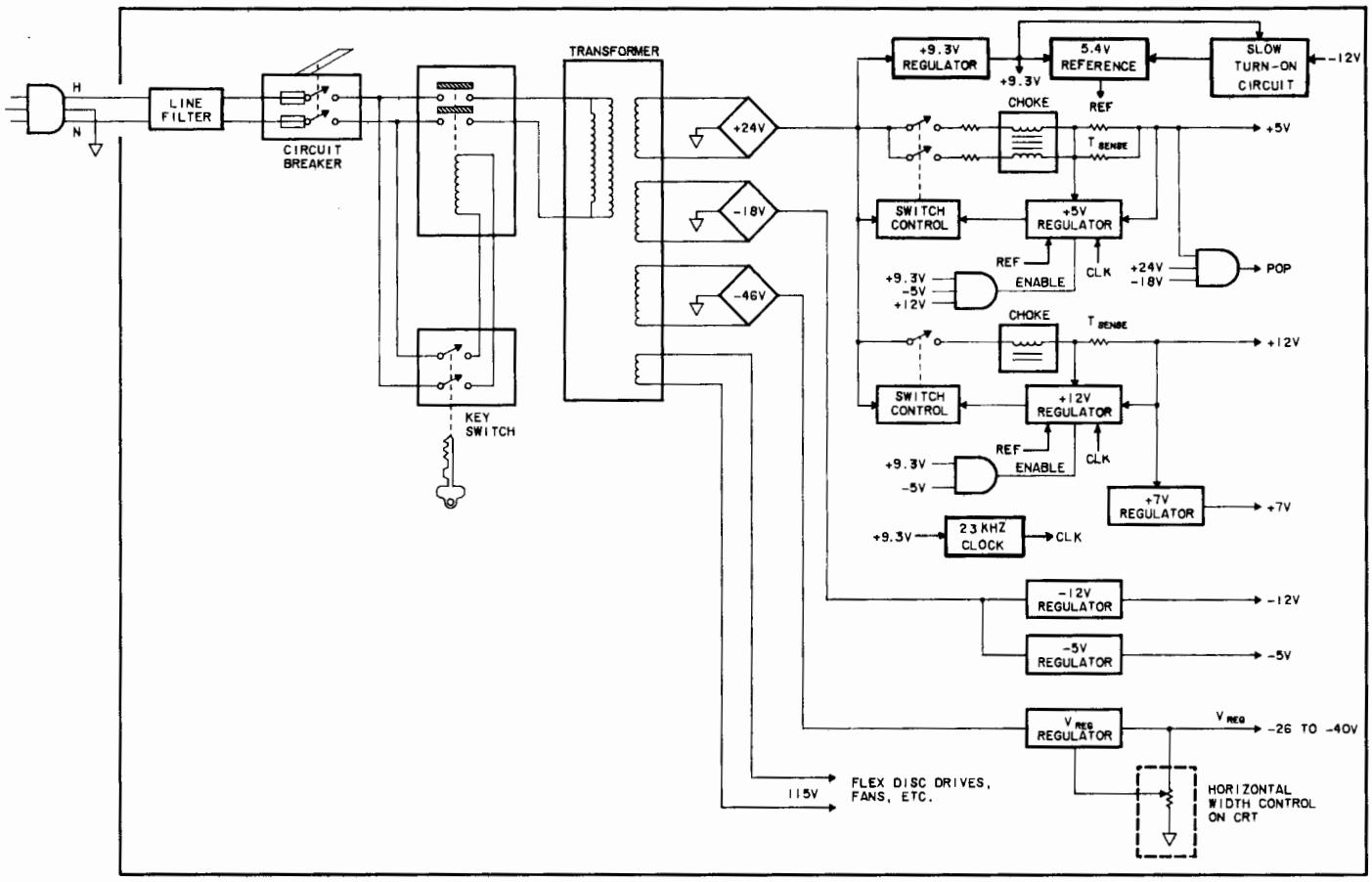


Figure 3-18: Power Supply Board Block Diagram

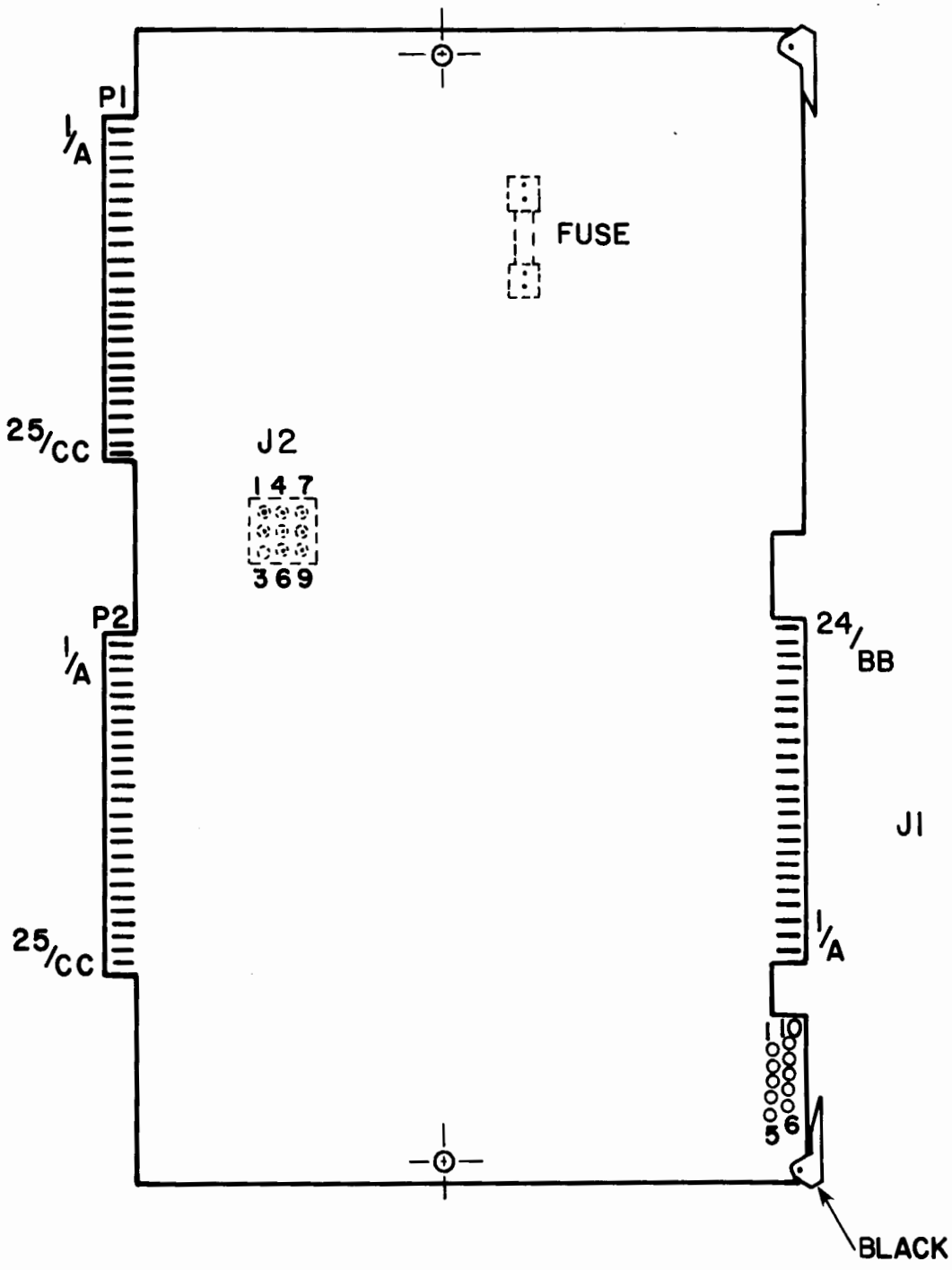


Figure 3-19: Power Supply Board, A11

Table 3-10: Power Supply Board Connector Signals

A11P1 Backplane			
Pin	Signal	Pin	Signal
1		A	
2		B	
3		C	
4		D	
5	+5V	E	+5V
6		F	
7		H	
8		J	
9		K	
10		L	
11		M	
12		N	
13		P	$\overline{POP}$
14		R	
15		S	
16		T	
17	Gnd	U	Gnd
18		V	
19		W	
20		X	
21		Y	
22		Z	
23		AA	
24	-12V	BB	-12V
25		CC	

A11P2 Backplane			
Pin	Signal	Pin	Signal
1		A	
2		B	
3		C	
4	+12V	D	+12V
5		E	
6		F	
7		H	
8		J	
9	-5V	K	-5V
10		L	
11		M	
12		N	
13		P	
14		R	
15		S	
16		T	
17	Gnd	U	Gnd
18		V	
19		W	
20		X	
21		Y	
22		Z	
23		AA	
24	+7V	BB	+7V
25		CC	

A11J1 - CRT and PWR XFMR			
Pin	Signal	Pin	Signal
1	24VAC	A	24VAC
2		B	
3	24VAC	C	24VAC
4		D	
5	18VAC	E	18VAC
6	18VAC	F	18VAC
7		H	
8	46VAC	J	46VAC
9		K	
10	46VAC	L	46VAC
11		M	
12	VREG	N	VREG
13		P	
14	VSENSE	R	VSENSE
15		S	
16	-12V	T	-12V
17	+12V	U	+12V
18	+5V	V	+5V
19	Gnd	W	Gnd
20		X	
21		Y	
22		Z	
23		AA	
24		BB	

A11J2 DC Power Bus			
Pin	Signal	Pin	Signal
1	+5V(3)	6	Gnd(0)
2	Gnd(0)	7	+5V(3)
3	+24V(2)	8	Gnd(0)
4	+5V(3)	9	-5V(6)
5	Gnd(0)		

(#) - wire color using resistor color code

* A11J1 ac pin are connected to their complement. For example: pin 8 is connected to pin J and pins 1 & 2 are connected to A & B

Chart 3-8: Power Supply Board Test-Points

-Name-	-Description-
TP1	GND: common (ground)
TP2	+12V: +12 volts; spec= +12, + or - 3% range= 11.64V to 12.36V
TP3	-5V: -5 volts; spec= -5, + or - 5% range= -4.75V to -5.25V
TP4	VSENSE: represents a current source to the Width adjustment on the CRT Board. Depending on the setting of the width adjustment, the voltage at TP4 will be between -12V and -28V.
TP5	+24V: this is a +24 volt unregulated supply.
TP6	VREG: -26 volts to -40 volts; depends on the position of the CRT Board Width Adjustment
TP7	-12V: -12 volts; spec= -12, + or - 5% range= -11.4V to -12.6V
TP8	+7V: +7 volts; spce= +7, + or - 5% range= 6.65V to 7.35V
TP9	+5V: +5 volts; spec= +5, + or - 3% range= 4.85V to 5.15V
TP10	POP: a negative pulse which occurs at power-up and when the POP Switch on the Processor Board is pressed.

Memory Board, A13 and A23

The 64 kbyte Memory Board is separated into two 16 kbyte memory blocks. (The 32 kbyte Memory Board is a single block.) The board can be used to select two separate and distinct 16 kbyte memory blocks by using the Memory Board Block Select Switches located on the board. The 64 kbyte board has two switches and the 16 kbyte board has one. See System Configuration in Chapter 2 for details in setting the Block Select Switches.

The Memory Board responds to the two address selected by the switches, and performs either a read or a write cycle as directed by the processor control signals. The Memory Board also has the timing to refresh all of the memory chips on the board every 1.7 ms.

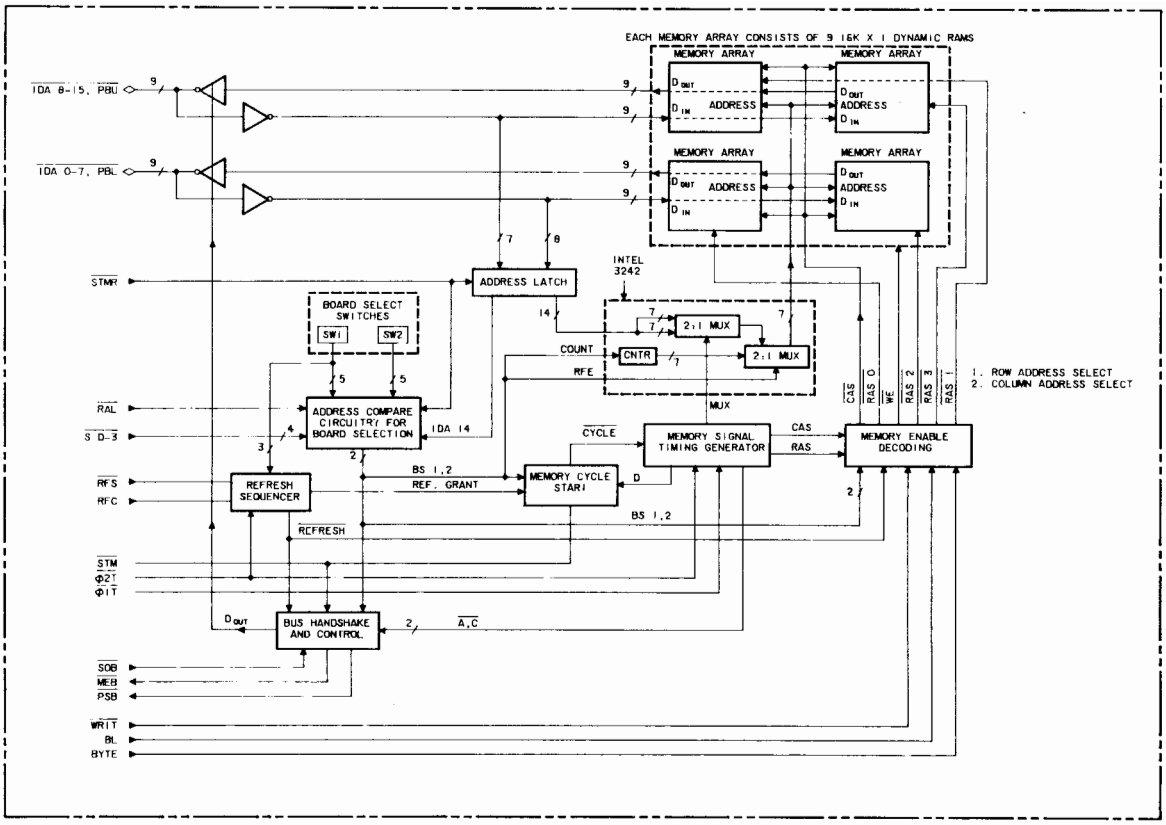
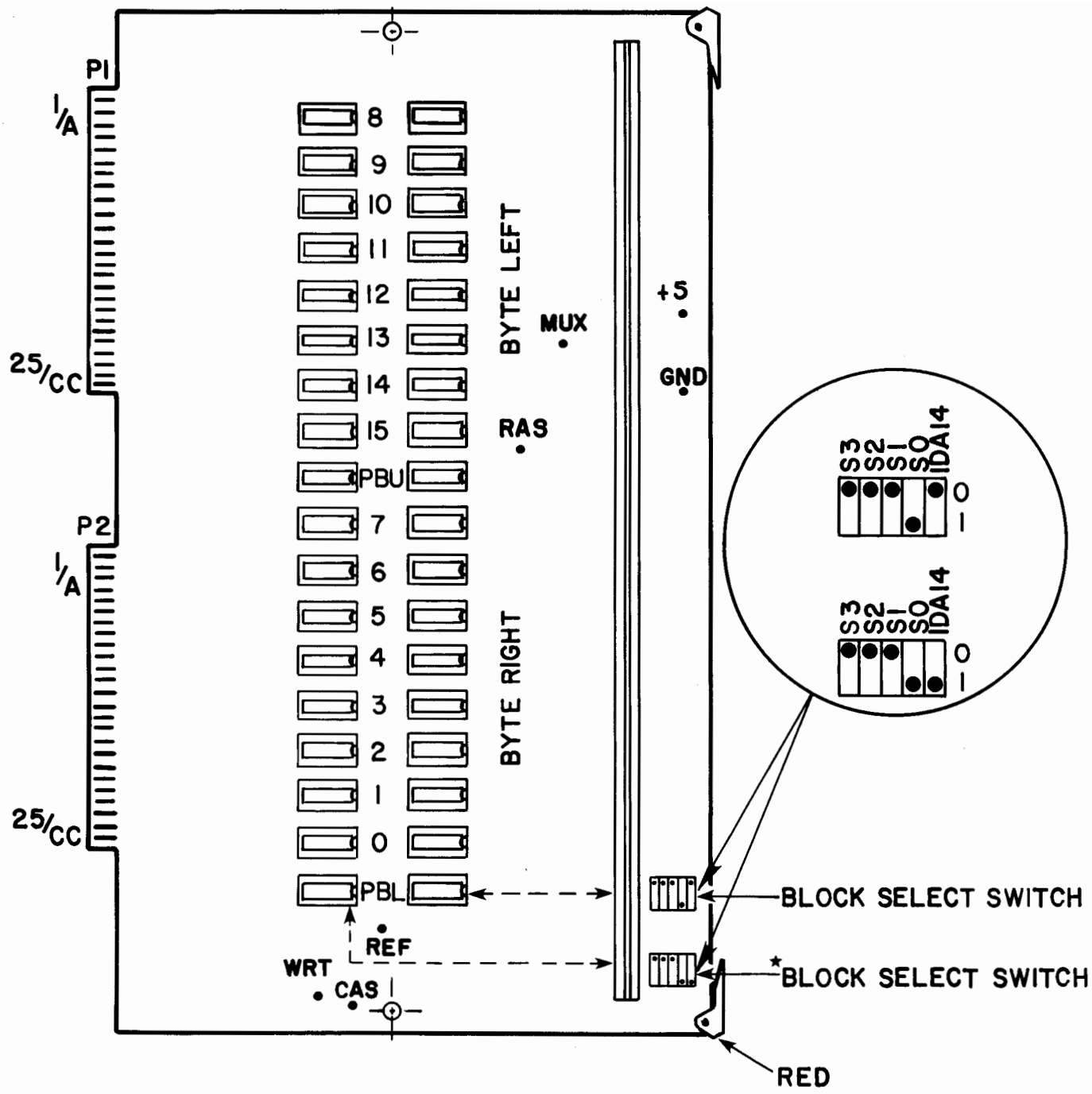


Figure 3-20: Memory Board Block Diagram



*This switch is used only on 64 kbyte Memory Boards

Figure 3-21: Memory Board, A13 and A23

Table 3-11: Memory Board (A13 and A23) Connector Signals

A13P1/A23P1 Backplane			
Pin	Signal	Pin	Signal
1		A	
2	Gnd	B	Gnd
3	Gnd	C	Gnd
4	$\overline{IDA14}$	D	$\overline{IDA15}$
5	$\overline{IDA12}$	E	$\overline{IDA13}$
6	$\overline{IDA1Ø}$	F	$\overline{IDA11}$
7	$\overline{IDA8}$	H	$\overline{IDA9}$
8	$\overline{IDA6}$	J	$\overline{IDA7}$
9	$\overline{IDA4}$	K	$\overline{IDA5}$
10	$\overline{IDA2}$	L	$\overline{IDA3}$
11	$\overline{IDAØ}$	M	$\overline{IDA1}$
12		N	
13		P	
14		R	
15		S	
16		T	
17		U	
18		V	
19		W	
20		X	
21	$\overline{MEB}$	Y	
22	$\overline{STM}$	Z	
23	Gnd	AA	Gnd
24	-5V	BB	-5V
25	+12V	CC	+12V

A13P2/A23P2 Backplane			
Pin	Signal	Pin	Signal
1	+12V	A	+12V
2		B	
3	Gnd	C	Gnd
4		D	SØ
5	S1	E	
6		F	S2
7	S3	H	
8		J	
9	BYTE	K	BL
10	RFC	L	$\overline{RFS}$
11	Ø1	M	$\overline{SOB}$
12	$\overline{WRT}$	N	
13	PSB	P	
14		R	
15	$\overline{STMR}$	S	$\overline{RAL}$
16		T	
17		U	Ø2
18	$\overline{PBL}$	V	$\overline{PBU}$
19		W	
20		X	
21		Y	
22	Gnd	Z	Gnd
23	Gnd	AA	Gnd
24	+5V	BB	+5V
25	+5V	CC	+5V

Block Switch Board, A14

The major purpose of the Block Switch Board is to allow the system to address more than 64 kwords of memory. The block switch can address a maximum of sixteen 32k memory boards; however, in actual operation this is not practical due to a physical limitation on the number of slots in the card-cage and power supply current limitations.

The Block Switch Board contains its own instruction decoder to route, fetch, execute, and DMA information to the proper memory block. It also has registers that allow protection of two 64 kbyte boards for Operating System use. An interrupt is generated if this area is violated.

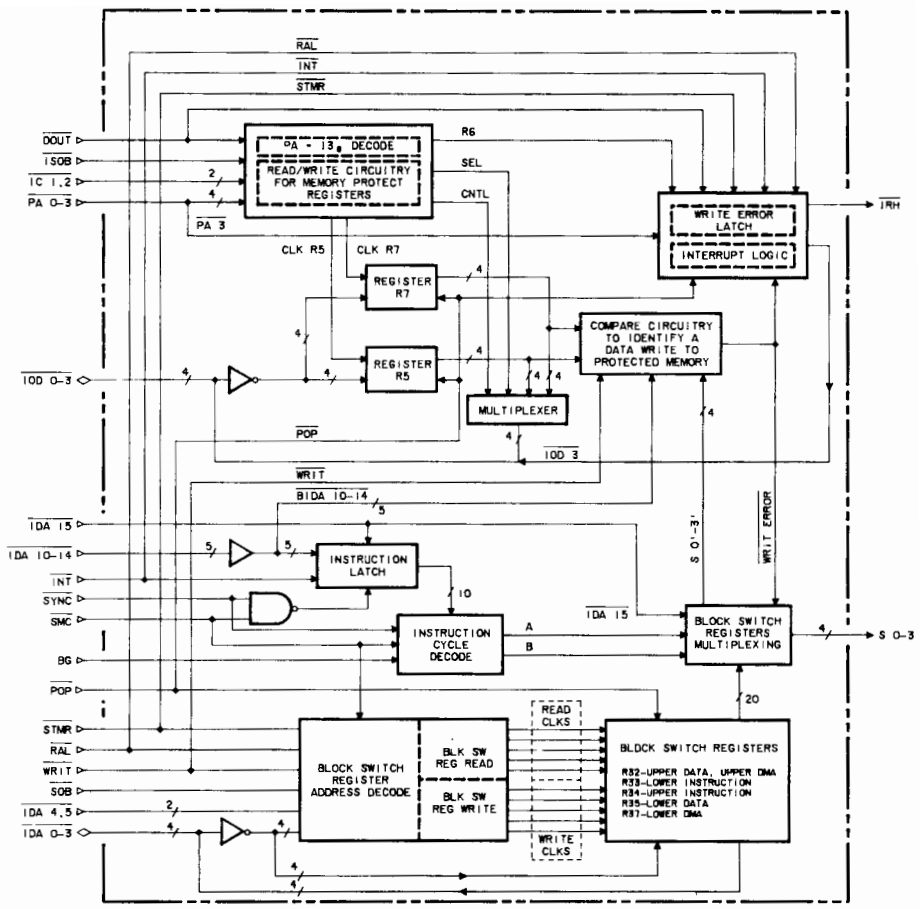


Figure 3-22: Block Switch Board Block Diagram

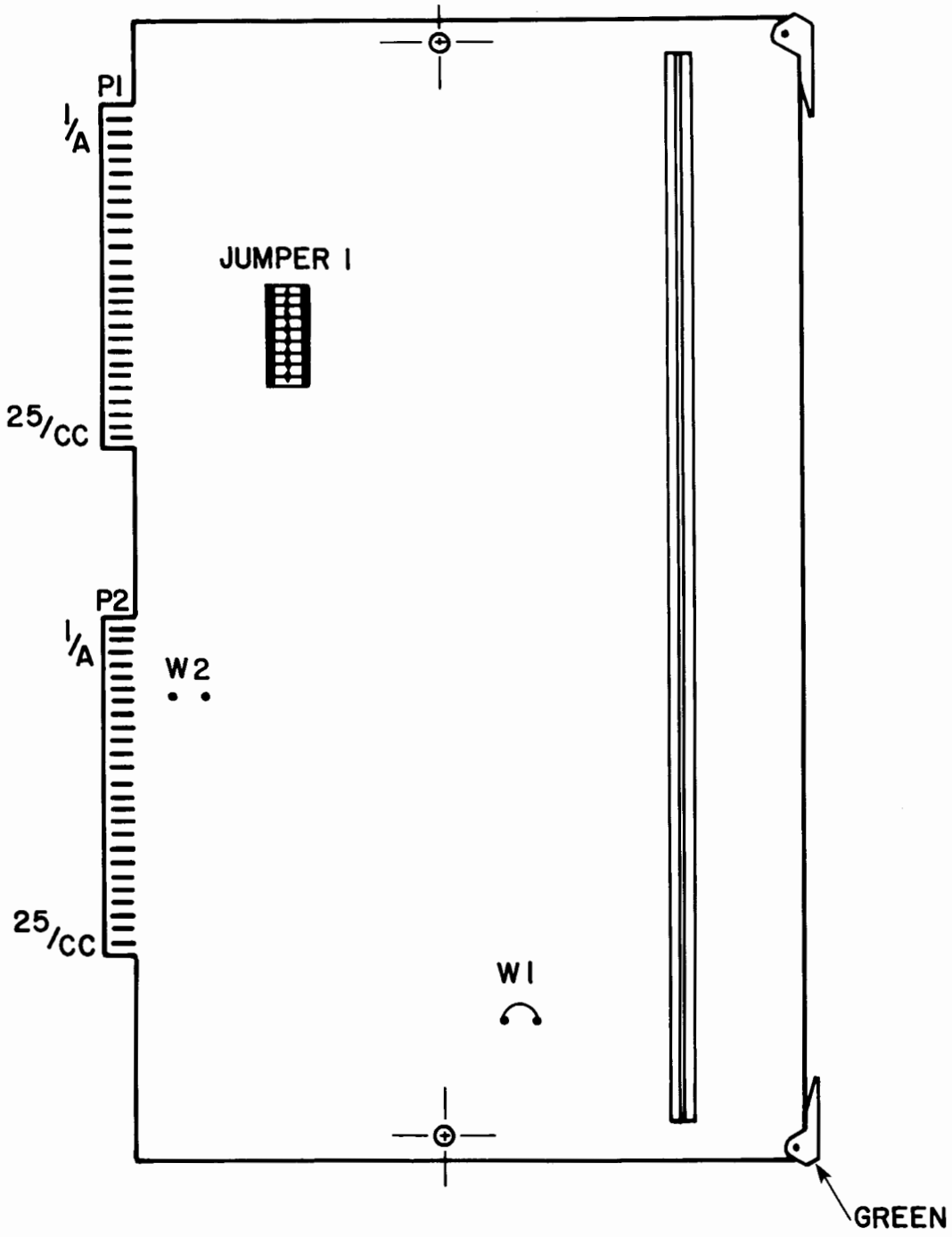


Figure 3-23: Block Switch Board, A14

Table 3-12: Block Switch Board (A14) Connector Signals

A14P1 Backplane			
Pin	Signal	Pin	Signal
1		A	
2	Gnd	B	Gnd
3	Gnd	C	Gnd
4		D	
5	$\overline{\text{IDA11}}$	E	$\overline{\text{IDA10}}$
6	$\overline{\text{IDA13}}$	F	$\overline{\text{IDA12}}$
7	$\overline{\text{IDA14}}$	H	$\overline{\text{IDA14}}$
8		J	
9	$\overline{\text{IDA4}}$	K	$\overline{\text{IDA5}}$
10	$\overline{\text{IDA2}}$	L	$\overline{\text{IDA3}}$
11	$\overline{\text{IDA0}}$	M	$\overline{\text{IDA1}}$
12		N	
13		P	
14	$\overline{\text{IDA2}}$	R	$\overline{\text{IOD3}}$
15	$\overline{\text{IOD0}}$	S	$\overline{\text{IOD1}}$
16		T	
17		U	
18		V	
19		W	
20	$\overline{\text{SYNC}}$	X	BG
21		Y	$\overline{\text{SMC}}$
22		Z	
23		AA	
24		BB	
25		CC	

A14P2 Backplane			
Pin	Signal	Pin	Signal
1		A	
2		B	
3	Gnd	C	Gnd
4	$\overline{\text{IRH}}$	D	
5	S1	E	
6		F	S2
7	S3	H	
8		J	
9		K	
10		L	
11		M	$\overline{\text{SOB}}$
12	$\overline{\text{WRIT}}$	N	$\overline{\text{PA2}}$
13		P	$\overline{\text{PA0}}$
14	$\overline{\text{PA1}}$	R	$\overline{\text{IOSB}}$
15	$\overline{\text{STMR}}$	S	$\overline{\text{RAL}}$
16	$\overline{\text{DOUT}}$	T	$\overline{\text{IC2}}$
17	$\overline{\text{IC1}}$	U	
18		V	
19	$\overline{\text{PA3}}$	W	$\overline{\text{INT}}$
20		X	
21	$\overline{\text{BSI}}$	Y	$\overline{\text{POP}}$
22	Gnd	Z	Gnd
23	Gnd	AA	Gnd
24	+5V	BB	+5V
25	+5V	CC	+5V

Disc Drive Board, A25

The following paragraphs explain functional areas of the Disc Drive board as shown in Figure 3-24: Disc Drive Board Block Diagram.

The Stepper Motor drive consists of four drivers controlled by STPHA and STPHB from the Controller Board. The controller is responsible to ensure that data is not read or written while the stepper motor is moving the heads.

The Drive Select circuit decodes HDSL1, HDSL2, and LDSLV by using the position of the Drive Select Switch to determine when the drive is to be activated.

The Control Register Decoder decodes the input signals to the stepper motor and holds these signals until a change is received.

The Read/Write select determines when the drive is to perform a read or write operation.

The Drive Ready Detector circuits combines RSPIN from the controller, signals from the Control Register Decoder, and the Status Detector and uses them to control the IN USE and READY lights. It also outputs a REDY signal to the controller.

The Status Detector determines when the write protect, track 0 detect, and index pulse signals are active. This information is then fed to the controller.

The Head Select Circuit determines whether head 0 or head 1 is to be accessed.

The Erase Current Source provides a DC current to the erase heads when WRITE is selected. The erase heads then erase a path on each side of the write area. This ensures that during READ, there will be no stray signals outside the track thereby improving the signal-to-noise ratio.

The Line Driver and Receiver acts as an interface between the controller and the read and write sections.

The Write Current Source provides the required current to the heads during a WRITE operation. The head selected to write is the only one which will draw current from the source.

The Read Amplifier and Shaper takes the low-level signal from the heads and converts it to a digital signal before sending it to the Line Driver.

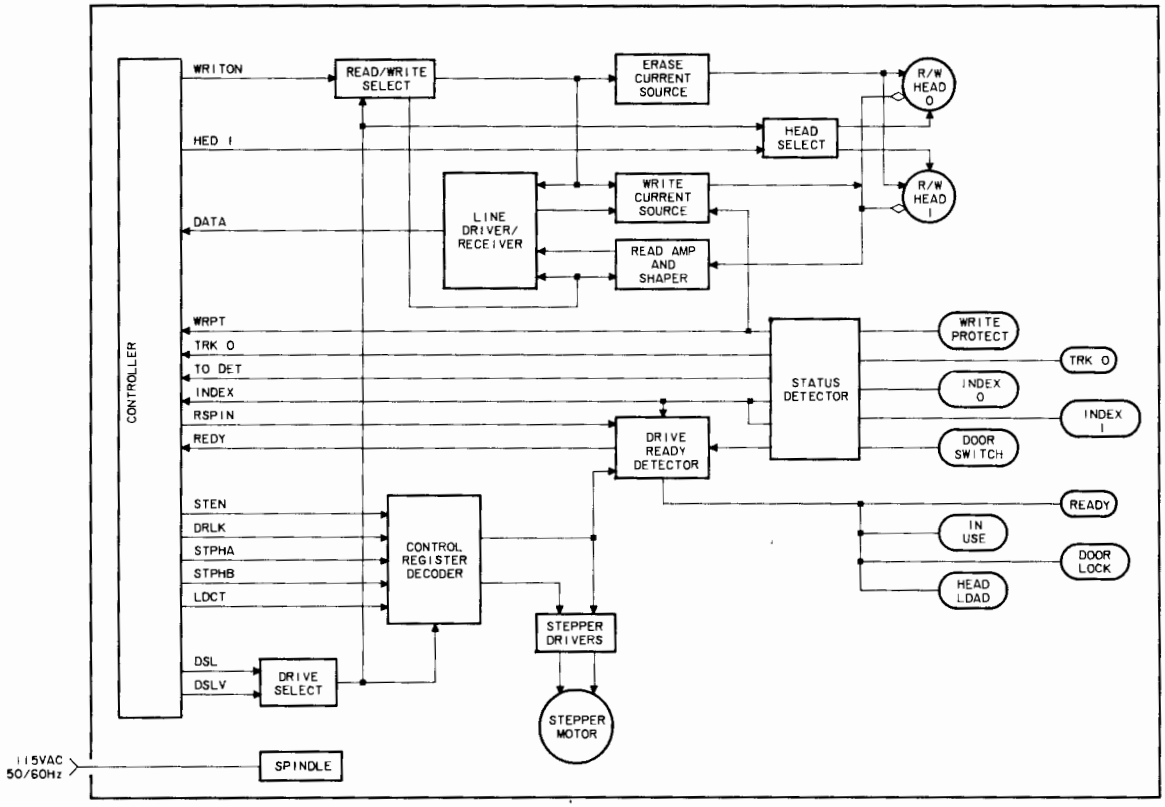


Figure 3-24: Disc Drive Board Block Diagram

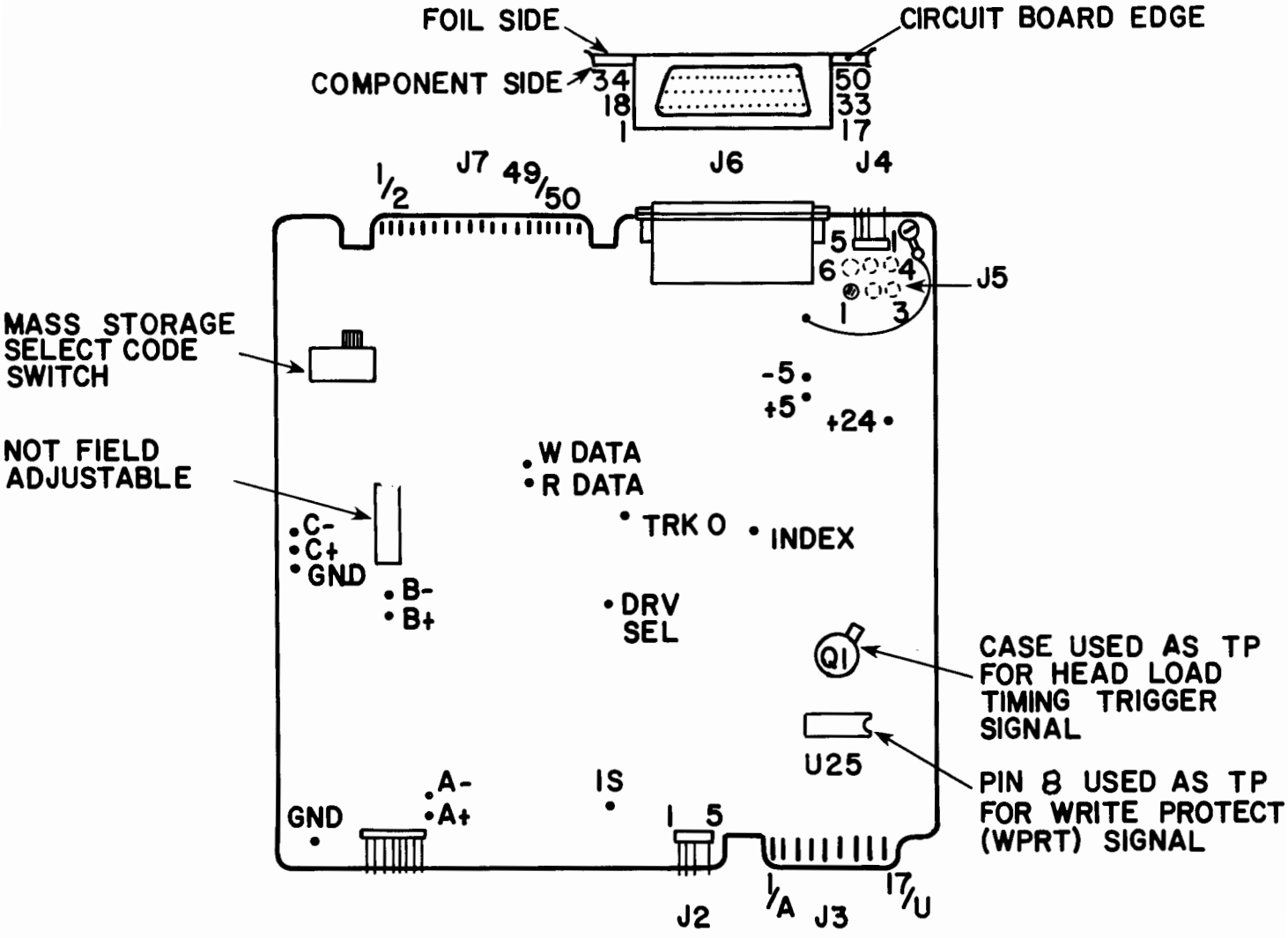


Figure 3-25: Disc Drive Board, A25

Table 3-13: Disc Drive Board Connector Signals

A25J1 Read/Write Heads

Pin	Signal	Pin	Signal
1	R/W Ø	5	R/W 1
2		6	
3		7	
4		8	

A25J2 Drive Rdy/Invse Lamps

Pin	Signal	Pin	Signal
1	+5V	5	$\overline{\text{INUSE}}$
2	$\overline{\text{READY}}$		
3	+5V		
4			

A25J3 Disc Signal Distribution

Pin	Signal	Pin	Signal
1		A	
2		B	
3	+5V	C	TRK Ø LMP
4	+5V	D	WRT PROT LMP
5	+5V	E	INDEX LMP
6	$\overline{\text{DOOR OPEN}}$	F	Gnd
7	$\overline{\text{DOOR CLOSE}}$	H	
8		J	
9	$\overline{\text{DOOR LOCK}}$	K	+24V
10	TRK Ø DET	L	+5V
11	WRT PROT DET	M	+5V
12	INDEX Ø DET	N	+5V
13	INDEX 1 DET	P	
14		R	
15	SMAR	S	SMAR
16	SMBR	T	SMBR
17	$\overline{\text{HEAD LOAD}}$	U	+24V

A25J4 Head Stepper Motor

Pin	Signal	Pin	Signal
1	SMB	5	SMA
2			
3	SMA		
4	SMB		

SMA-Stepper Motor A
SMB-Stepper Motor B

A25J5 DC Power Bus

Pin	Signal	Pin	Signal
1	Gnd	5	-5V
2	Gnd	6	+24V
3	+5V		
4			

A25J6 Disc Controller Board

Pin	Signal	Pin	Signal	Pin	Signal
1		18	LLDCT	34	HDSL1
2	HHED1	19		35	HDSLØ
3	LDSLV	20		36	
4	STPHB	21		37	
5	HPOR	22		38	HDATA
6	HRSPIN	23		39	LDATA
7	STPHA	24		40	
8	LSTEN	25		41	
9	LDRLK	26	Gnd	42	
10	LWRITON	27		43	
11		28		44	
12	LSPIN	29		45	Gnd
13	HREDY	30		46	
14	LTRKØ	31		47	
15	LWRPT	32		48	
16	LINDX	33		49	
17	HPON			50	

A25J7 Disc Interconnect Ribbon

Pin	Signal	Pin	Signal	Pin	Signal
1	*	18	STPHB	34	LWRPT
2	HDSLØ	19		35	
3		20	STPHA	36	HREDY
4	HDSL1	21		37	
5		22	LDRLK	38	HDATA
6		23		39	
7		24	HHED1	40	LDATA
8	LDSLV	25		41	
9		26	HPOR	42	HTØDET
10	LLDCT	27		43	
11		28	LINDX	44	+5V
12	LSTEN	29		45	
13		30	LSPIN	46	+5V
14	HRSPIN	31		47	
15		32	LTRKØ	48	HPON
16	LWRITON	33		49	
17				50	

* Odd #'s are Gnd

Chart 3-9: Disc Drive Controls

-Name-	-Description-	-Adjustment Procedure-
Drive Select-Code Switch	Used to give each disc drive a specific address (0 -2) to be used when using the MASS STORAGE IS (MSI) statement.	none

Test Points

Information concerning the use of Disc Controller Test-Points may be found in Chapter 5, Disc Drive Tests and Alignments.

CHAPTER 4

Software and Firmware

Table of Contents

Parity Error--Data Decoding

Two types of parity error may occur. The program execution parity error, ERROR 1010, is recoverable and will be discussed in this section; the system crash parity error, SYSTEM ERROR P, is not recoverable and will be discussed in the System Crash--Data Decoding section of this chapter.

Error Message

Should a recoverable parity error occur during program execution, the following message will appear on the CRT display:

```
PARITY:  <word 1>  <word 2>
ERROR 1010
```

word 1--is a six digit octal number identifying the memory location at which the parity error occured.

word 2--is a six digit octal number identifying the execution address at which the interrupt occured.

Error Message Decoding

After converting the first error word to binary, Figure 4-1: Parity Error Decoding shows how to decode the error message. Decoding this word allows you to determine which 32k byte memory block caused the parity error. See Chapter 5, Tests and Procedures to isolate the memory down to the IC level.

The second word in the error message is the octal program execution address when the parity error occured.

```
BIT---15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
CODE-- U   L   -   -   -   -  -  -  -  -  -  S3 S2 S1 S0 14
```

-Bit 14 and 15 identify memory word byte

If bit 15=1, error is in upper byte
If bit 14=1, error is in lower byte

-Bits 5 thru 13 are not significant.

-Bits 1 thru 4 give the memory block address were error occurred.

-Bit 0 identifies whether error is in an upper or lower memory block.

If bit 0=1, error is in an upper block
If bit 0=0, error is in a lower block.

Figure 4-1: Parity Error Decoding

Error Recovery

Parity errors identified by the ERROR 1010 message are recoverable. To recover from such an error, execute the CONTINUE or CONT command.

System Crash--Data Decoding

There are four system error types: G, General System Error; M, Memory Protect; I, Illegal Interrupt; and P, Memory Parity Error. The General System Error and Memory Protect Error are usually associated with or caused by software, and the Illegal Interrupt and Memory Parity Error with hardware.

Each of the system errors is considered fatal and will therefore result in a system failure or crash. When a system crash occurs, the error type and system information will appear on the display in the form of a table.

System Crash Message

Two samples of system crash messages appear in Figure 4-2: System Crash-sample message. Note that the SYSTEM ERROR P message has two more lines of data than the SYSTEM ERROR G. The two additional lines are located above the blank line and contain parity error information as explained in the Parity Error--Data Decoding section.

SYSTEM ERROR P	SYSTEM ERROR G
000000	000000
000000	000000
107517	107517
177553	177553
140002	140002
000002	000002
176226	176226
000015	000015
000002	000002
000002	000002
000022	000022
143225	
017361	162027
	161734
162027	044202
161732	044120
044202	043272
044120	042773
043272	
042773	

Figure 4-2: System Crash--sample message

Crash Message Decoding

The octal numbers displayed after a system crash are identified in Figure 4-3: System Crash Decoding. Note that the parity information is only included in the displayed message when SYSTEM ERROR P occurs.

```
SYSTEM ERROR X          identifies the type error
        XXXXXX          contents of accumulator A
        XXXXXX          contents of accumulator B
        XXXXXX          contents of stack pointer
        XXXXXX          contents of stack pointer
        XXXXXX          DMA peripheral address
        XXXXXX          contents of PA register
        XXXXXX          contents of return stack pointer
        XXXXXX          contents of register R32
        XXXXXX          contents of register R34
        XXXXXX          contents of register R35
        XXXXXX          current program line number
        xxxxxx          word 1, parity error memory location
        xxxxxx          word 2, execution address of
                          interrupt

        XXXXXX          remaining numbers are the contents
        XXXXXX            of the return stack
        XXXXXX
        XXXXXX
        XXXXXX
        XXXXXX
```

```
*G--General System Error(software)
 M--Memory Protect Error(software)
 I--Illegal Interrupt Error(hardware)
 P--Memory Parity Error(hardware)
```

Figure 4-3: System Crash Decoding

Crash Recovery

A system crash is a non-recoverable error. The system must be powered down and the Operating System must be reloaded by standard power up procedures.

Support Disc--Utility Routines

Several utility routines are provided on the Support Disc that are not on the Operating System Disc. These routines can be accessed by running an entry program named MENU. Figure 4-4: Support Disc Programs, shows the catalog provided by the MENU program.

```
The programs available on this diskette are as follows:

 1.  LIST   - produces a paginated listing of a SAVED program file.
 2.  UNPRO  - will unprotect a user's protected data files or programs.
 3.  FALIGN - flexible disc alignment programs.
 4.  PWEDIT - allows editing of a data base's maintenance word and passwords
 5.  PTEST  - performs a pattern test on a blank initialized diskette.
 6.  VTEST  - performs a read verify on a diskette.
 7.  PRTCRT - produces a hard copy output of CRT screen.
 8.  NUMCON - displays decimal, octal, hex, and binary equivalent numbers.
 9.  SINFO  - lists system table found on record 0 of disc media.
10.  LISTAT - lists a disc's availability table.
11.  TEST   - gives access to the USER TESTS found on operating system disc.

Enter the number of the test to be called?
```

Figure 4-4: Support Disc Programs

Each of the programs listed requires the user to be active in execution except PTEST and VTEST. PTEST and VTEST are designed to test the disc drive and media.

PTEST is a pattern test that writes several patterns on an initialized disc. The disc must be free of all programs and data. The test writes a pattern on all sectors of each track and then reads and verifies each track and sector. Three different patterns are used for the standard test. Several test options are provided, including a long and short test. The long test takes about 85 minutes per pass, and the short test about 6 minutes per pass. Any errors which occur will be output to a printer.

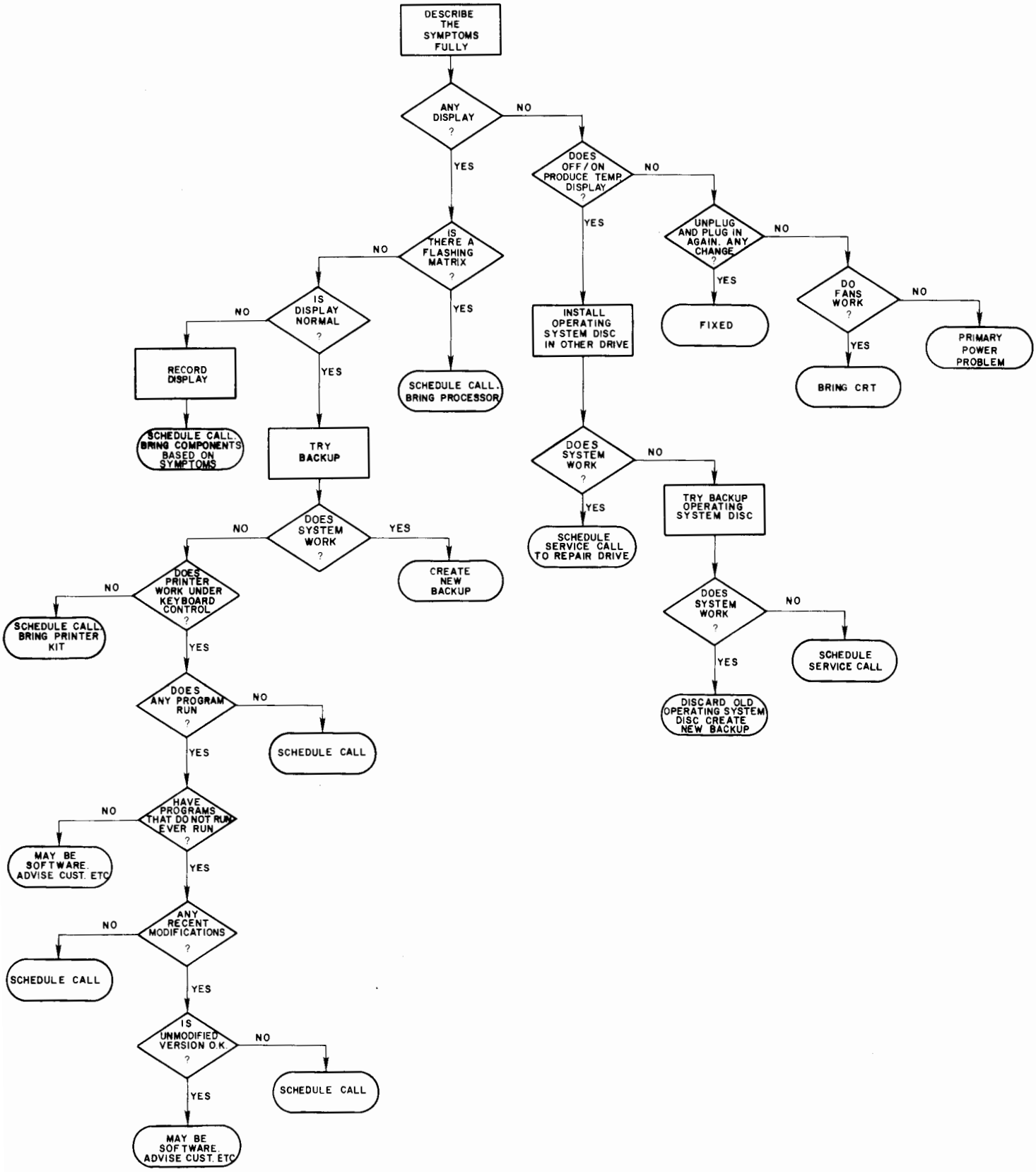
VTEST reads and verifies each track and sector on the disc. The verify is done with tight margins. There are two versions of the test (Fast Test and Detailed Test). The Fast Test will verify the disc in about 1 minute per pass, and the Detailed Test takes about 15 minutes per pass. Both tests are identical except that the Fast Test cannot give the specific area on the disc where the error occured, while the Detailed Test can give the track and sector location of the error.

CHAPTER 5

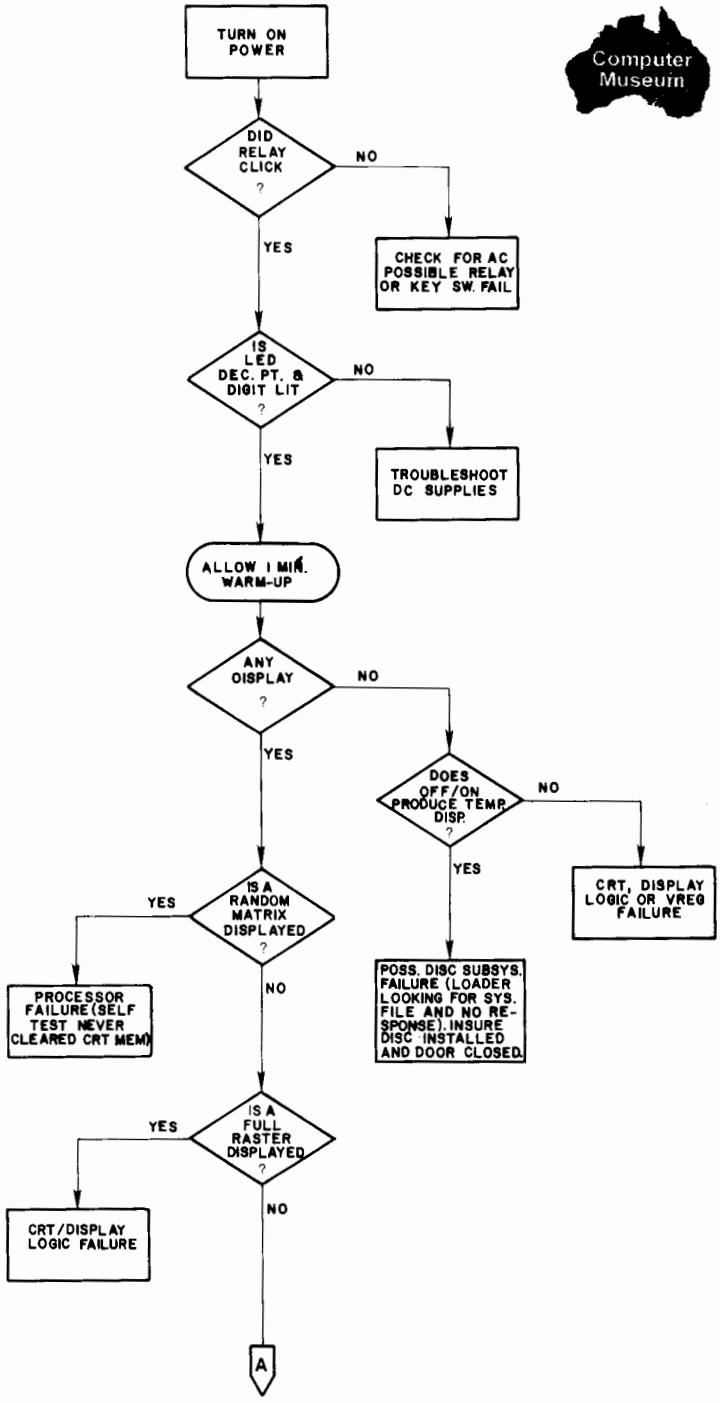
Tests and Procedures

Table of Contents

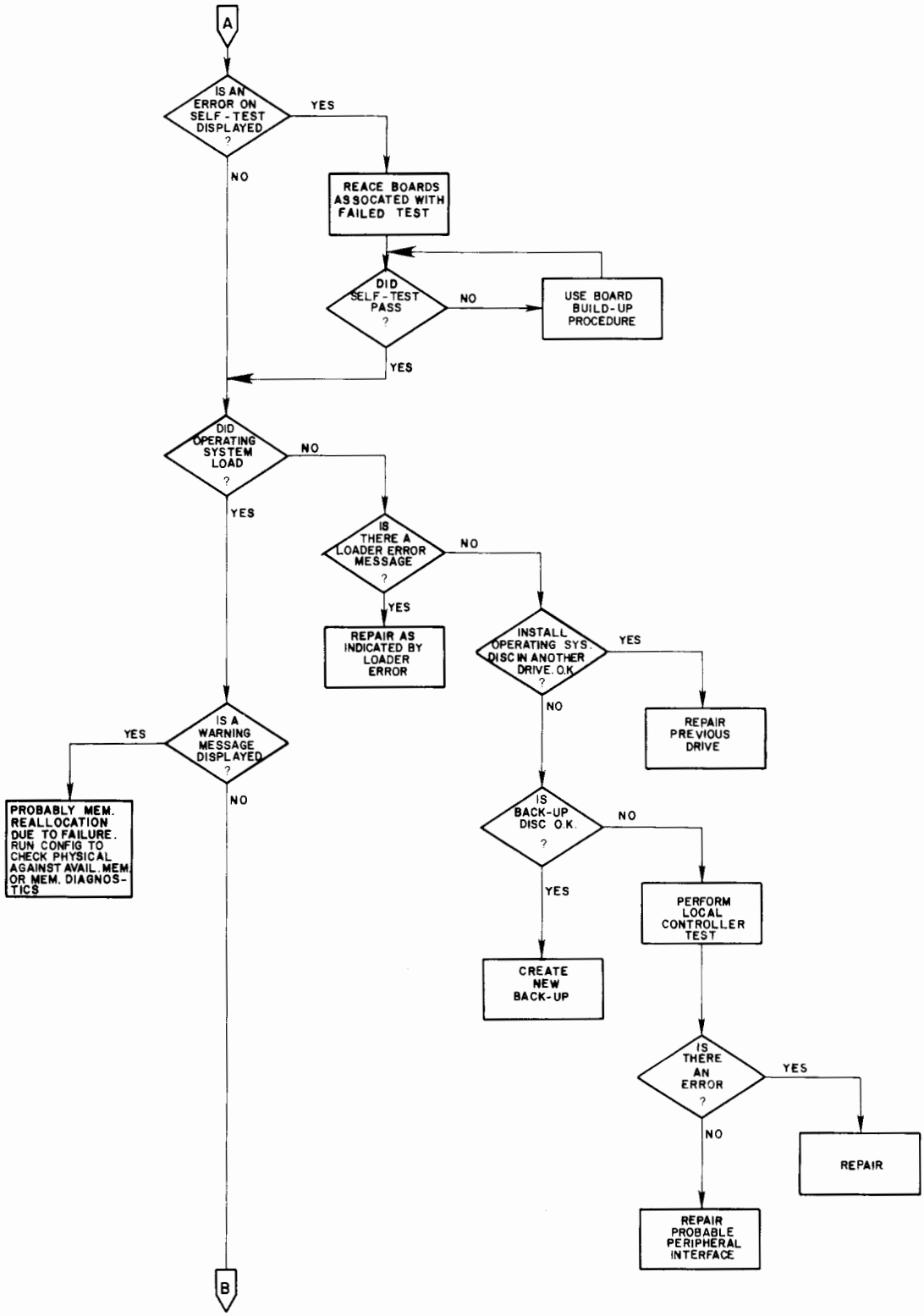
Service Call--Customer Contact Flowchart



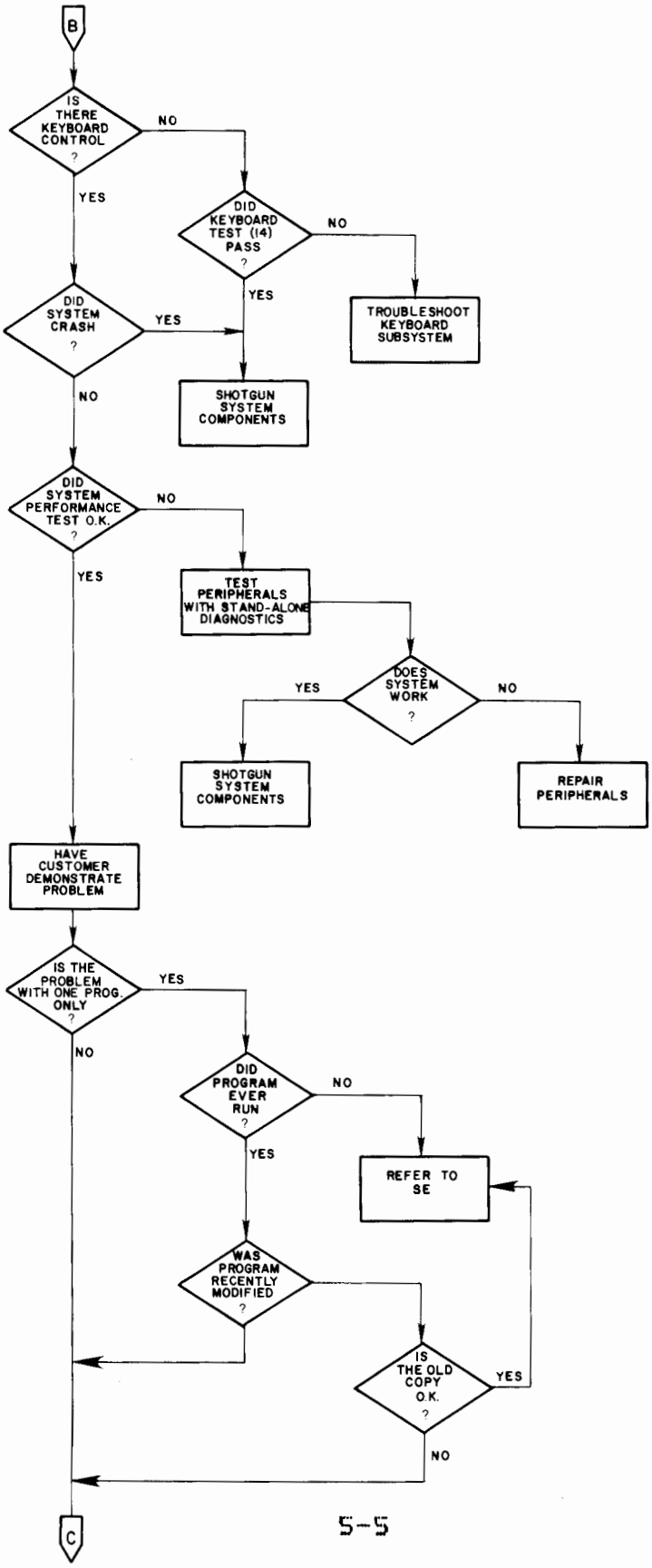
Failure Analysis Flowchart



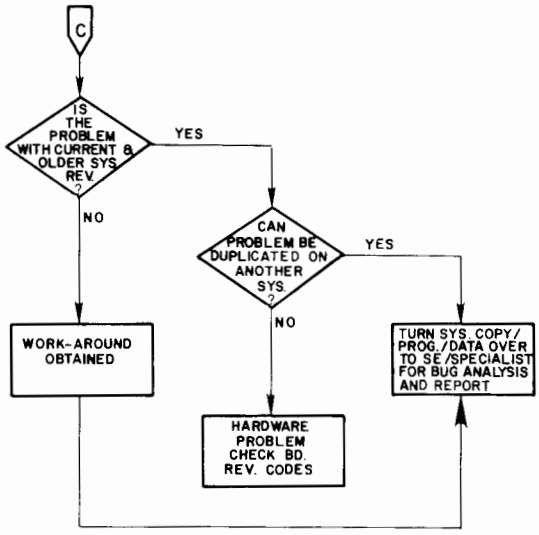
Failure Analysis Flowchart (continued)



Failure Analysis Flowchart (continued)



Failure Analysis Flowchart (continued)



Processor Thumbwheel Switch Tests

The Processor Thumbwheel Switch is used to select which ROM stored self-test is to be performed at system turn-on or when the POP Switch is pressed. The switch has sixteen positions, but only nine of them are available for field service. See Figure 3-8: Processor Board, A5.

Positions 0-3 are used as an extension of the normal turn-on self-test routine.

-Position-	-Function-
0	At turn-on the self-test routine checks that the disc drive and HP 7910K passes its internal self-test. If either one fails, the system self-test will fail.
1	At turn-on the self-test routine does not check the results of any disc internal self-test.
2	At turn-on the self-test routine checks that the disc drive passes its internal self-test. If it fails, the system self-test will fail.
3	At turn-on the self-test routine checks that the HP 7910K passes its internal self-test. If it fails, the system self-test will fail.

The remaining switch positions are used for diagnostic purposes. Consequently, do not leave a customers system with the Processor Thumbwheel Switch in any of the following positions.

-Position-	-Function-
8	Read/Write Memory Test
12	Display ROM Test
13	Display RAM Test
14	Keyboard Test
15	Loop on System Self-test

Read/Write Memory Test

Two types of Read/Write Memory Test are available. A short test which takes approximately two minutes per 32k byte upper block, and a long test which takes approximately one hour per 32k byte upper block. Both types of test will allow a faulty memory chip to be isolated.

The short test consists of three routines: Rotating Pattern, Random Pattern, and Byte Test. When the Read/Write Memory Test is initiated, these routines are automatically run sequentially for each upper memory block selected. Perform the following steps to run the short Read/Write Memory Test:

-Short Test-

1. Set all Block Select switches for Memory Boards to be tested to an upper block in sequence from blocks 1 to 14.
2. Set the Processor Thumbwheel switch to position 8.
3. Press the POP switch.
4. Set thé Processor Thumbwheel switch to the quantity of upper blocks to be tested.
5. The test will automatically repeat itself until terminated or an error occurs.
6. If the Error Log shows a chip which has failed, see Figure 3-21: Memory Board, to locate the faulty chip.
7. Terminate the test by setting the Processor Thumbwheel switch to a position from 0 to 3 and pressing the POP switch.

The long test consists of a single Galloping Pattern routine. This is a pseudoinfinite pattern test that checks each upper memory block selected. Perform the following steps to run the long Read/Write Memory Test:

-Long Test-

1. Set all Block Select switches for Memory Boards to be tested to an upper block in sequence from blocks 1 to 14.
2. Set the Processor Thumbwheel switch to position 8.
3. Press the POP switch.

4. Set the Processor Thumbwheel switch to position 15.

5. Wait until the program asks for the number of blocks to be tested, then set the Processor Thumbwheel switch to the quantity of upper blocks to be tested.

6. The test will automatically repeat itself until terminated or an error coours.

7. If the Error Log shows a chip which has failed, see Figure 3-21: Memory Board, to locate the faulty chip.

8. Terminate the test by setting the Processor Thumbwheel switch to a position from 0 to 3 and pressing the POP switch.

Display ROM Test

The Display ROM Test routine is used to display all characters and enhancement features found in the Display Board. The following is a sample test pattern resulting from the test. The large bars at the bottom of the test pattern may be various characters depending on the Display Board features.

-Test-

1. Set the Processor Thumbwheel switch to position 12.

2. Press the POP switch.

3. Terminate the test by setting the Processor Thumbwheel switch to a position from 0 to 3 and pressing the POP switch.

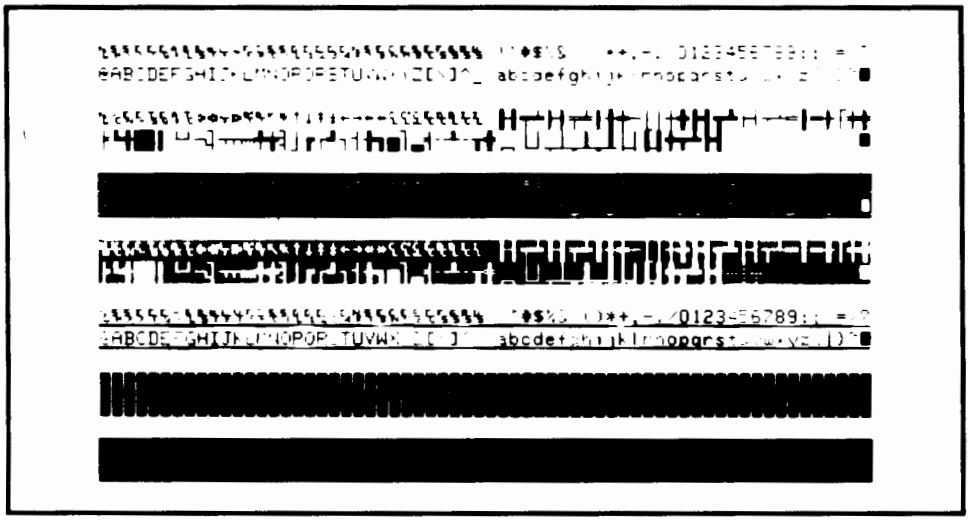


Figure 5-1: Display ROM Test--sample pattern

Display RAM Test

The Display RAM Test checks all display refresh memory locations by writing ones and zeros into each memory location. When the test is performed, the display will alternate between two presentations at about a 10 Hz rate.

Each displayed presentation consists of two columns of half-bright, blinking 'U's with cursor alternating with two columns of underlined, inverse video '*'s. The order of the columns will change from one to the other. The figure shows a sample of the test patterns.

-Test-

1. Set the Processor Thumbwheel switch to position 13.
2. Press the POP switch.
3. Terminate the test by setting the Processor Thumbwheel switch to a position from 0 to 3 and pressing the POP switch.

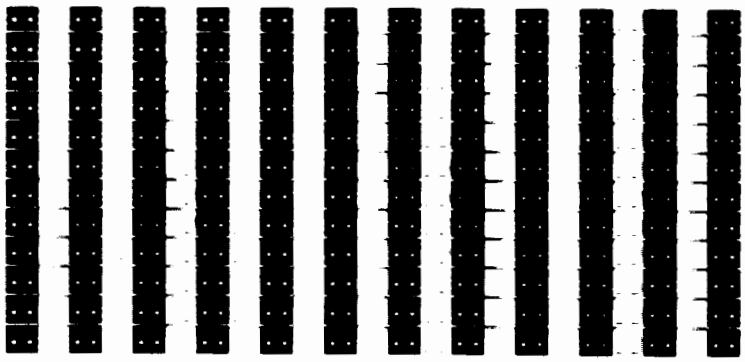


Figure 5-2: Display RAM Test--sample pattern

Keyboard Test

The Keyboard Test services interrupts from the keyboard, converts the keycode to ASCII, and displays the U.S. ASCII character on the CRT. The halt and user defined keys do hot have ASCII characters to 'HT' and 'K#' (#=1-24) are displayed respectively. If shift is used, a beep is sounded when the halt key is pressed.

Figure 5-3 shows the displayed results when the keys are pressed in the following order: user defined keys, typewriter keyboard keys, and data entry pad keys. The order is then repeated with the shift key depressed.

-Test-

1. Set the Processor Thumbwheel switch to position 14.

2. Press the POP switch.

3. With the shift key up, perform the following:
   a. Going from left to right press all user defined keys (including softkeys) and editing keys including halt.

   b. Going from left to right press all typewriter block keys.

   c. Going from left to right press all data entry pad keys.

   d. Press the minus and plus key on the data entry pad.

4. Press and lock the shift key, and repeat steps 3a to 3d.

5. Check that the CRT display matches Figure 5-3.

6. Terminate the test by setting the Processor Thumbwheel switch to a position from 0 to 3 and pressing the POP switch.

```
SELF-TEST  A
 1 BPC              PASS
 2 BLKSW            PASS
 3 PWFIND           PASS
 4 IOC              PASS
 5 EMC              PASS
 6 BLKSW2           PASS
 7 PROC BD          PASS
KEYBD
  K 1 K 2 K 3 K 4 K 5 K 6 K 7 K 8 K 9 K10 K11 K12 K13 K14 K15 K16↖↑↑←↑↓→↖ HT↹12
34567890-=◆◆qwertyuiop[¶asdfghjkl;'%z>cvbnm,./7894561230.%%   K 1 K 2 K 3 K 4 K
5 K 6 K 7 K 8 K17 K18 K19 K20 K21 K22 K23 K24↖↑↑←↑↓→↖ HT↹!@◆$%^&*()_+◆◆QWERTYUI
OP]¶ASDFGHJKL:'%Z>CVBNM<>?7894561230.%%
```

Figure 5-3: Keyboard Test--sample display

Loop on System Self-Test

The Loop on Self-Test routine repeats the standard self-test that is run at power on. The routine is initiated by placing the Processor Thumbwheel switch to position 15, and pressing the POP switch. Terminate the routine by placing the thumbwheel switch to a position from 0 to 3.

Cardcage Board Build-up Procedures

The following procedures allow the HP 250 electronics (cardcage boards) to be installed one by one so that the faulty board may be isolated. Before performing each step, turn the HP 250 off. After each step is performed, turn the HP 250 back on and check for the indicated results.

-STEP-	-BOARDS INSTALLED-	-LED*-	-CRT-	
1.	Display Logic (orange)		Random Pattern	
2.	Processor (violet)	0	1. BPC 2. Blksw	Pass Fail
3.	Block Switch (green)	2	1. BPC 2. Blksw 3. RW Find	Pass Pass Fail
4.	Memory (red)	7	1. BPC 2. Blksw 3. RW Find 4. IOC 5. EMC 6. Blksw2 7. Proc. Bd. 8. Mem. Table 9. HPIB I/O	Pass Pass Pass Pass Pass Pass Pass Pass Fail
5.	Peripheral Interface (blue)	7	1. thru 9. 10. Floppy	Pass Fail
6.	Floppy Controller (yellow)	9	1. thru 10. system loads, but there is no keyboard control	Pass
7.	Keyboard Logic (gray)	9	1. thru 10. system loads, normal operation	Pass

*Displayed number on the Processor Board Test Indicator
See Chapter 3, Hardware; Figure 3-8: Processor Board, A5.

Disc Drive Tests and Alignments

This section contains a listing of all special tools and equipment required to service the HP 250 disc drive, and all test and alignment procedures that are to be performed in the field.

-WARNING-

Use extreme caution when working on the disc drive with power applied. Hazardous voltages are present inside the disc drive whenever it is connected to an active ac power source.

Do not attempt to remove or change printed circuit assemblies or interconnecting cables without first removing power from the disc drive.

-CAUTION-

Never attempt to swing open the cartridge guide assembly without first unloading the heads from the head load bail. See Figure 5-5: Head Unloading.

Never allow the heads to touch each other. Whenever the heads are unloaded from the head load bail, place a piece of clean lens tissue between the heads to prevent them from touching.

The read/write heads are factory aligned with a four-track offset between the heads. Loosening the head-mounting screw will destroy this offset and necessitate the return of the disc drive for realignment.

Do not lubricate the disc drive--oil will cause dust and dirt to accumulate.

Instructions displayed when running the FALIGN program may conflict with those of the following procedures. Should this happen, the procedures and instructions listed herein will take precedence.

Special Tools and Equipment

-Tool-	-Part Number-
Alignment Disc No. 360/2	9164-0098
Alignment Disc No. 360/2A	9164-0111
Cartridge Guide Adjustment Tool	1150-1310
Bail Gauge	1535-3875
Oscilloscope, dual-trace	-----
Support Disc	45000-15000

Disc Drive Component Locations

This section contains pictures and drawings showing various parts of the disc drive unit. Refer to this section as necessary when performing the test and alignment procedures for the disc drive.

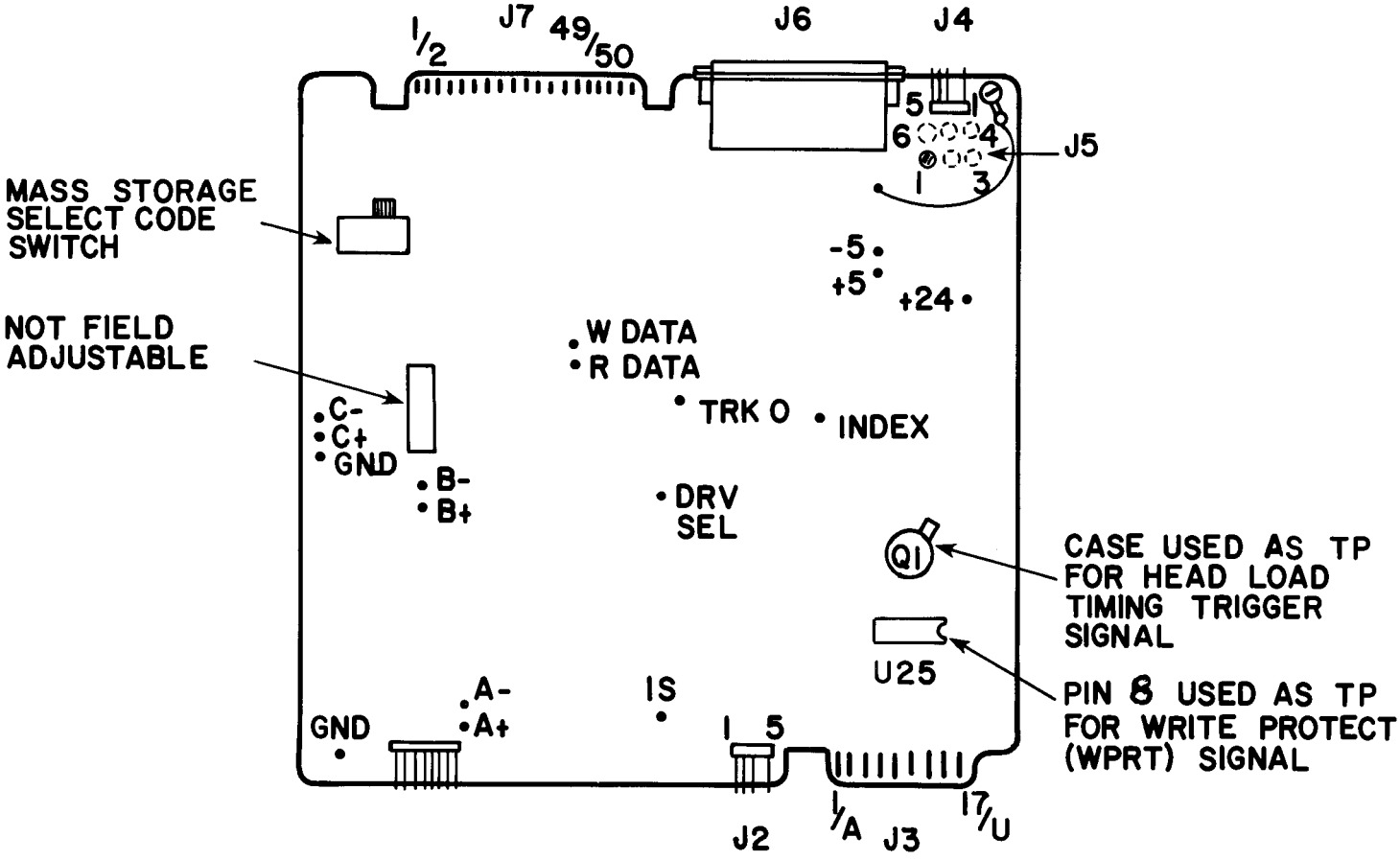
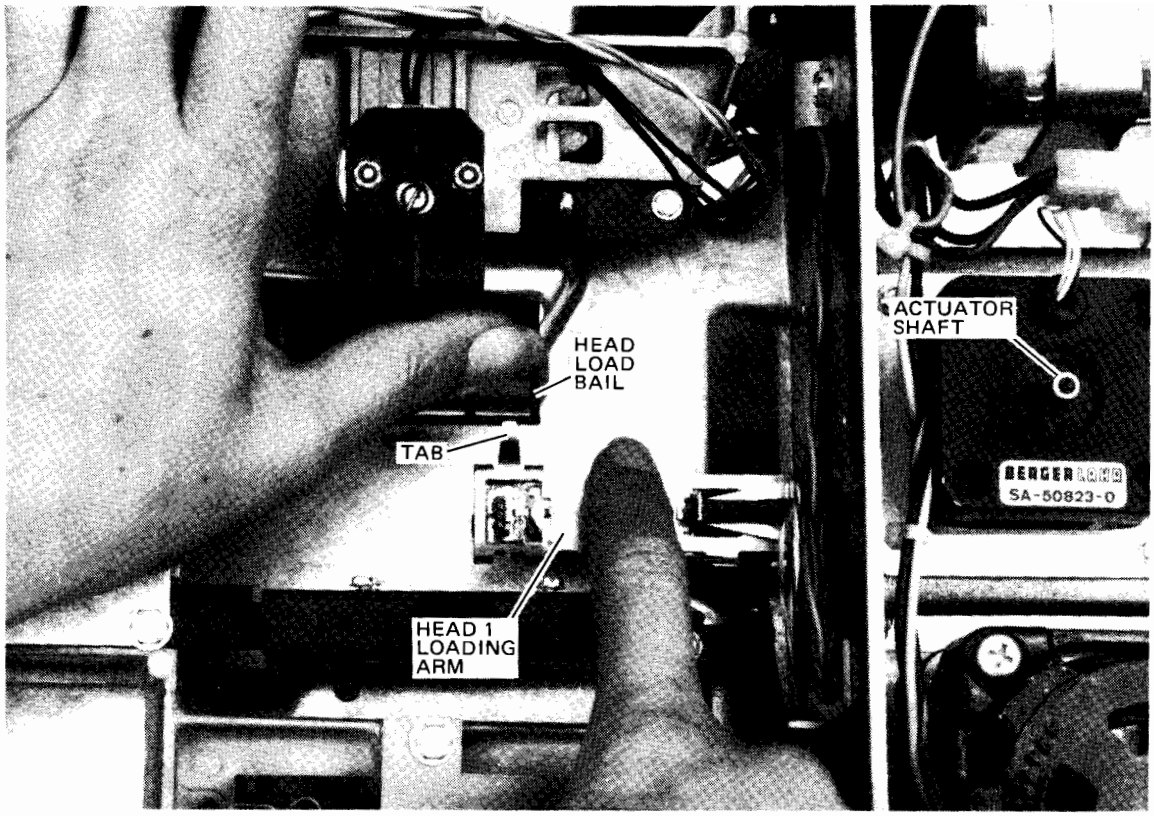
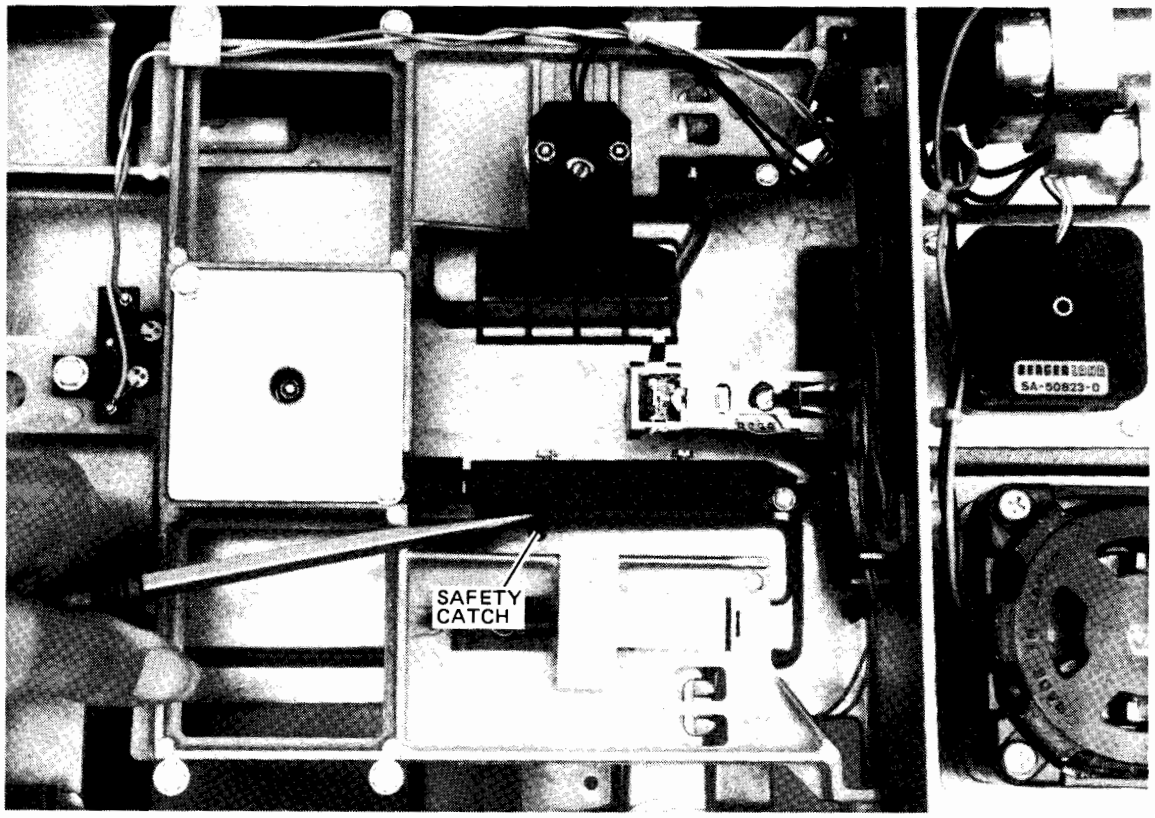


Figure 5-4: Disc Drive Board



A. HEAD UNLOADING



B. SAFETY CATCH RELEASE

Figure 5-5: Head Unloading

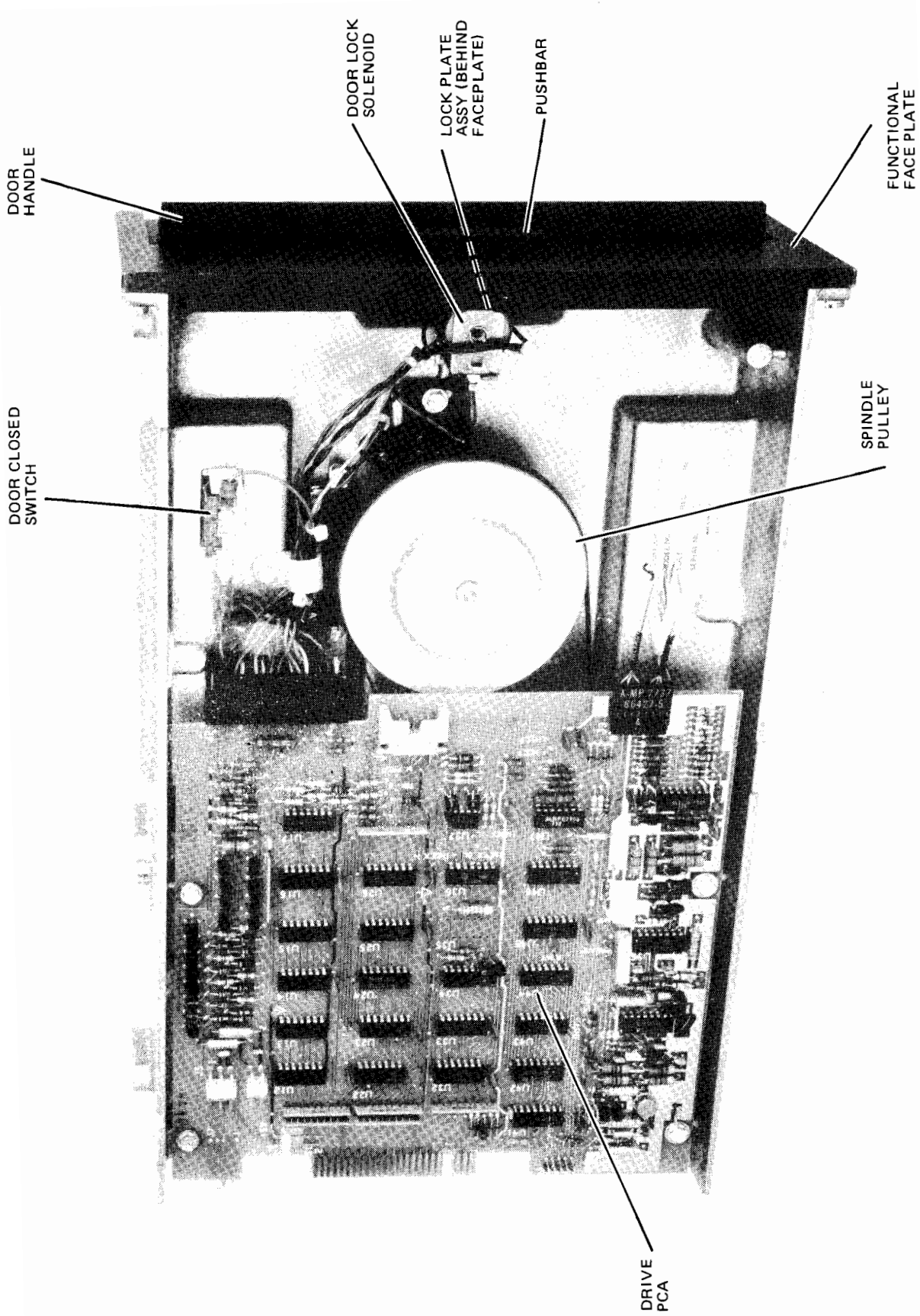


Figure 5-6: Component Location, Bottom View

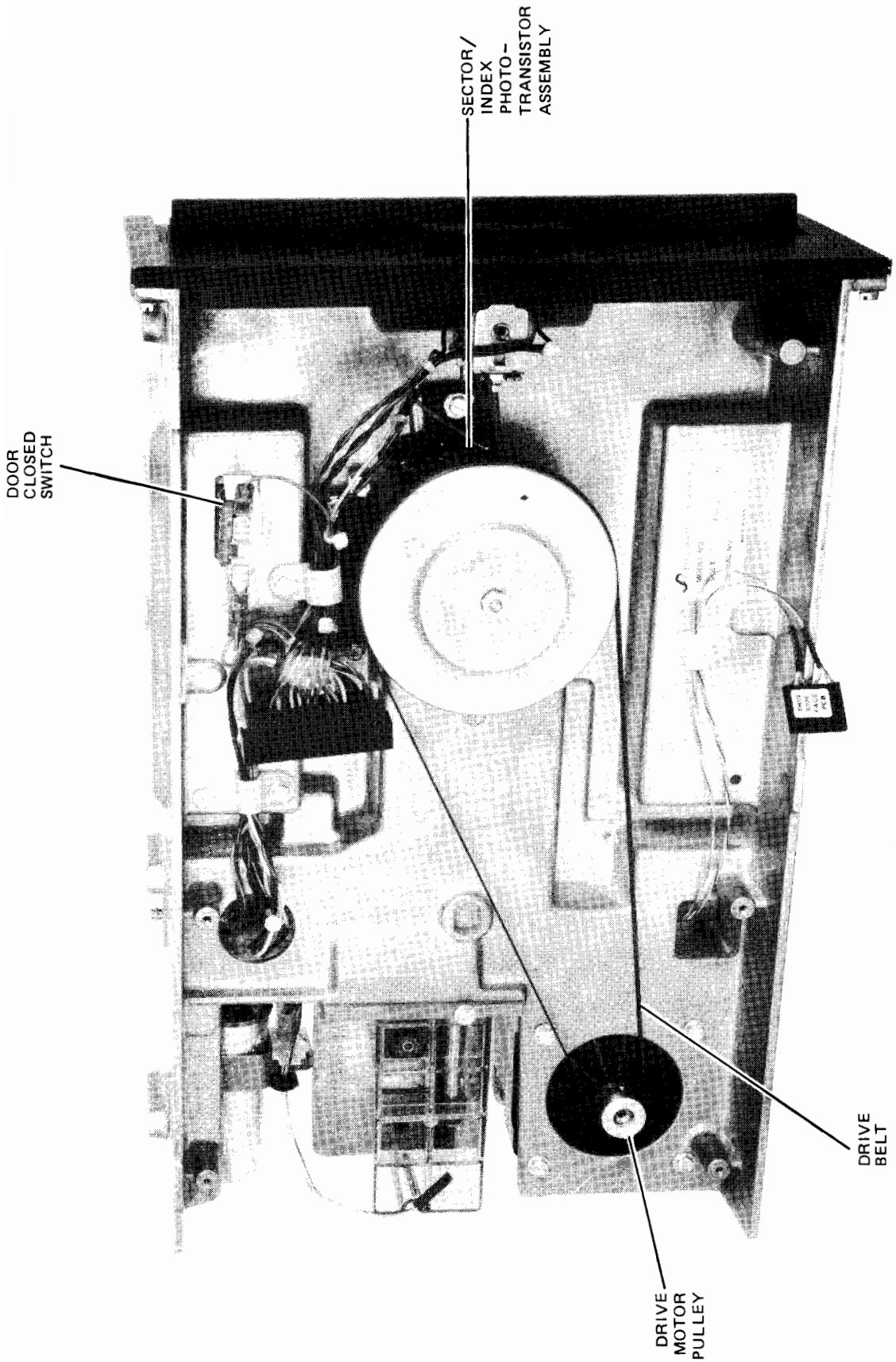


Figure 5-7: Component Location, Bottom View
Drive Board Removed

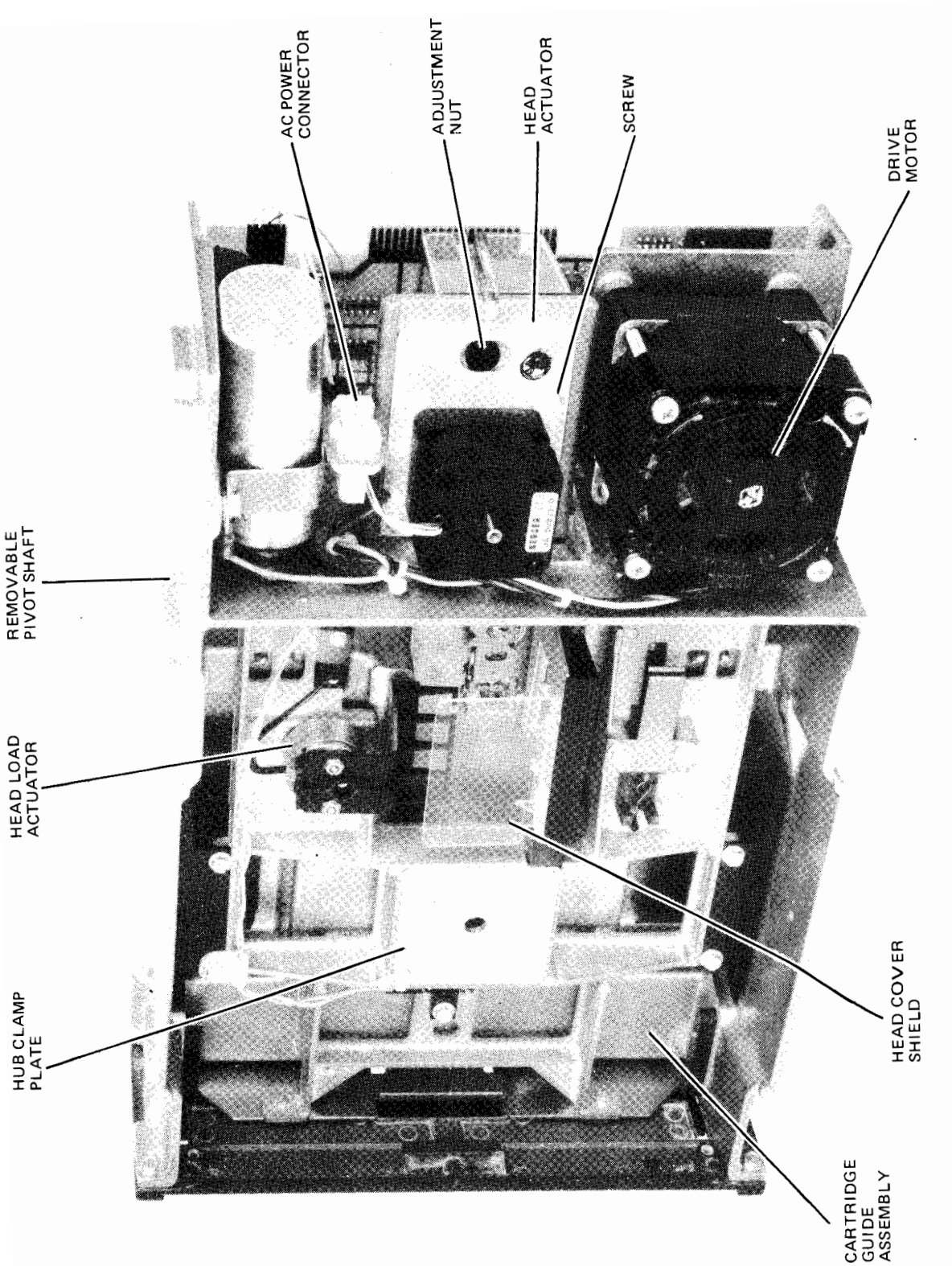


Figure 5-8: Component Location, Top View.

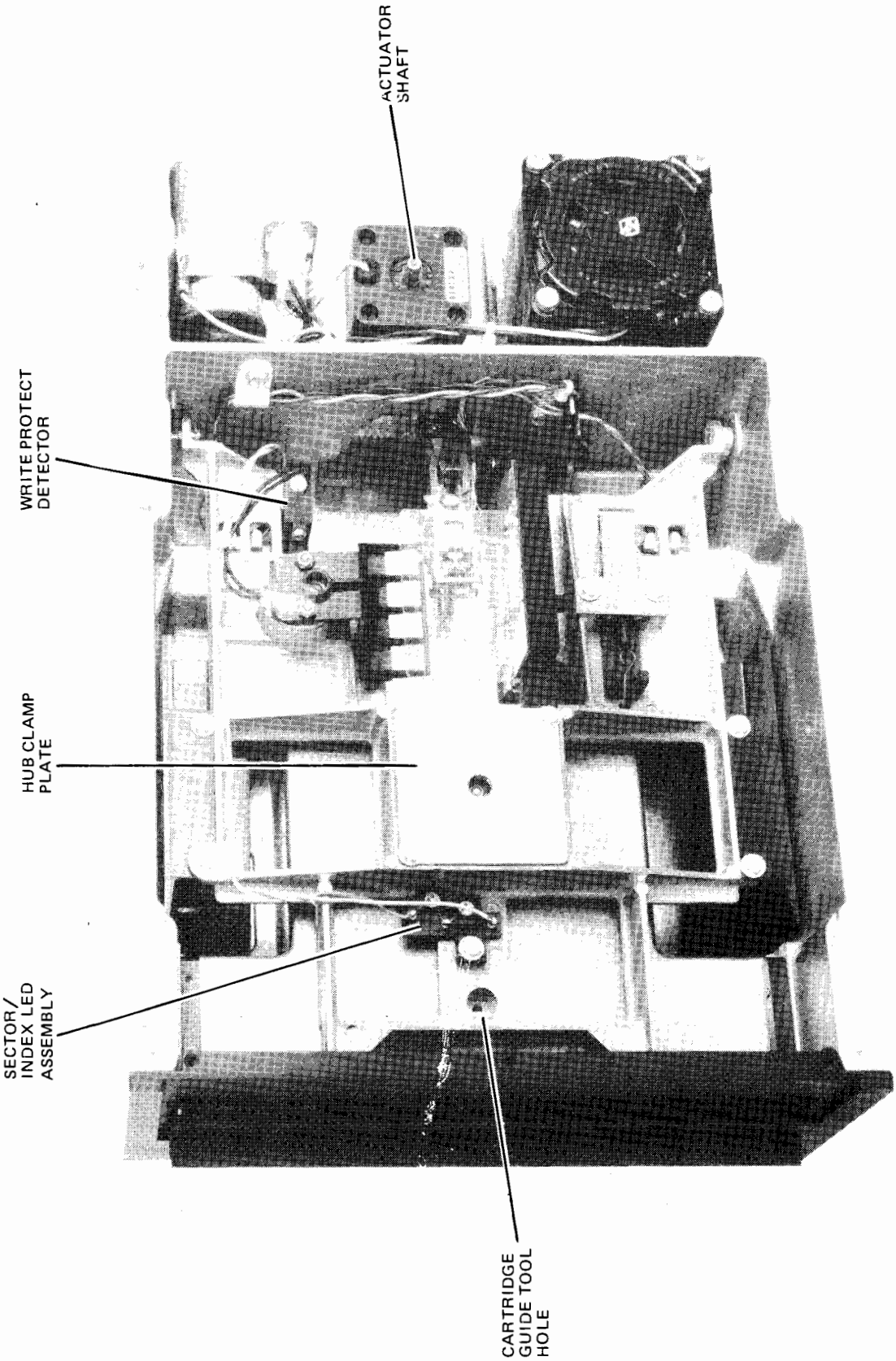


Figure 5-9: Component Location, Top View

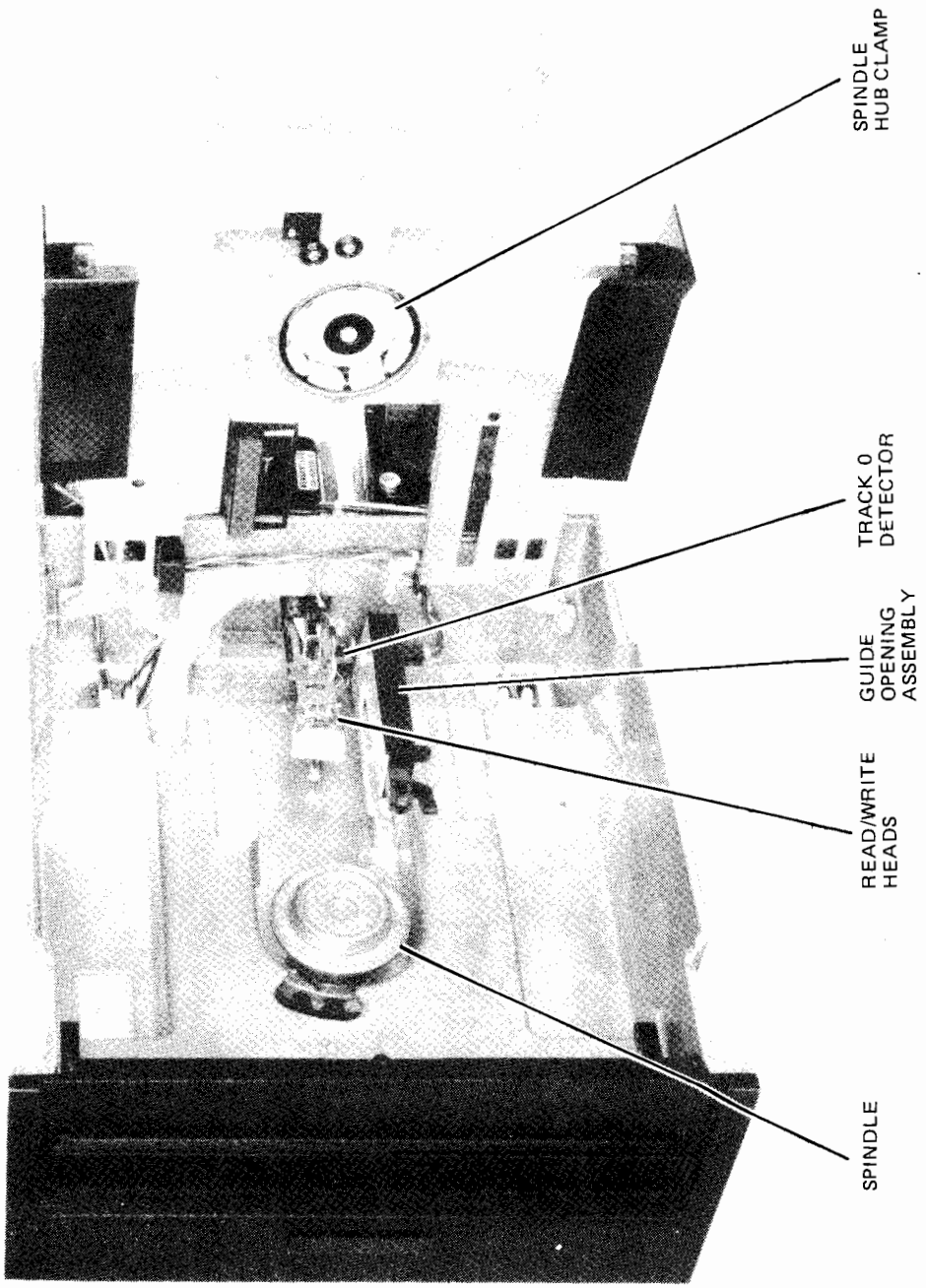


Figure 5-10: Component Location, Cartridge Guide Assembly

Head Load Timing and Actuator Adjustment

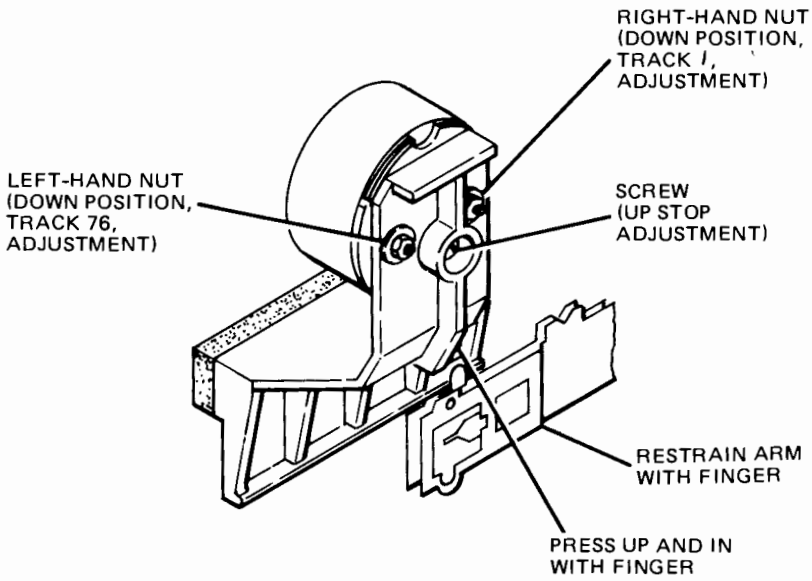
This procedure consists of a coarse mechanical and a fine electrical adjustment to set the head loading delays and data settling times. It should be performed anytime the head load solenoid is removed, adjusted, or replaced; or when errors in reading or writing onto the disc occur.

-Adjustment-

1. Remove the head Cover Shield.

2. Position the head to track 1 by performing the following:
   a. Run the FALIGN program found on the Support Disc.
   b. Press the INDEX TEST softkey.
   c. Insert the Alignment Disc into the drive to be aligned. Close the drive door and press the CONTINUE softkey when ready.
   d. Select the drive to be aligned by pressing the desired softkey. (this will step to track 1 and load the head)

3. Adjust the right-hand self-locking nut securing the bail to the actuator until the bail adjustment gauge just fits between the bail and the tab on the head arm.



ADJUSTMENT CONTROLS AND UNLOADING DETAILS

Figure 5-11: Head Load Actuator Adjustment

4. Press the STEP TO TRACK 76 softkey and repeat step 3 by adjusting the left-hand nut.

5. Return to track 1 and recheck the adjustment. Repeat steps 3 and 4 if necessary.

6. Press the STEP TO TRACK 76 softkey to reposition the heads to track 76.

7. Press RESTART softkey to exit this test routine.

8. Remove the Alignment Disc and leave the drive door open.

9. Place the loop of the bail adjustment gauge over the tip of the load arm tab and carefully pull the arm up to its maximum travel being careful not to flex the arm. Adjust the up-stop screw until the bail just contacts the head load arm tab.

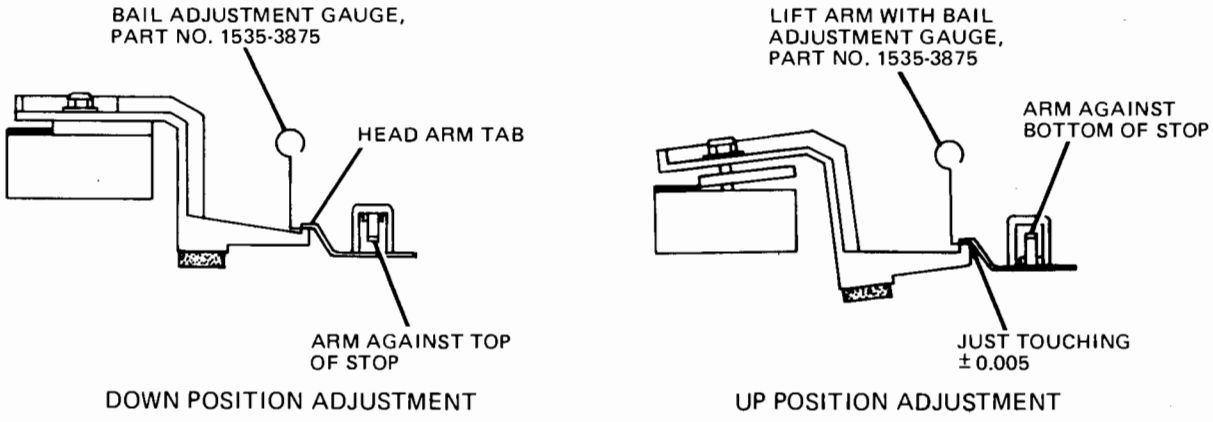


Figure 5-12: Head Load Actuator Up-stop Adjustment

10. Instal a scratch disc and check that there is clearance between the disc and the upper head, and then remove the disc.

11. Replace the head Cover Shield.

12. Set the oscilloscope controls as follows:

    sweep: 5 msec/div
    sensitivity: .1 volts/div
    input: DC
    display: A
    trigger: normal, external, -

13. Set the A-channel probe to TP C+, and the EXT TRIG probe to the case of transistor Q1. See Figure 5-4: Disc Drive Board.

14. Press the HEAD LOAD TIMING softkey.

15. Insert the Alignment Disc into the drive to be aligned. Close the drive door, and press the CONTINUE softkey when ready.

16. Select the drive to be aligned by pressing the desired softkey. (this will cycle the head load function with head 0 selected)

17. The signal amplitude should reach 90% of its steady state within 35 ms. If the time exceeds 35 ms, adjust the up stop screw clockwise (not more than 1/4 turn) until the timing is less than 35 ms.

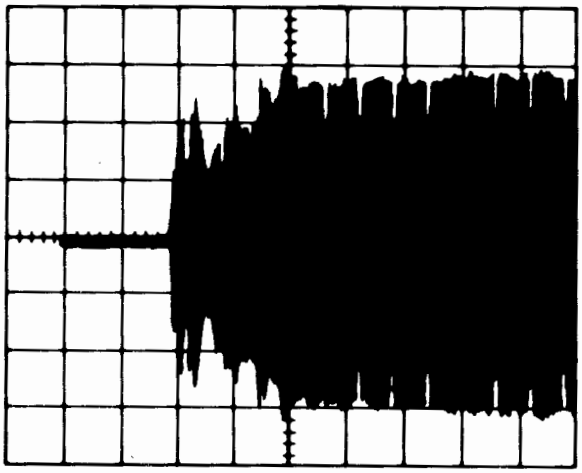


Figure 5-13: Head Load Timing waveform

18. Press the UPPER HEAD 1 softkey and repeat step 17.

19. If the proper timing cannot be acquired by turning the up stop screw less than 1/4 turn repeat the entire procedure.

20. Press the RESTART softkey to exit this test routine.

21. Remove the Alignment Disc.

Azimuth Test

This test checks the offset of each head from the perpendicular to the tangent of the track. It should be performed anytime read errors occur or when there is incompatibility between discs and drives.

To perform this test requires version No. 360/2A of the Alignment Disc. There is a unique pattern on track 76 to measure the amount of angular offset of the head gap to the track. An offset deviation of + or - 18 minutes is the maximum allowable. The following procedures check that the drive is within these limits.

-Test-

1. Set the oscilloscope controls as follows:

   sweep: .5 msec/div
   sensitivity: .1 volts/div
   input: DC
   display: A+B, B inverted
   trigger: normal, external, +

2. Connect the A-channel probe to TP C+, B-channel probe to TP C-, and the EXT TRIG probe to TP INDEX. See Figure 5-4: Disc Drive Board.

3. Run the FALIGN program found on the Support Disc.

4. Press the AZIMUTH ADJUST softkey.

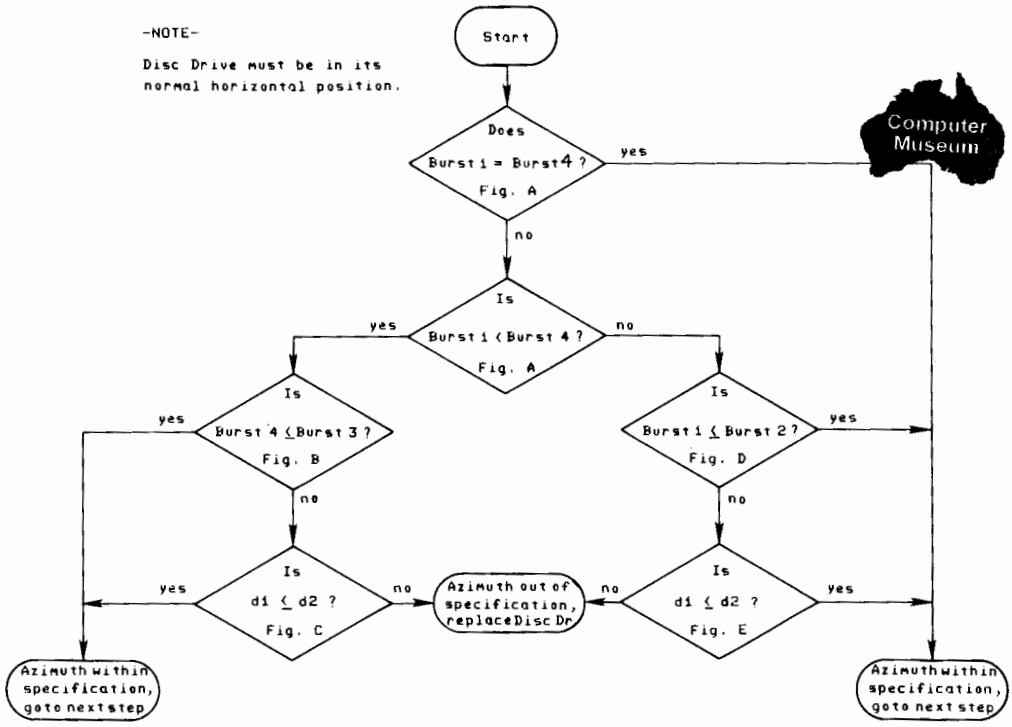
5. Insert the Alignment Disc into the drive to be aligned. Close the drive door, and press the CONTINUE softkey when ready.

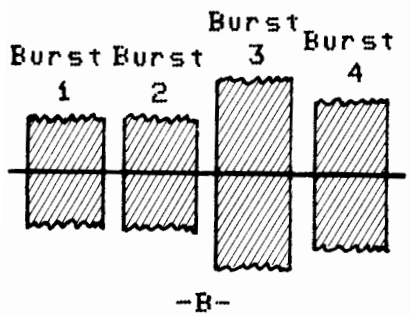
6. Select the drive to be aligned by pressing the desired softkey. (head will seek to track 76, select head 0, and do a continuous read)

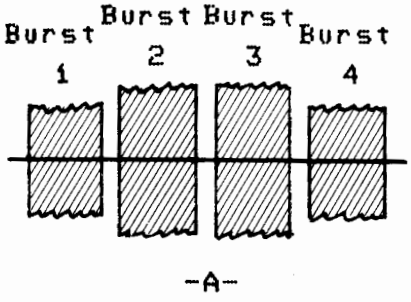
NOTE

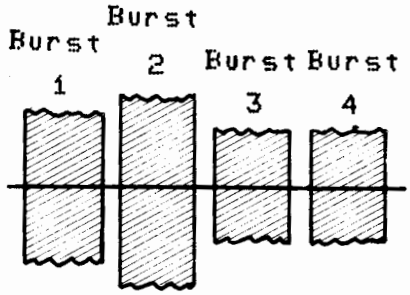
The disc drive unit under test must be in its normal horizontal position. Failure to properly position the drive will result in errors in the azimuth measurement.

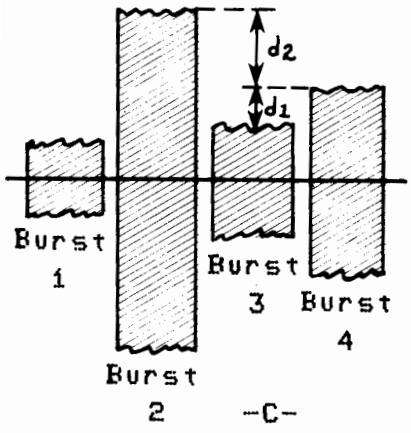
7. Follow the flowchart in Figure 5-14. Reject the disc drive or continue to step 8 as directed by the flowchart.











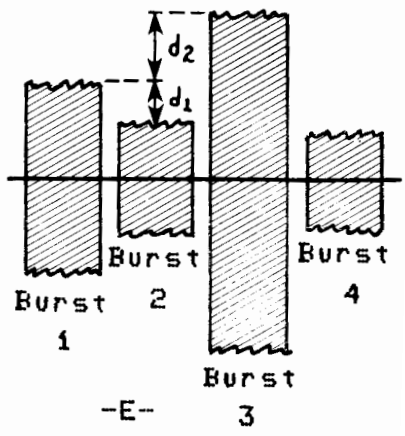


Figure 5-14: Azimuth Test procedure flowchart

8. Test Head 1 by pressing the UPPER HEAD1 softkey and repeating step 7.

9. Press the RESTART softkey to exit this routine.

10. Remove the Alignment Disc.

Head Radial Alignment Test and Adjustment

This test checks the radial alignment of the disc drive heads to ensure disc to disc compatibility. It should be performed when repeated read errors occur or when there appears to be a disc compatibility problem.

The adjustment is made by reading a cat's eye pattern from track 38 on the Alignment Disc. A compromise from the optimum setting for each head may be necessary since they are moved simultaneously.

NOTE

Due to variations in disc size with temperature and humidity, approximately 20 minutes should be allowed for the Alignment Disc to stablize at the ambient room conditions. For best results, the disc should be removed from the PSP and taken out of its protective jacket as soon as you arrive at the test site. This lets the disc acclimate as fast as possible. The longer you can wait, the more accurate the test results.

-Test and Adjustment-

1. Set the oscilloscope controls as follows:

   sweep: 20 msec/div
   sensitivity: .01 volts/div
   input: DC
   display: A+B, B inverted
   trigger: normal, external, +

2. Connect the A-channel probe to TP B+, the B-channel probe to TP B-, and the EXT TRIG probe to TP INDEX. See Figure 5-4: Disc Drive Board.

3. Run the FALIGN program found on the Support Disc.

4. Press the RADIAL ALIGNMENT softkey.

5. Insert the Alignment Disc into the drive to be aligned. Close the drive door, and press the CONTINUE softkey when ready.

6. Select the drive to be aligned by pressing the desired softkey. (head will step to track 38, select head 0, and do a continuous read)

7. Make an estimate of the relative humidity in the room where the drive is operating, i.e. is it low (8% to 39%), medium (40% to 59%), or high (60% to 80%).

8. Compare the waveform with that shown in Figure 5-15: Head Radial Alignment waveforms. Use the following limits when checking the waveforms.

   LOW HUMIDITY (8% to 39%): The left lobe amplitude must be between 65% and 105% of the right lobe amplitude.

   MEDIUM HUMIDITY (40% to 59%): The smaller lobe amplitude, either left or right, must be at least 80% of the larger lobe amplitude.

   HIGH HUMIDITY (60% to 80%): The right lobe amplitude must be between 65% and 105% of the left lobe amplitude.

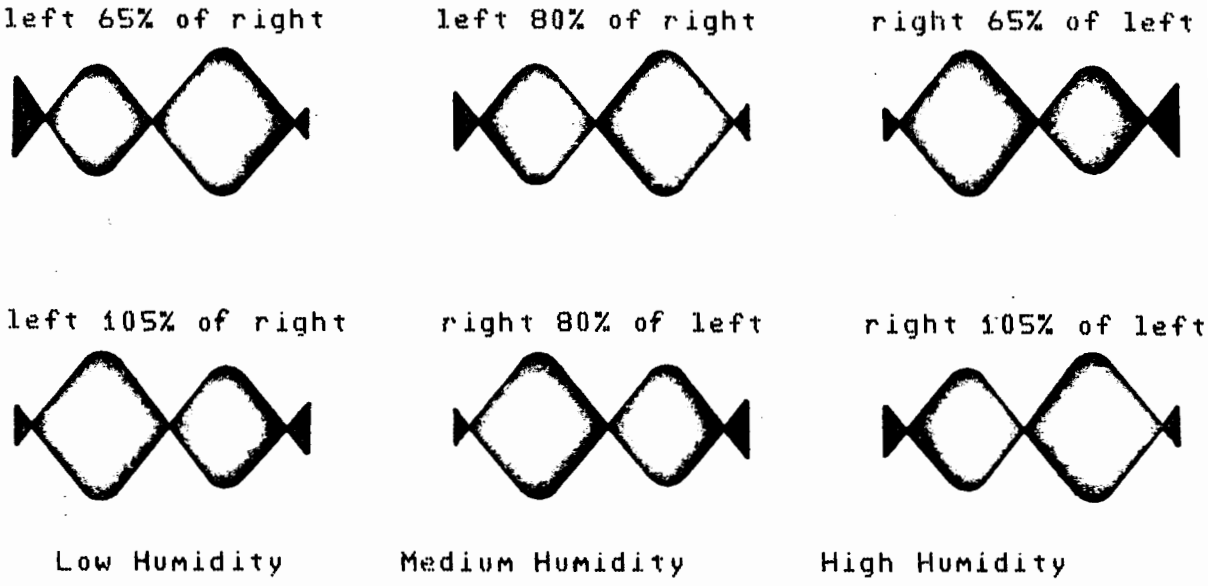


Figure 5-15: Head Radial Alignment waveforms

9. Press the UPPER HEAD 1 softkey and repeat step 8.

10. If either head is out of adjustment, loosen the locking screws adjacent to the stepper motor and rotate the adjustment screw until the head that is out of alignment comes into specification. Recheck the other head.

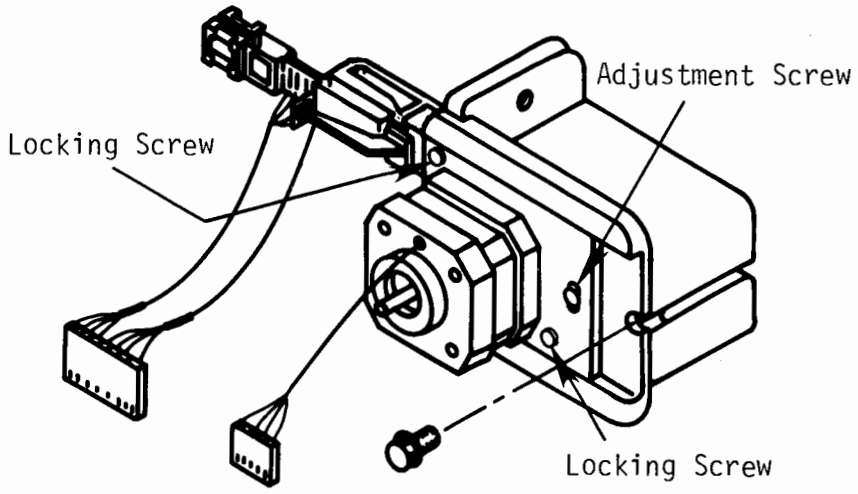


Figure 5-16: Radial Alignment Adjustment

11. Repeat steps 8 through 10 until an optimum signal is obtained for each head. To obtain alignment for both heads, a compromise from the optimum for either head may be necessary.

Steps 12 and 13 check the amount of hysteresis in the radial movement of the heads. Hystersisis must not add or subtract more than 15% to the ratio (percentage) found during step 8. You should note that any hysteresis is independent of the radial alignment and if the amount of hysteresis exceeds + or - 15%, the drive unit must be replaced.

12. Step to track 39 and back to track 38 by pressing the STEP IN TRACK 39 softkey. The lobe amplitudes should not change by more than 15%. (i.e., if one lobe was 80% of the other, now it should be from 65% to 95% of the other.

13. Step to track 37 and back to track 38 by pressing the STEP OUT TRACK 37 softkey. The lobe amplitudes should remain within the limits specified in step 12.

14. Press the RESTART softkey to exit this test routine.

15. Remove the Alignment Disc.

16. Perform the Track 0 Detector Test and Adjustment on page 5-31.

Track 0 Detector Test and Adjustment

This test ensures that track '0' is detected at only one position on the disc. It should be performed anytime seek errors occur or when the Head Radial Alignment adjustment is made.

The detector is adjusted so that its output will change states as the heads step from track 1 to track 2 or track 2 to track 1. The output of the detector is ANDed with inputs to the stepper motor which represent steps 0, 4, 8, etc.

-Test and Adjustment-

1. Set the oscilloscope controls as follows:

   sweep: 5msec/div
   sensitivity: .2 volts/div
   input: DC
   display: A
   trigger: auto

2. Connect the A-channel probe to TP TRK0. See Figure 5-4: Disc Drive Board.

3. Run the FALIGN program found on the Support Disc.

4. Press the TRACK 0 DETECT softkey. (heads will step to track 1)

5. Insert a scratch disc into the drive to be aligned. Close the drive door and press the CONTINUE softkey when ready.

6. Select the drive to be aligned by pressing the desired softkey.

7. Check that the signal at TP TRK0 is high. If it is low, loosen the screw securing the Track 0 Detector Assembly and slowly move it toward the spindle until the signal at TP TRK0 goes high. Carefully tighten the assembly mounting screw.

8. Press the STEP TO TRACK 2 softkey.

9. Check that the signal at TP TRK0 is low. If it is high, carefully loosen the screw securing the Track 0 Detector Assembly and slowly move the assembly away from the spindle until the signal at TP TRK0 goes low. Carefully tighten the assembly mounting screw.

10. Press the STEP TO TRACK 1 softkey.

11. Repeat steps 7 thru 10 until the signal at TP TRK0 is high at track 1 and low at track 2.

12. Press the RESTART softkey to exit the test routine.

13. Remove the scratch disc.

Write Protect Detector Adjustment

This adjustment ensures that the Write Protect Detector assembly is functioning properly. It should be performed anytime there is a problem with the write protect feature or when the Write Protect Detector Assembly has been removed or replaced.

-Adjustment-

1. Set the oscilloscope controls as follows:

   sweep: 5 msec/div
   sensitivity: .2 volts/div
   input: DC
   display: A
   trigger: auto

4. Connect the A-channel probe to U25 pin 8. See Figure 5-4: Disc Drive Board.

3. Insert a disc with the WRITE tab removed (Alignment Disc may be used) into the drive, and close the drive door.

4. Check that the signal at U25 pin 8 is greater than 4.5 volts. If it is, skip to step 7. If not continue.

5. Loosen the screw securing the Write Protect Detector Assembly and position the assembly until a maximum amplitude is obtained at U25 pin 8. The maximum must be at least 3.5 volts. If this cannot not be obtained, replace the Write Protect Detector Assembly.

6. Carefully tighten the assembly mounting screw.

7. Remove the disc and insert a disc with a WRITE tab installed. (scratch disc may be used)

8. Check that the signal at U25 pin 8 is low.

9. Remove the disc.

Index Pulse Test

This test checks the operation of the Index Detector and LED Assemblies. It should be performed anytime there is a problem reading one size disc and not the other, i.e. 1.2 megabyte and .5 megabyte, or when the Detector or LED Assembly is replaced.

-Test-

1. Set the oscilloscope controls as follows:

   sweep: 2 msec/div
   sensitivity: .2 volts/div
   input: DC
   display: A
   trigger: normal, internal, +

2. Connect the A-channel probe to TP INDEX. See Figure 5-4: Disc Drive Board.

3. Insert the Alignment Disc, and close the drive door.

4. Check that two pulses are present as shown in the figure. The amplitude of the pulses should be approximately 4.0 volts.

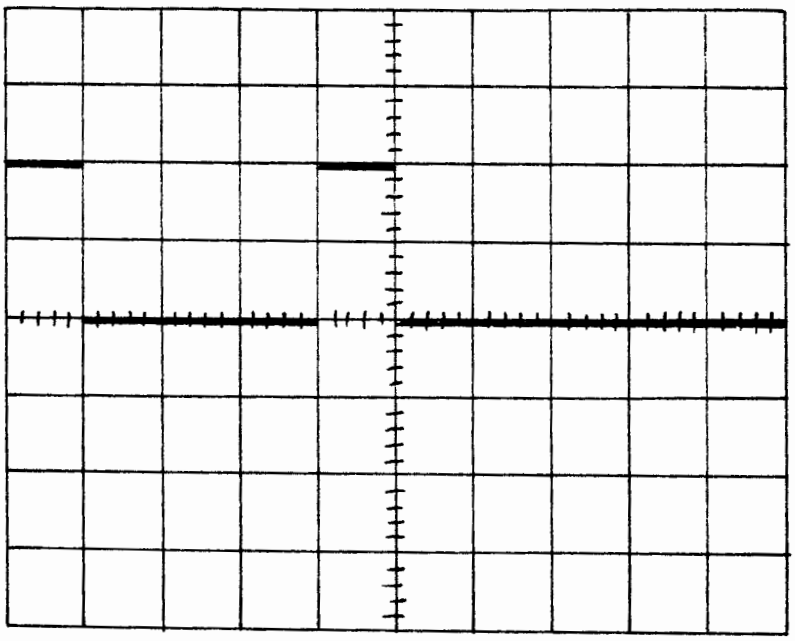


Figure 5-17: Index Pulse waveform

Cartridge Guide Adjustment

This adjustment positions the cartridge guide so that it will accomodate a standard size disc. It should be performed anytime the door latch plate is removed from the cartridge guide or if there is a problem installing or removing a disc.

-Adjustment-

1. Insert the #2 end of the Cartridge Guide Adjustment Tool through the adjustment hole in the cartridge guide and screw it hand tight into the base casting.

2. Loosen the two screws holding the cartridge guide to the door latch plate, if they are not already loose.

3. Position the door handle to the latched position and hold it in place by applying a slight downward pressure.

4. Tighten the two screws that hold the cartridge guide to the latch plate.

5. Remove the Cartridge Guide Adjustment Tool.

6. Rotate the spindle and check that it turns freely.

7. Adjust the cartridge guide limiter by loosening its mounting screw and positioning the limiter lightly against the base casting. Tighten the mounting screw.

8. Insert a disc into the drive and check for proper door open and close operation, i.e. no binding or hesitation.

Disc Controller Self-Test

The Disc Controller Self-Test firmware checks the basic operation of the Controller Board and drive subsystems by performing comprehensive tests and comparing these results with expected values. The self-test routines are divided into three functional areas: standard, read, and write.

The Controller Self-Test includes a test of all the LEDs used to display the test code. When the self-test is initiated, all of the LEDs will come on signifying the beginning of the test. After this, each LED starting with the MSB will light and then extinguish. This sequence is the LED Pattern Test and will show that each LED is operating.

The controls and indicators used with the Disc Controller Self-Test are located on the Disc Controller Board, A10. Figure 5-18: Controller Self-Test Controls and Indicators shows the location and name of the switches and indicators used when performing the self-test.

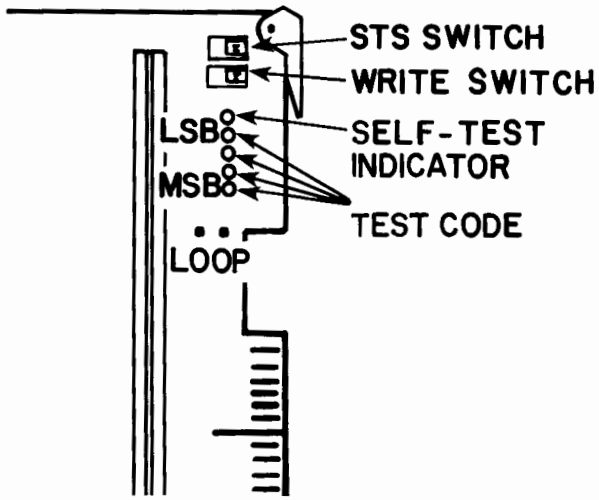


Figure 5-18: Controller Self-Test Controls and Indictors

1. Disconnect the Peripheral Interface Board (blu) from the Disc Controller Board (yel) by disconnecting the Interface/Controller Ribbon Cable (W18). See Figure 3-2: Condensed Wiring Diagram.

2. Instal a scratch disc which has been initialized and has no defective tracks into each disc drive to be tested.

CAUTION

The WRITE/READ and WRITE/VERIFY tests are destructive to the disc initialization. Do not use a disc which contains programs or data when performing these two tests. Use only a scratch disc with zero defective tracks when performing any of the Disc Controller self-tests.

3. Select and perform the desired test described in Table 5-1: Disc Controller Self-Test Procedures.

Table 5-1 shows the 3-step procedures used to perform the desired controller test. These steps must be performed in the sequence shown.

Table 5-1: Disc Controller Self-Test Procedures

Step1** Loop Pin	Step2* WRITE switch	Step3* STS switch	ACTION***
off	off	press/ release	Perform STANDARD SELF-TEST only and then go on-line. Pause 20 seconds if soft error occurs before going on-line.
off	off	press/ hold	Perform READ-ONLY TEST on incrementing tracks with .5 second delay between increments. Wait for release of STS switch if error occurs before going on-line.
off	on	press/ hold	Perform WRITE/READ TEST on incrementing tracks with .5 second delay between increments. Wait for release of STS switch if error occurs before going on-line.
on**	off	press/ release	Perform STANDARD SELF-TEST REPETITIVELY. Pause 20 seconds if error occurs before repeating standard self-test.
on**	on	press/ release	Perform WRITE/READ TEST REPETITIVELY on incrementing tracks with no wait between increments. Pause 20 seconds if error occurs before continuing test.
on**	off	press/ hold	Perform READ ONLY TEST REPETITIVELY on incrementing tracks with no wait between increments. Pause .2 seconds if error occurs before repeating failed test.
on**	on	press/ hold	Repetetively performs WRITE/VERIFY TEST on incrementing tracks with no wait between increments. Pause .2 seconds if an error occurs before repeating failed test.

*After performing Step3, the WRITE switch is no longer an active part of the test sequence. (WRITE switch=don't care)

**Tests performed with a loop on the loop pin are designed for factory and component level repair. Installation of the loop is not recommended for field use.

***The Standard Self-Test is always performed as part of the Read or Write/Read tests.

Self-Test Codes

The Controller Self-Test Codes indicate when the self-test is in progress and what test is being performed. The self-test indicator (see Figures 5-18 and 5-19) is on anytime the self-test is running. The other four LEDs represent a code for the particular test that is in progress or has failed.

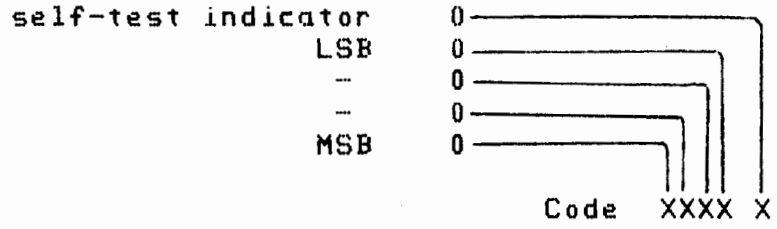


Figure 5-19: Self-Test Indicator to Code Conversion

Table 5-2: Self-Test Codes

Code	Explanation
0001 0*	End of self-test: no errors, Peripheral Interface Board connected to controller
0000 1*	End of self-test: no errors, Peripheral Interface Board not connected to controller

Table 5-2 (continued)

Code	Explanation
0001 1	Controller ROM Test (upper left byte)
0010 1	Controller ROM Test (upper right byte)
0011 1	Controller ROM Test (lower left byte)
0100 1	Controller ROM Test (lower right byte)
0101 1	Controller RAM Pattern Test (left byte)
0110 1	Controller RAM Pattern Test (right byte)
0111 1	Controller PHI Chip Test
1000 1	Controller Timeout and Overrrun Test
1001 1	Controller Data Loop and Margin Error Logic Test
1010 1	Controller CRC Logic Test
1011 1	Drive and Controller Board Drive Logic Test
1100 1	Rotational Timing Test(disc must be installed)
1101 1	Data Recording and Formating (Write Test)
1110 1	Data Reading (Read Test)
1111 1	Controller MCC, PHI, and RAM Logic Test

*When the Controller is connected to a disc drive, after a successful self-test the controller will automatically go on-line. When this happens the LEDs will flash through code 0000 1 and stop at code 0001 0 indicating that the drive system is on-line.

Table of Contents

Parts Ordering Information

Five digit part numbers ending in "SHU" are manufacturer's part numbers. They may be ordered from:

Shugart Associates
Sunnyvale, California 94086

408-733-0100

All other part numbers are Hewlett-Packard, and may be ordered through your local Hewlett-Packard Sales and Service Office.

When ordering parts, always provide the following information:

model and serial number

part number

complete description

Documentation and Support**

HP Part Number	Description
45251-87901*	System Documentation Kit
45251-90000	System Operation Guide
45251-90005	QUERY Operation Guide
45251-87902	Programming Manuals Kit
45251-87902	Programming Manuals Kit
45251-90015	BASIC Programming Manual Pages
45251-90020	IMAGE Programming
45251-90021	QUERY Programming
45251-90022	Report Writer Programming
45251-90023	FORMS Programming
45251-90024	SORT Programming
45251-90045	System Index
45251-90050	Syntax Reference
9282-0685	Binder, BASIC
9282-0686	Binder, System Software
45251-90019	Tabset
45251-87903	Site Selection Kit
45251-90040	Site Selection Guide
45251-90041	Site Selection Folder
45251-62500	Quick Reference Kit
45251-90070	Card Set
9282-0688	Binder, Quick Reference
9222-0654	Disc Envelope
45251-90001	TIO Programming Manual
45251-87904*	Service Manual Kit
45251-90030	On-Site Service Manual
45251-90035	On-Site Service Manual Pages
9282-0702	Binder, On-Site Service Manual
45251-90037	Tabset, On-Site Service Manual
45251-90060	Service Reference Manual
45251-90065	Service Reference Manual Pages
9282-0687	Binder, Service Reference Mnl
45251-90067	Tabset, Service Reference Mnl
45120-90065	HP45120A Asynchronous Serial Interrface Installation Manual

45250-67801	Product Support Package
45251-13000	Operating System Disc
45251-90071	Operating System Card
45000-15000	System Support Disc
9164-0098	Alignment Disc
1150-1310	Cartridge Guide Adjustment Tool
1535-3875	Bail Gauge
1540-0177	Plastic Parts Container
1540-0557	Carry Case, PSP
45000-68809	Installation Hardware Kit
9164-0099	Disc, Dbl-side
9164-0100	Disc, Pkg-10 Dbl-side
45251-10100	Disc, Initialized Dbl-side
7120-7497	Overlay, SFK
8710-1179	Puller, Keycap

*included with Product Support Package
**Check with your local Sales Office for information on availability of translated manuals.

Recommended Field Service Inventory

Part Number	Description	Qty
	All Exchange Circuit Boards. See Circuit Boards parts list.	
	Disc Drive Exchange Assembly. See Disc Drive Assembly, Figure 6-9 parts list.	
1540-0535	Case, FSI Carry (hlds 15 Bd Cartons)	1
9211-3005	Carton, HP 250 Board	0
6010-0695	Paint, Touch-up Beige	1
6010-0694	Paint, Touch-up Cocoa Brown	1
45000-66518	Filter Board, new	1
0960-0502	Tripler, Voltage	1
45000-66512	Softkey Board, new	1
8120-2737	Cable, Interface/Controller Ribbon	1
45000-61602	Cable, Disc Controller	1
45000-61615	Cable, Keyboard Matrix	1
45000-60109	Assembly, Key Switch	1
45000-66519	Terminator Board, new	1
2110-0012	Fuse, .5A 250V	5
2110-0030	Fuse, 5A	5
2110-0459	Fuse, 20A	5
45000-61601	Cable, Keyboard	1

Circuit Boards

HP Part Number	Description
45000-66501	CRT Board, new
45000-69501	CRT Board, exchange
1200-0816	Connector, CRT Neck
9100-3859	Xfmr, Potcore
9100-4089	Xfmr, High Voltage
1250-0835	Connector, RF SMC (A1J1)
1251-5137	Connector, 3-pin (A1J2)
1251-5238	Connector, 10-pin (A1J3)
1251-5136	Connector, 5-pin (A1J4)
1251-5184	Connector, 7-pin (A1J5)
45000-66504	Mother Board, new
1251-2915	Connector, 2x25 female (A4J1/J4)
45000-66505	Processor Board (violet), new
45000-69505	Processor Board (violet), exchange
1990-0531	LED, 7-segment
3100-3434	Switch, 16-position
3101-2256	Switch, Pushbutton 23-020-003
0410-0661	Crystal
45000-66506	Display Logic Board (orange), new
45000-69506	Display Logic Board (orange), exchange
0410-1114	Crystal, Quartz
3100-3435	Switch, 10-position
45000-66507	Peripheral Interface Board (blue), new
45000-69507	Peripheral Interface Board (blue), exchg
0410-1101	Crystal, Quartz
2110-0568	Fuse, 4A 125V
1251-3283	Connector, 24 pin female (A7J1)
1251-5068	Connector, 2x17 male (A7J2)
45000-66508	Keyboard Logic Board (gray), new
45000-69508	Keyboard Logic Board (gray), exchange
45000-66509	Keyboard Matrix Board, new
45000-69509	Keyboard Matrix Board, exchange
1460-1519	Spacebar
1460-1617	Key, 3 PL
3101-2133	Switch, Dual Force (4ea)
3101-2253	Switch, Straight Shank (53ea)
3101-2254	Switch, Angle Shank (28ea)
3101-2255	Switch, Alt. Action (1ea)
4342-0039	Strip, Felt

Circuit Boards (continued)

HP Part Number	Description
45000-66510	Disc Controller Board (yellow), new
45000-69510	Disc Controller Board (yellow), exchange
0410-1031	Crystal, Quartz
1990-0622	LED, Visible
3101-2256	Switch, Pushbutton 23-020-003
3101-2259	Switch, Slide
1251-5068	Connector, 2x17 male (A10J2)
45000-66511	Power Supply Board (black), new
45000-69511	Power Supply Board (black), exchange
2110-0054	Fuse, 15A 250V
2110-0269	Holder, Fuse (2ea)
1251-4278	Connector, male (A11J2)
45000-66512	Softkey Board, new
1251-4245	Connector, 2-pin male
1251-5121	Connector, 11-pin male
5060-9436	Switch, PC Pushbutton (8ea)
45000-66513	64K-Byte Memory Board (red), new
45000-69513	64K-Byte Memory Board (red), exchange
3101-1860	Switch, Slide S1A-NS (2ea)
45000-66514	Block Switch Board (green), new
45000-69514	Block Switch Board (green), exchange
45000-66517	Disc Front Board, new
1990-0523	LED, visible green
1990-0524	LED, visible yellow
1251-5043	Connector, 5-pin female
1251-4182	Contact, Connector female
0380-0589	Spacer, Round
45000-66518	Filter Board, new
1251-5098	Contact, Comming (2ea)
1251-4245	Connector, 2-pin male (2ea)
2110-0012	Fuse, .5A 250V
2110-0269	Holder, Fuse (2ea)
0160-0576	C-F .1 uF 50V
0180-0578	C-F 750 uF 40V
0683-5125	R-F 5100 ohm .05
1901-0743	Diode 400V 1A
4330-0496	Insulator, Bead Glass
4330-0952	Bead, Glass Insulator

Circuit Boards (continued)

HP Part Number	Description
45000-66519	Terminator Board, new
0160-0576	C-F .1 uF 50V
0683-1015	R-F 100 ohm .05
45000-66523	32K-Byte Memory Board (red), new
45000-69523	32K-Byte Memory Board (red), exchange
3101-1860	Switch, Slide 51A-NS (1ea)
45000-66525	Disc Drive Board, new
3101-1951	Switch, Slide DP3T NS
1251-4008	Connector, 8-pin male (A25J1)
1251-4338	Connector, 5-pin male (A25J2,J4)
1251-4280	Connector, 2x3 (A25J5)
1251-5174	Connector, Receptacle (A25J6)

Condensed Wiring Diagram, Figure 3-2

Ref.	Part Number	Description
	0360-1893	Block, Barrier 9-position
	9100-4054	Xfmr, Main Power w/o cables
	2110-0012	Fuse, .5A 250V
F1	2110-0459	Fuse, 20A
F2,3	2110-0030	Fuse, 5A
	2110-0550	Spring, Fuseholder
	2110-0549	Contact, Fuseholder
	2110-0548	Cap, Fuseholder
	2110-0547	Body, Fuseholder
	1251-5123	Connector, Commoning 10-point
	1251-5122	Connector, Commoning 15-point
C	0160-4413	C-F .6 uF .10
R	0686-3345	R-F 330K ohm .5 .5W
W1		Cable, AC Power
	8120-0651	Europe, 220V/240V
	8120-1351	United Kingdom, 220V
	8120-1369	Australia, 220V
	8120-2667	United States, 115V
	8120-0698	United States, 220V/240V
	8120-0651	France, 110V/120V
W2	45000-61614	Cable, On/Off
W3	45000-61612	Cable, AC Power Distribution
W4	45000-61607	Cable, CRT Speaker
W5	45000-61610	Cable, Disc AC Power
W6	45000-61611	Cable, Disc DC Power
W7	45000-61613	Cable, DC Power Distribution
W8	8120-2736	Cable, Disc Interconnect Ribbon
W9	45000-61602	Cable, Disc Controller
W10	45000-61608	Cable, CRT Intensity
W11	45000-61617	Cable, 24 VDC Internal
W12	45000-61619	Cable, System AC Power Distribution
W13	45120-61600	Cable, Asynchronous Board Interconnect
W14	45000-61601	Cable, Keyboard
W15	45000-61605	Cable, CRT Assembly
W16	45000-61615	Cable, Keyboard Matrix
W17	45000-61616	Cable, Display
W18	8120-2737	Cable, Interface/Controller Ribbon
W19	8120-1833	Cable, Peripheral Interface Internal
W20	8120-2720	Cable, Peripheral Interface External (3M)
W21	45000-61618	Cable, 24 VDC External

Tub Assembly, Figure 6-1

Ref.	Part Number	Description
1	45000-68811	Disc Drive Assembly w/o calbes, new
	45000-69811	Disc Drive Assembly w/o cables, exchange
2	45000-60101	Frame, Card Cage Assembly
3	4040-1395	Drawer
4	1530-2132	Frame, Tube Assembly
5	45000-64408	Panel, Accent Standard
	45000-64404	Panel, Accent Marine Blue #80
	45000-64405	Panel, Accent Leaf Green #81
	45000-64406	Panel, Accent Sweet Potato #82
	45000-64407	Panel, Accent Leaf Gold #83
6	4040-1367	Handle, Door
7	4040-1368	Slat, Door
8	1494-0036	Slide Assembly, Top
9	1494-0035	Slide Assembly, Bottom
10	6960-0079	Plug, Plastic
11	45000-04114	Retainer, Board
12	45000-04704	Cable Tray, Card Cage
13	45000-04109	Plate, Retaining
14	0590-0804	Nut, Clip
15	3030-0706	Screw, Allen #10x.75
16	0403-0246	Pad, Leveling

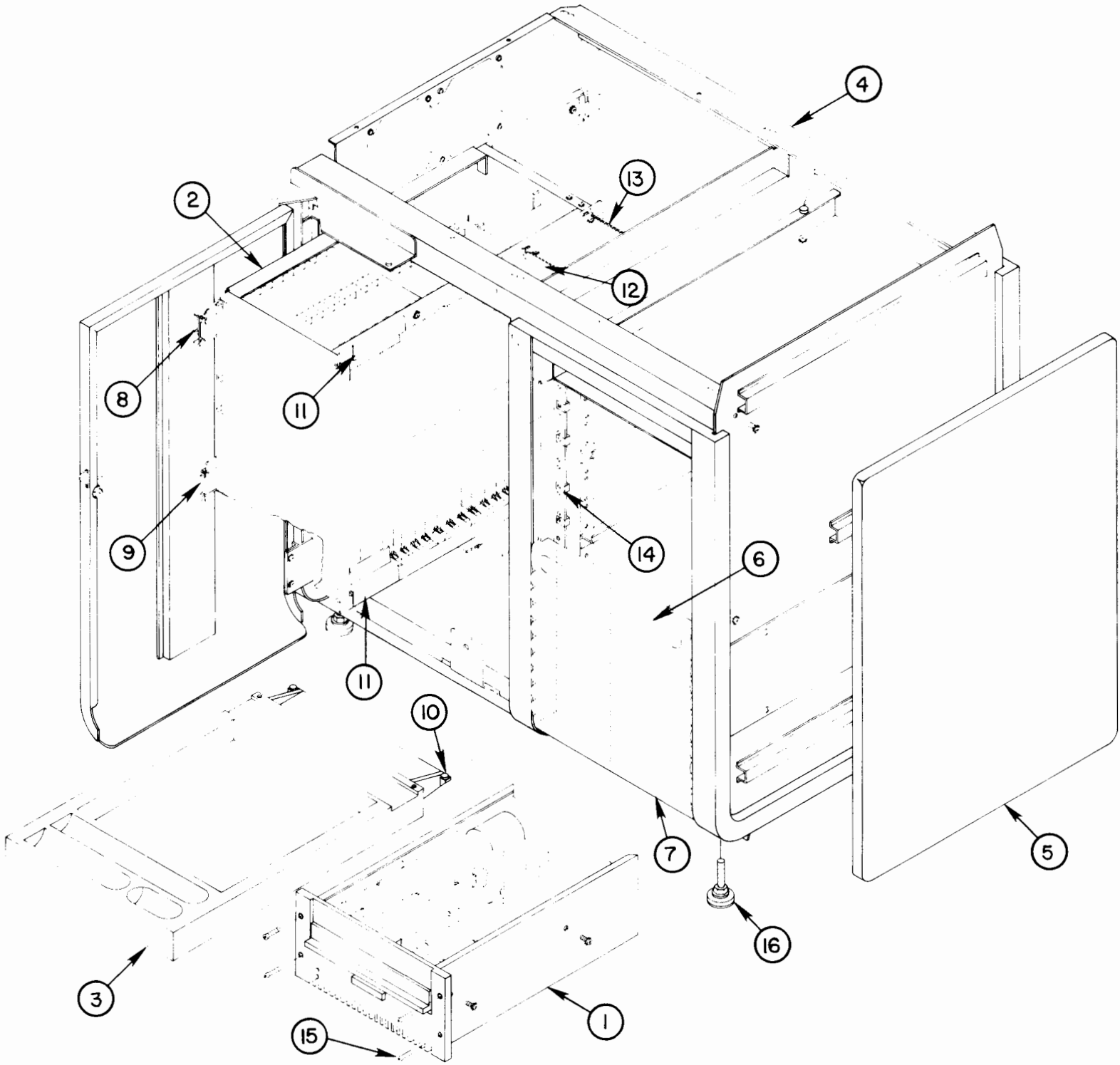


Figure 6-1: Tub Assembly

Tub Assembly, Figure 6-2

Ref.	Part Number	Description
1	3160-0262	Fan, 115V
2	09101-04601	Screen, Filter
3	4040-1394	Support, 3rd Disc Drive
4	0360-1893	Block, Barrier 9-position
5	45000-01209	Fan Bracker, Disc
6	4040-1403	Inductor, Ram Air
7	45000-60103	Box, Chassis Transformer
8	8120-1833	Cable, Peripheral Interface Internal
9	4040-1430	Shield, Barrier Block
10	45000-04102	Plate, Upper
11	45000-64402	Cover, Connector Panel
12	45000-04103	Plate, Cover
13	45000-00214	Panel, Cover
14	45000-00107	Lid, Tub
15	45120-00212	Panel, Connector
	45120-00211	Panel, Blank
16	0905-0751	Gasket, Vent
17	45000-04604	Screen, Vent
18	45000-04603	Screen, Vent
19	1530-2144	Slide, Drawer
20	1492-0081	Caster, swvl pl

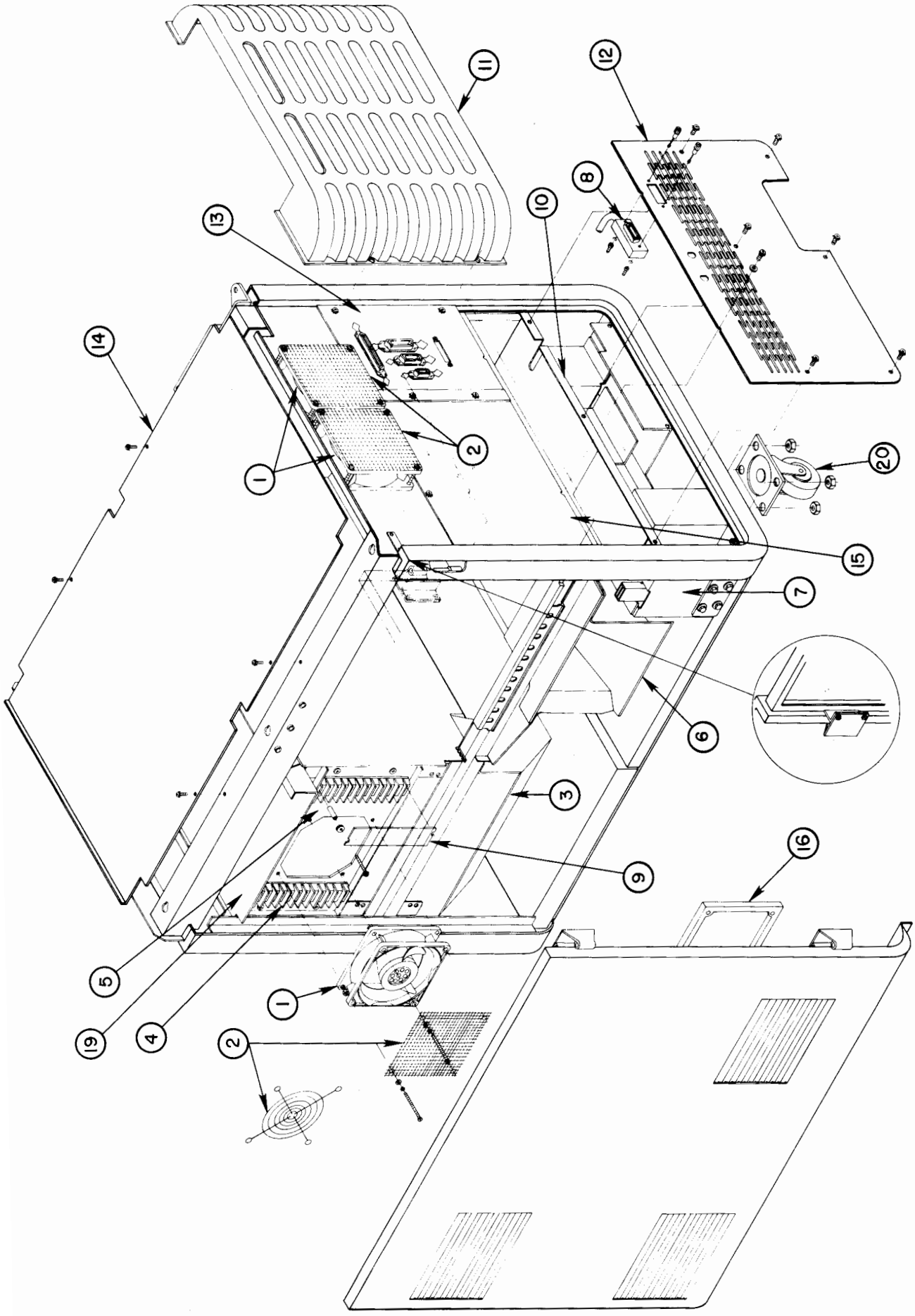


Figure 6-2: Tub Assembly

Primary Power, Figure 6-3

Ref.	Part Number	Description
1	45000-60103	Box, Chassis Xfmr
2	45000-04102	Plate, Upper
3	45000-66518	Filter Board, A18
4	9100-4054	Xfmr, Main Power w/o cables
4	45000-68806	Xfmr, Main Power w/cables
5	45000-60109	Assembly, Keyswitch
6	45000-61614	Cable, On-Off (W2)
7	1251-3805	Connector, 6-Pin Male (W3P1)
8	1251-5122	Connector, Commoning 15-point
9	1400-0290	Bracket, Right Angle
10	0340-0871	Bushing, .375 ID
11	1251-5123	Connector, Commoning 10-point
12		Chassis, Primary Power
	45000-64211	US 110V
	45253-64212	All Others

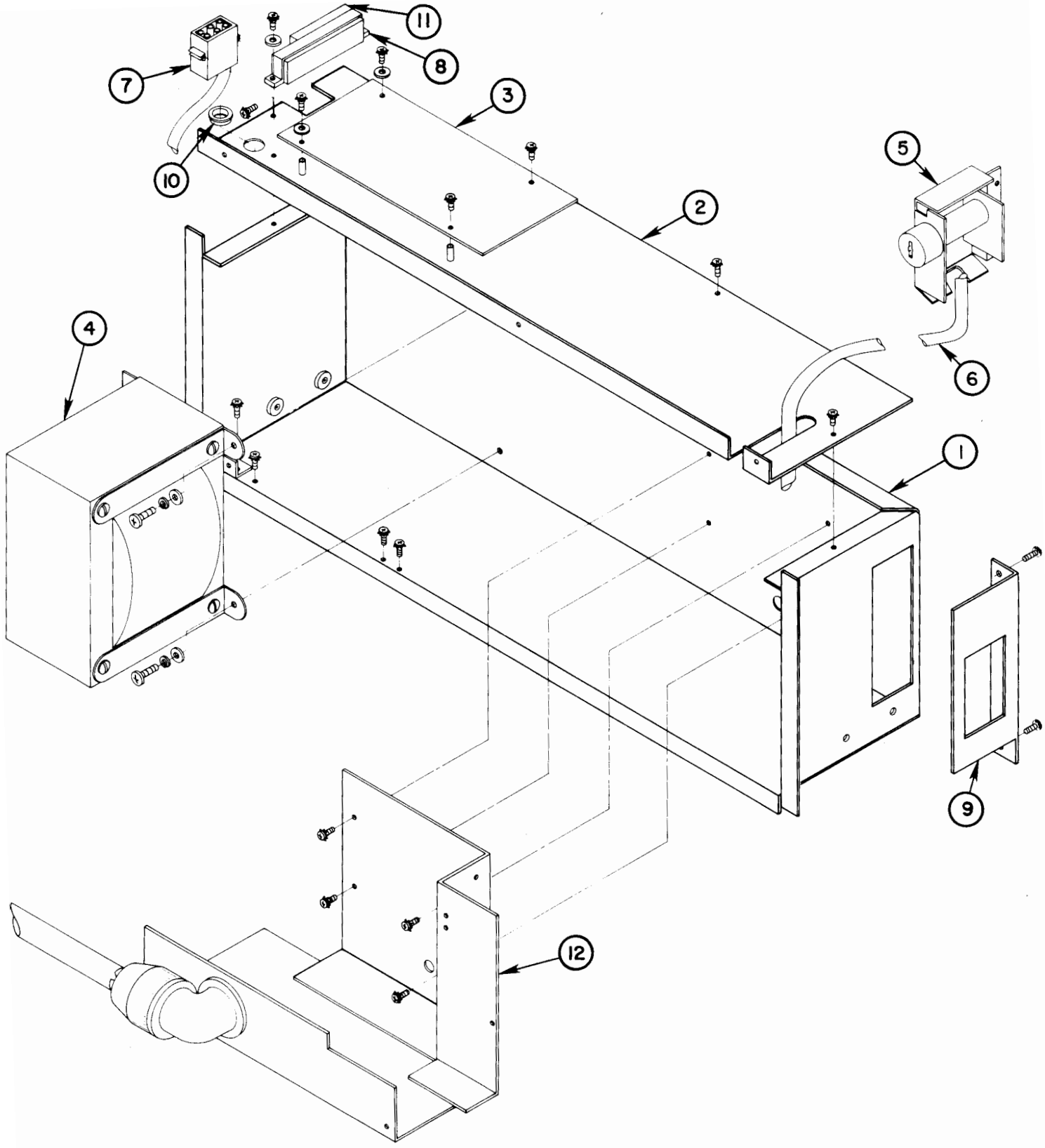


Figure 6-3: Primary Power

Primary Power, Figure 6-4

Ref.	Part Number	Description
		Assembly, Primary Power (1-9 below)
	45251-61211	U.S. 110V/120V
	45251-61212	U.S. 220V/240V
	45252-61211	France 110V
	45252-61612	France 220V
	45253-61212	Germany 220V/240V
	45254-61212	United Kingdom 220V
	45251-61213	Australia 220V
1	3105-0092	Circuit Breaker
2		Chassis, Primary Power
	45000-64211	U.S. 110V/120V
	45253-64212	All Others
3	0360-1912	Block, Terminal 4-position
4	0360-1911	Block, Terminal 2-position
5		Relief, Strain
	0100-1078	U.S. 110V/120V
	0100-1030	All Others
6		Assembly, Power Cable
	8120-2667	U.S. 110V/120V
	8120-0698	U.S. 220V/220V
	8120-0651	Europe 110V/220V/240V
	8120-1351	United Kingdom 220V
	8120-1369	Australia 220V
7	9135-0089	Filter, RFI
8		Relay
	0490-0754	100V/120V
	0490-0755	220V/240V
9		Nut, Strain Relief
	0100-1079	U.S. 110V/120V
	9310-0359	All Others

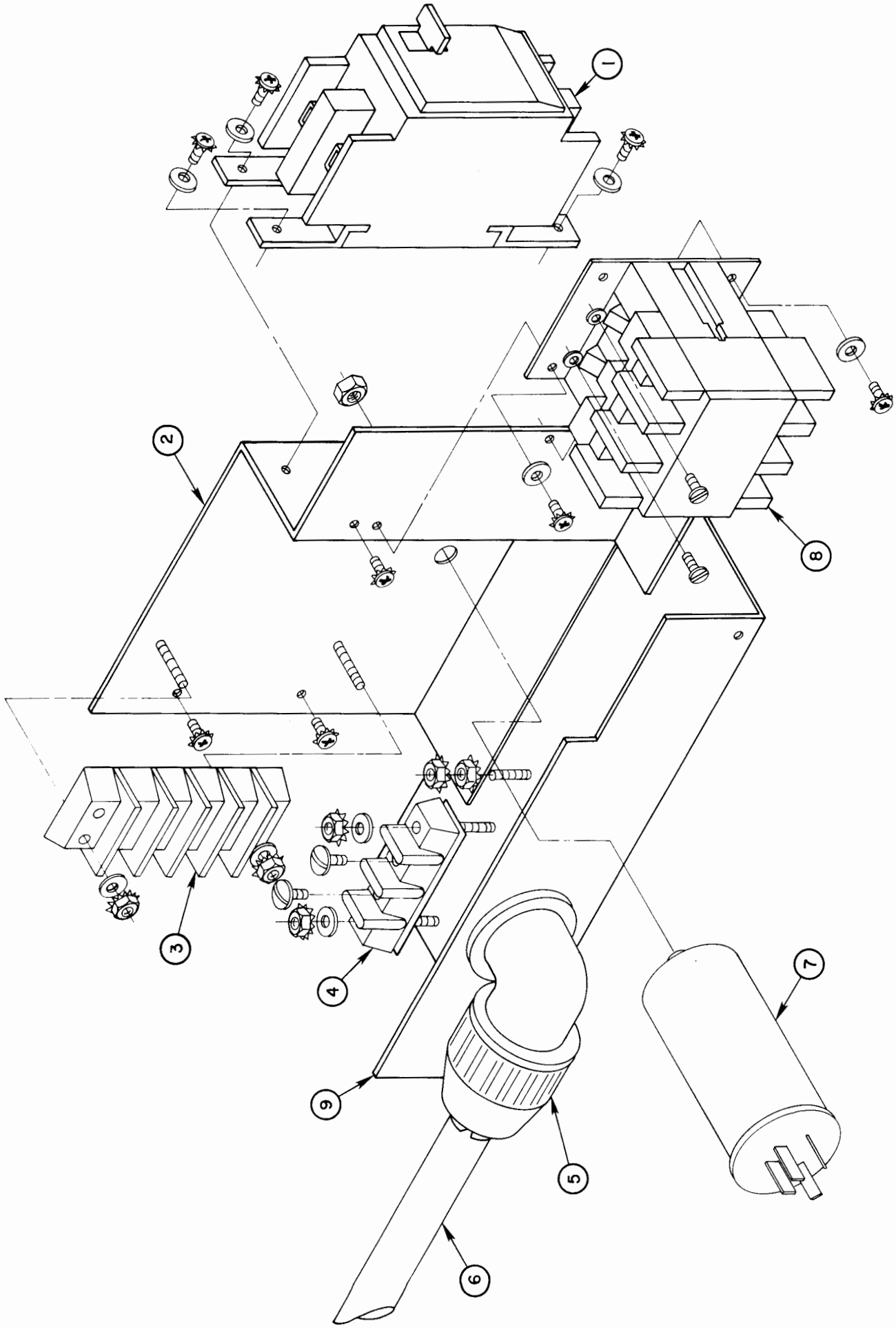


Figure 6-4: Primary Power

System Assembly, Figure 6-5

Ref.	Part Number	Description
1	45000-67905	Assembly, Crt w/cables
2	4040-1388	Top
3	45000-68853	Tubing, Flex (1.5 metre)
4	1530-2106	Leg
5	45000-04705	Retainer, CRT
6	5040-8386	Collar, Locking
7	1390-0445	Stud, Mounting
8	0403-0246	Pad, Leveling
9	1492-0081	Caster, swvl pl
10	45000-68809	Kit, Installation Hardware

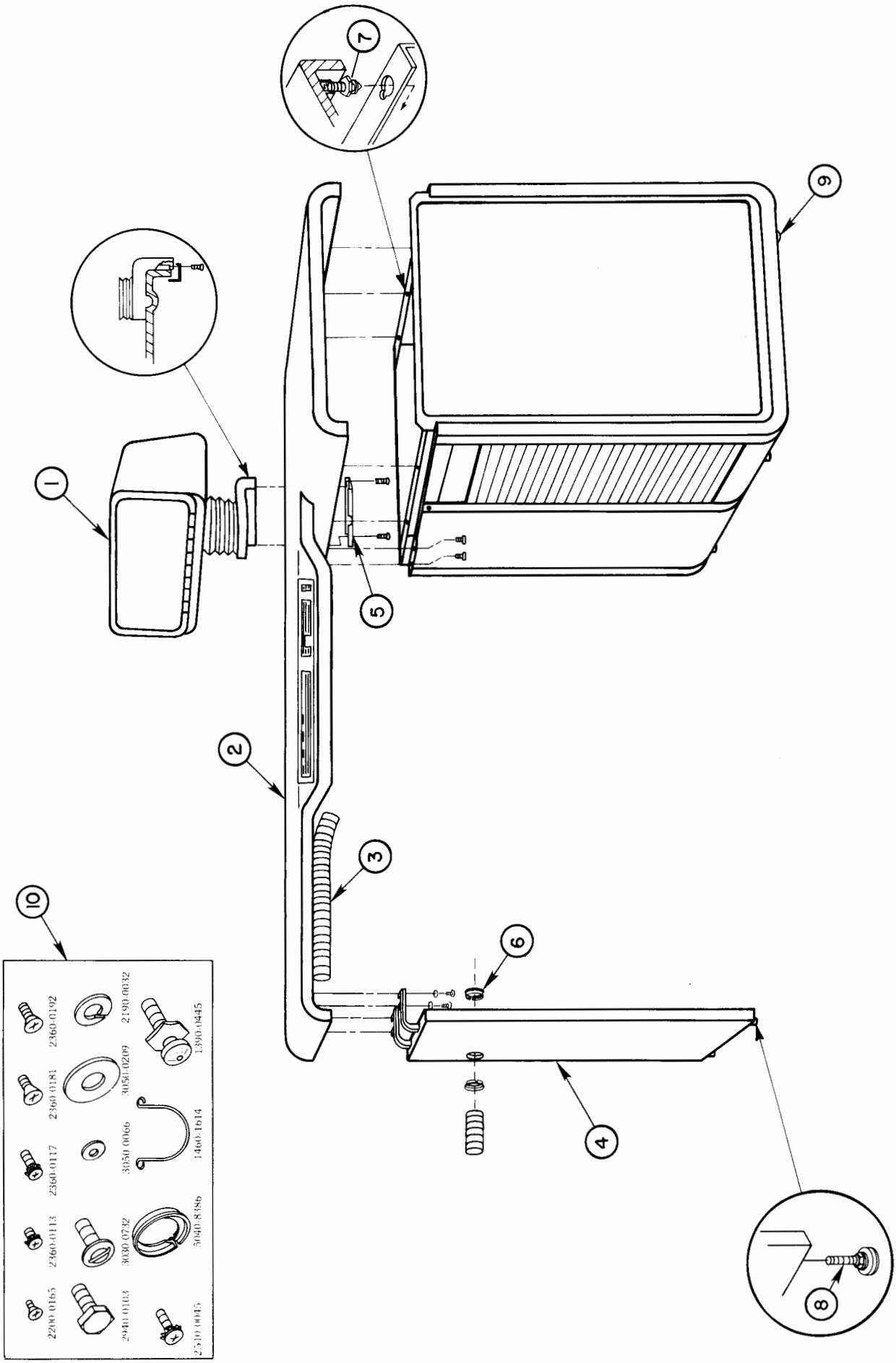


Figure 6-5: System Assembly

Power Supply, Figure 6-6

Ref.	Part Number	Description
1	0180-2409	C-F .018 F 50V
2	0180-2325	C-F 1500 uF 75V
3	1820-0430	IC-LM309K
4	45000-64701	Assembly, Power Supply
5	45000-01105	Heat Sink, High Voltage
6	1826-0123	IC-LM320K-12
7	1826-0202	IC-LM320K-5
8	1854-0063	Xstr, 2N3055
9	1906-0096	Diode, Full-wave Bridge
10	1813-0109	IC-PIC625
11	5040-4527	Insulator, Molded

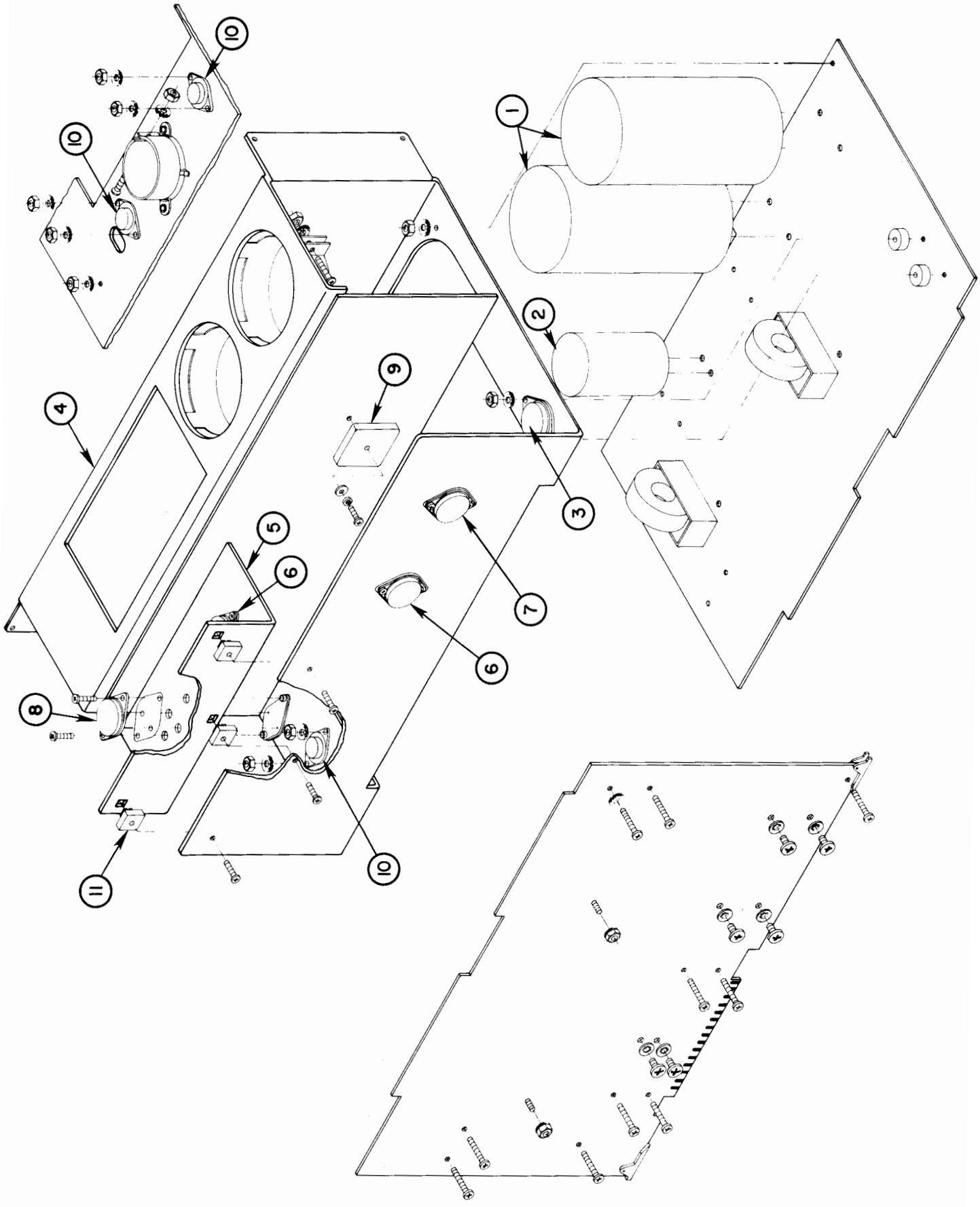


Figure 6-6: Power Supply

Keyboard Assembly, Figure 6-7

Ref.	Part Number	Description
1	45000-60105	Assembly, Keyboard
	0371-0891	Key, 0
	0371-0892	Key, Arrow Up
	0371-0896	Key, Space Bar
1	45000-68812	Assembly, Keyboard, new w/US keys
1	45000-69812	Assembly, Keyboard, exchg w/US keys
1	45000-68813	Assembly, Keyboard, new w/German keys
1	45000-69813	Assembly, Keyboard, exchg w/German keys
2	4040-1385	Bezel, Keyboard
3		Kit, Key
	45251-82500	United States
	45252-82500	France
	45253-82500	Germany
	45254-82500	United Kingdom
	45255-82500	Sweden
	45256-82500	Spain
	45257-82500	Italy
	45258-82500	Japan

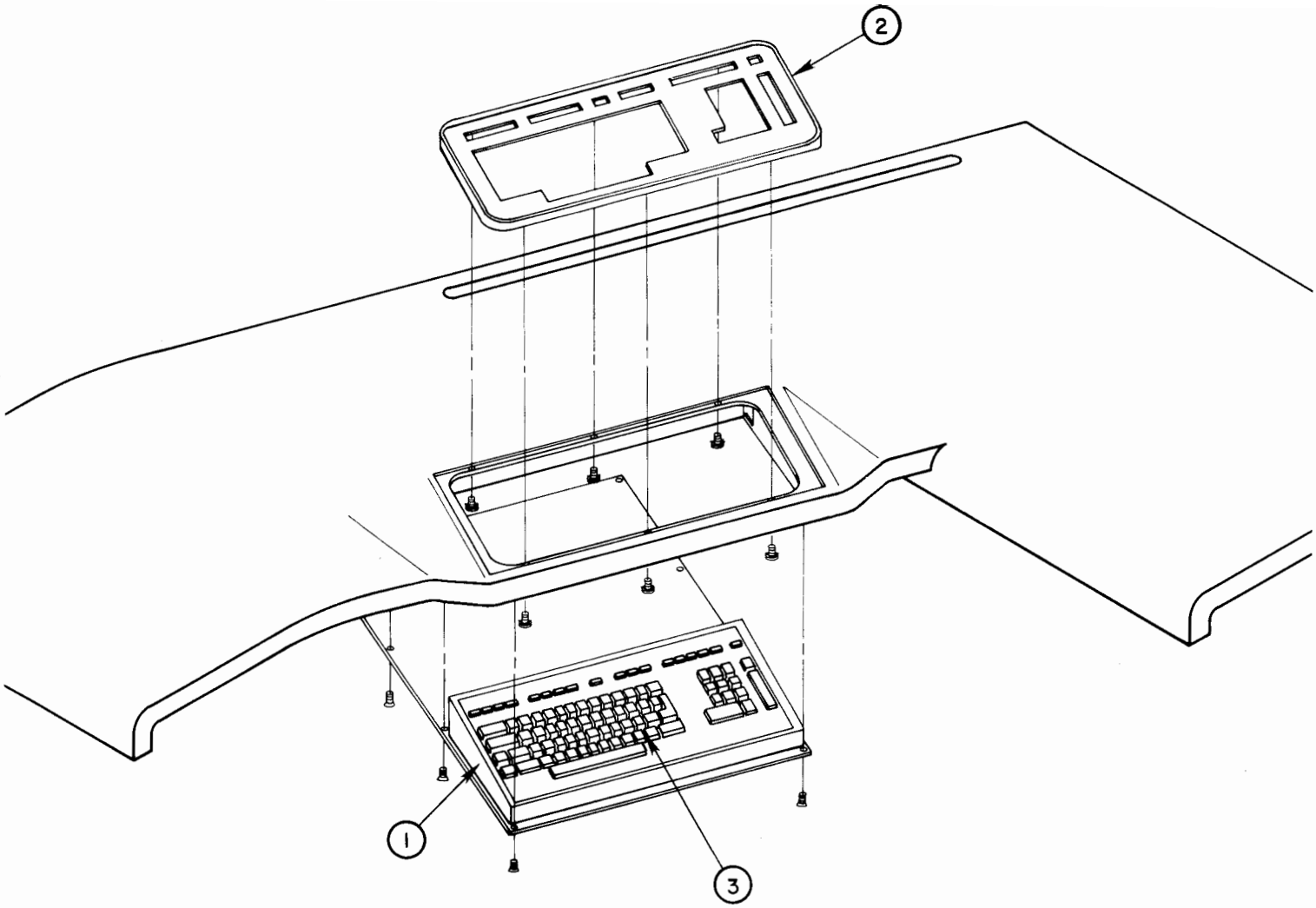


Figure 6-7: Keyboard Assembly

CRT Assembly, Figure 6-8

Ref.	Part Number	Description
1	0960-0502	Tripler
2	1540-0528	Bellows
3	2090-0028	Tube, Cathode Ray
4	45000-66501	Board, CRT A1
5	45000-66512	Board, Softkey A12
6	9100-4079	Yoke, Deflection
7	45000-61607	Assembly, Speaker
8	1530-2066	Hub, CRT
9	1400-0042	Clip, Component
10	0370-1089	Knob, Intensity
11	45000-01217	Clamp, Cable
12	4040-1393	Clamp, CRT
13	3050-0921	Washer, Spring
14	1460-1620	Spring, Music Wire
15	1600-0693	Bar, CRT Support
16	3050-0912	Washer, CRT
17	45000-60104	Assembly, Chassis Mount
18	45000-64105	Cover, CRT
19	4040-1392	Shell, CRT
20	45000-64401	Bezel, painted
21	45000-01203	Bracker, CRT Bezel
22	45000-01202	Bracker, CRT
23	2100-1832	Pot, Intensity p/o 45000-61608 Cable
24	45000-04705	Retainer, CRT
25	45000-01214	Support, Cable
26	0400-0018	Channeling, Nylon
27	1600-0793	Barrier, CRT

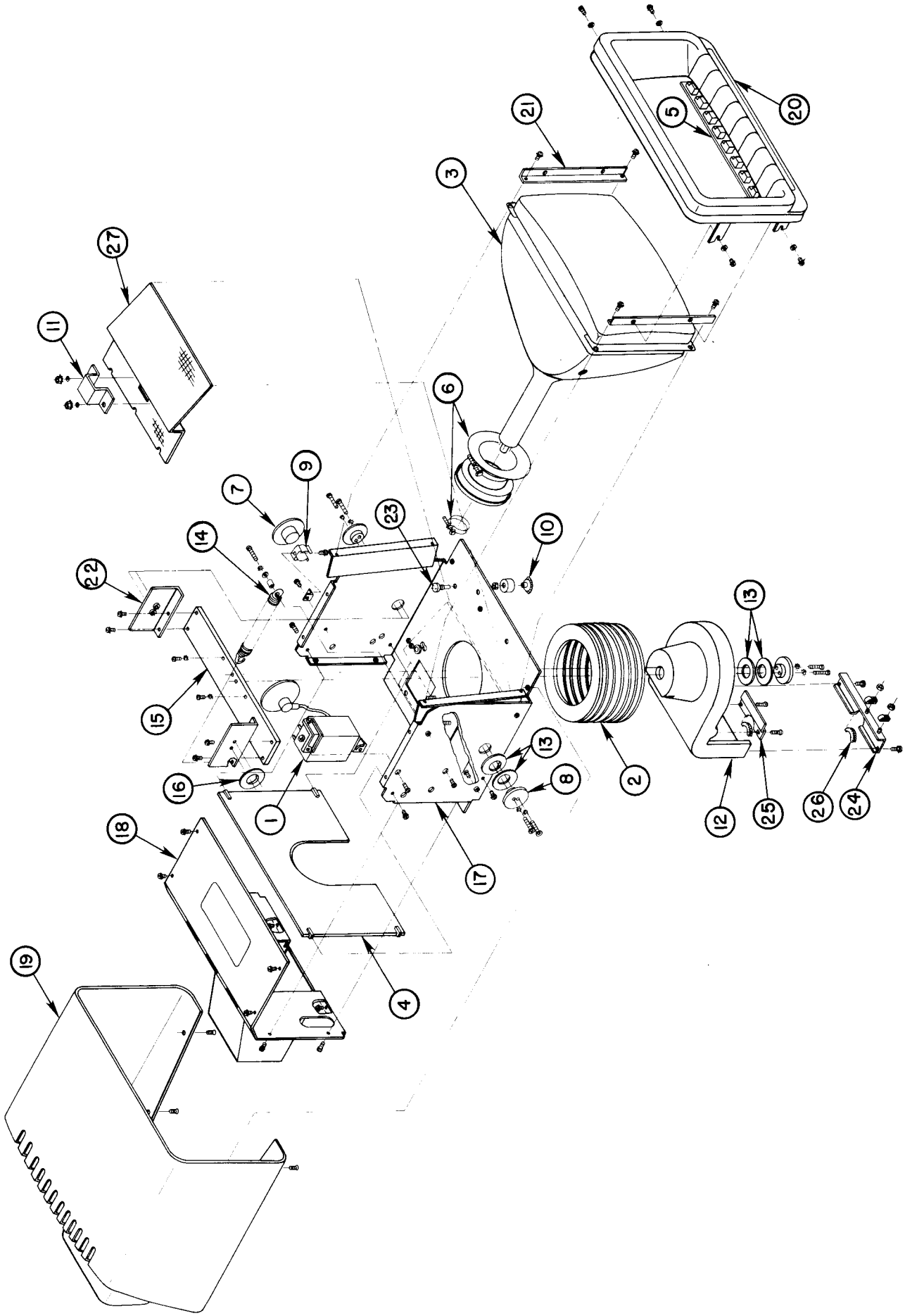


Figure 6-8: CRT Assembly

Disc Drive Assembly, Figure 6-9

Ref.	Part Number	Description
	45000-68811	Disc Drive Assembly, new
	45000-69811	Disc Drive Assembly, exchange
1	50747-SHU	Assembly, Drive Motor, 115V 50/60 Hz
2	1535-3883	Motor, 115V 50/60 Hz
3	1535-3905	Connector, 3-Pin Housing
4	50746-SHU	Bracket
5	1535-3882	Capacitor
6	10148-SHU	Boot
7		Pully, Drive Motor
	1535-3650	50 Hz, 20 mm dia
	50358-SHU	60 Hz, 16 mm dia
8	3030-0278	Screw, Set 6-32 x .125
9	1535-3873	Assembly, Track 0 Detect
10	1535-3887	Assembly, Guide Open
11	1535-3886	Shield, Cover
12	1553-3652	Switch, Door Open
13	1150-1369	Hub Assembly, Spindle
14	1410-0661	Flanged Bearing, Spindle
15	1535-3889	Spring, Spindle
16	1535-3890	Spacer, Spindle-Long
17	1410-0662	Bearing, Spindle
18	1535-3891	Spacer, Spindle-Short
19	1535-3892	Pulley Assembly, Spindle
20	1535-3885	Spring, Bias
21	1535-3906	Limiter
22	1251-4003	Connector Body, Disc Head Cable
23	15677-SHU	Connector Body, Motor Drive Cable

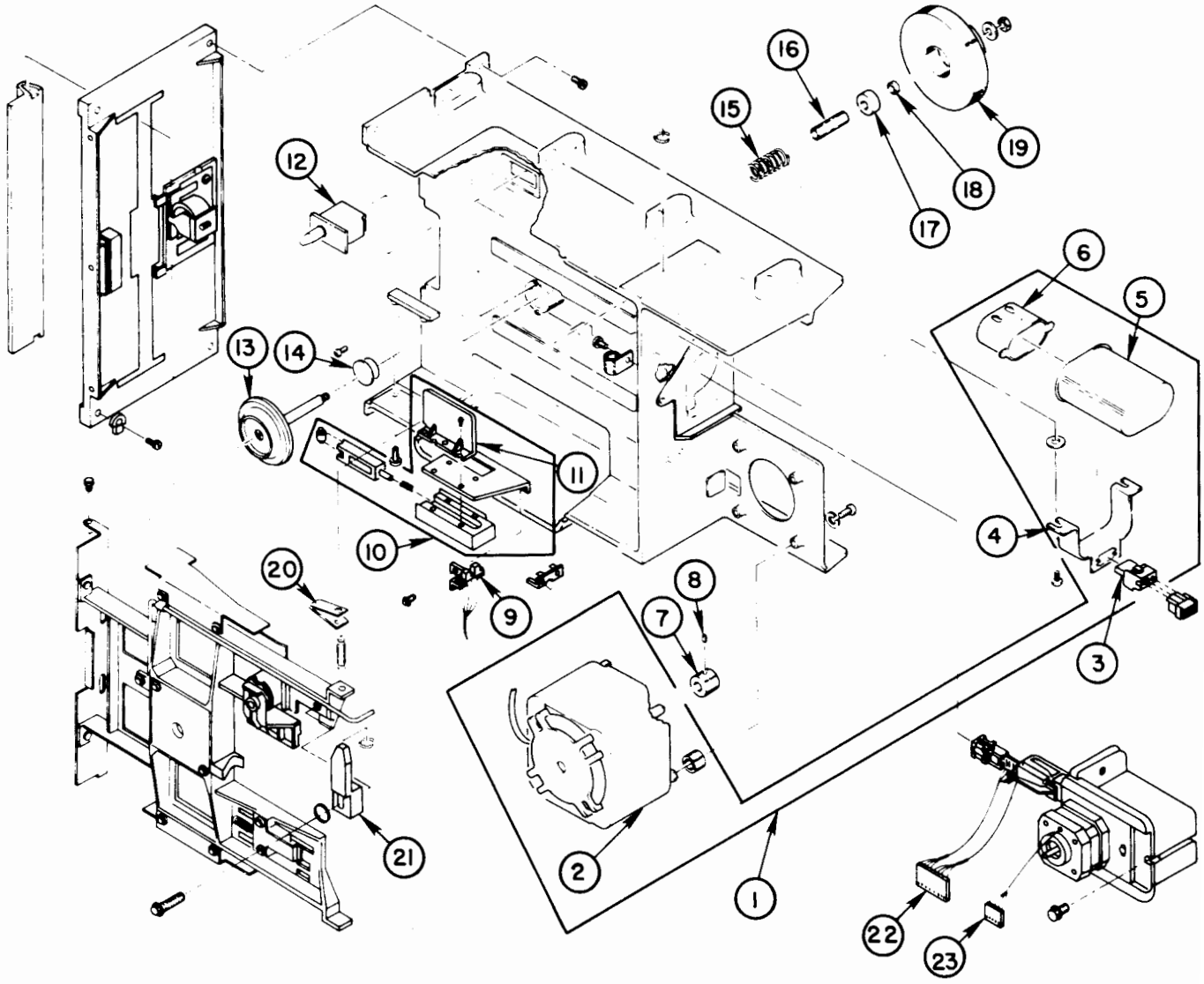


Figure 6-9: Disc Drive Assembly

Disc Drive Assembly, Figure 6-10

Ref.	Part Number	Description
1	45000-66525	Disc Drive Board, new
2	1535-3872	Assembly, Sector/Index Phototransistor
3	1553-3652	Switch, Door Open
4 & 5	88020-80023	Line Frequency Kit
4	1535-3650	50 Hz Drive Pulley, 20mm dia
4	50358-SHU	60 Hz Drive Pulley, 16mm dia
5	1535-3649	50 Hz Drive Belt, white mark
5	1535-3651	60 Hz Drive Belt
6	1535-3903	Resistor Assembly
7	1535-3902	Block, PC Board Connector

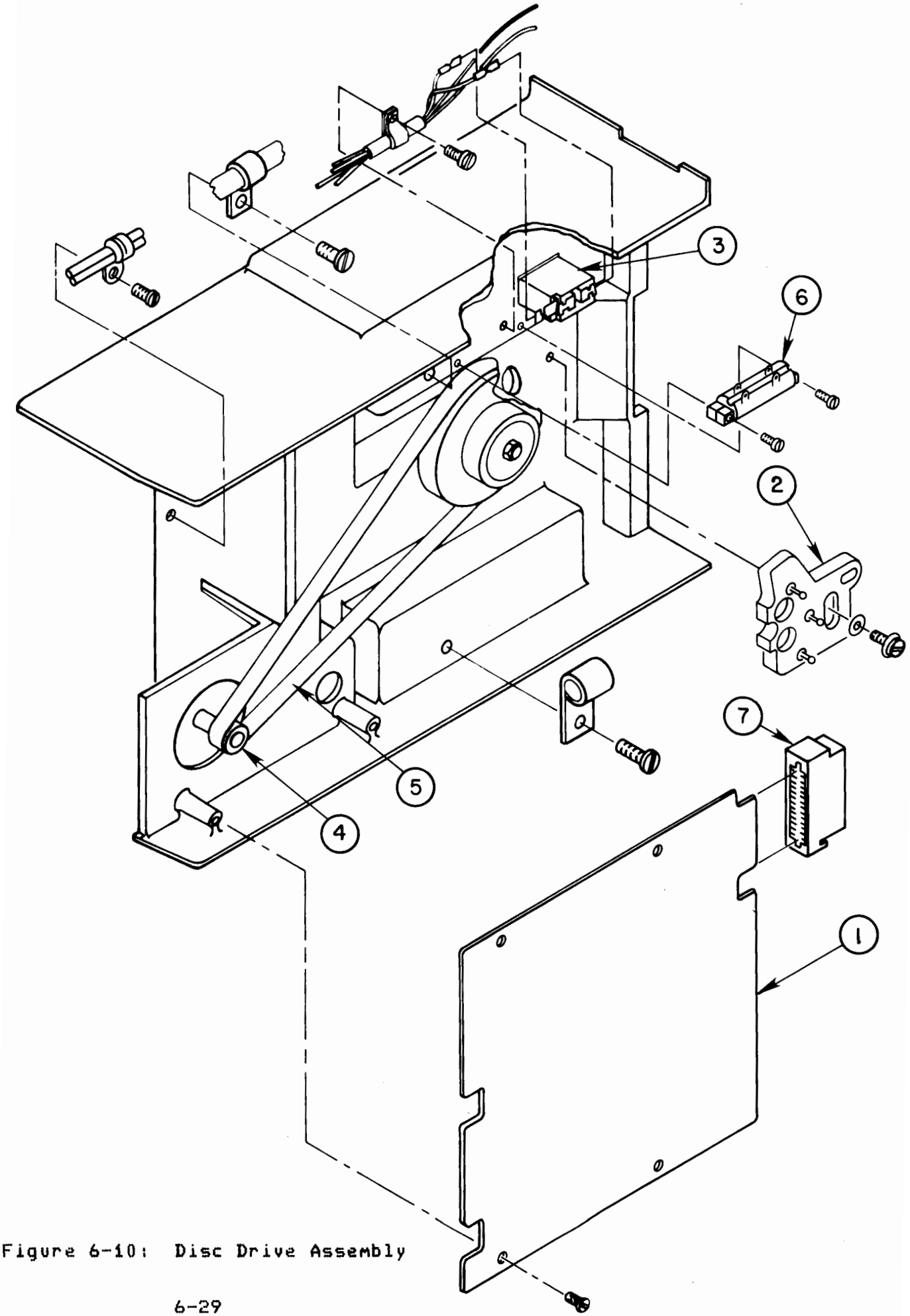


Figure 6-10: Disc Drive Assembly

Disc Drive Assembly, Figure 6-11

Ref.	Part Number	Description
1	1535-3901	Assembly, Head Load Actuator
2	1150-1309	Assembly, Write Protect Detector
3	1535-3871	Assembly, Sector/Index LED
4	50556-SHU	Hook, Spring
5	50609-SHU	Assembly, Ejector
6	1535-3900	Ejector, Spring Clamp
7	1535-3898	Plate, Hub Clamp
8	1535-3899	Spring, Hub Clamp
9	50254-SHU	Assembly, Hub Clamp
10	1535-3894	Latch
11	51305-SHU	Damper Assembly, Head Load Actuator
12	1535-3896	Stripper, Top
13	1535-3897	Stripper, Bottom

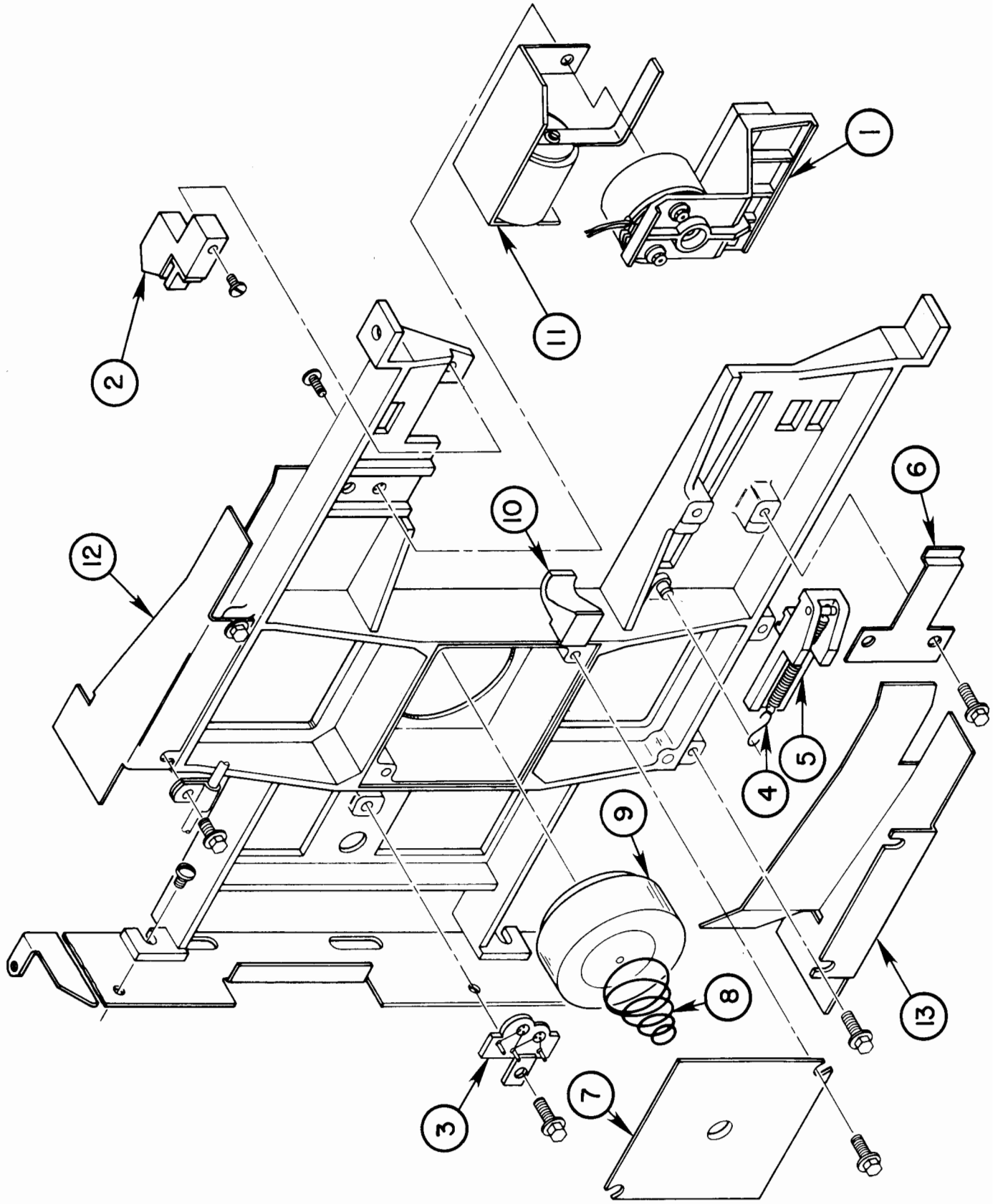


Figure 6-11: Disc Drive Assembly

Disc Drive Assembly, Figure 6-12

Ref.	Part Number	Description
1	50183-SHU	Bumper
2	1535-3893	Spring, Latch Interlock
3	1535-3874	Latch Assembly, Door Lock
4	7120-5171	Face Plate, USA
5	5041-1410	Button, Door Open
6	5041-1408	Door, Drive
7	45000-66517	Disc Front Board

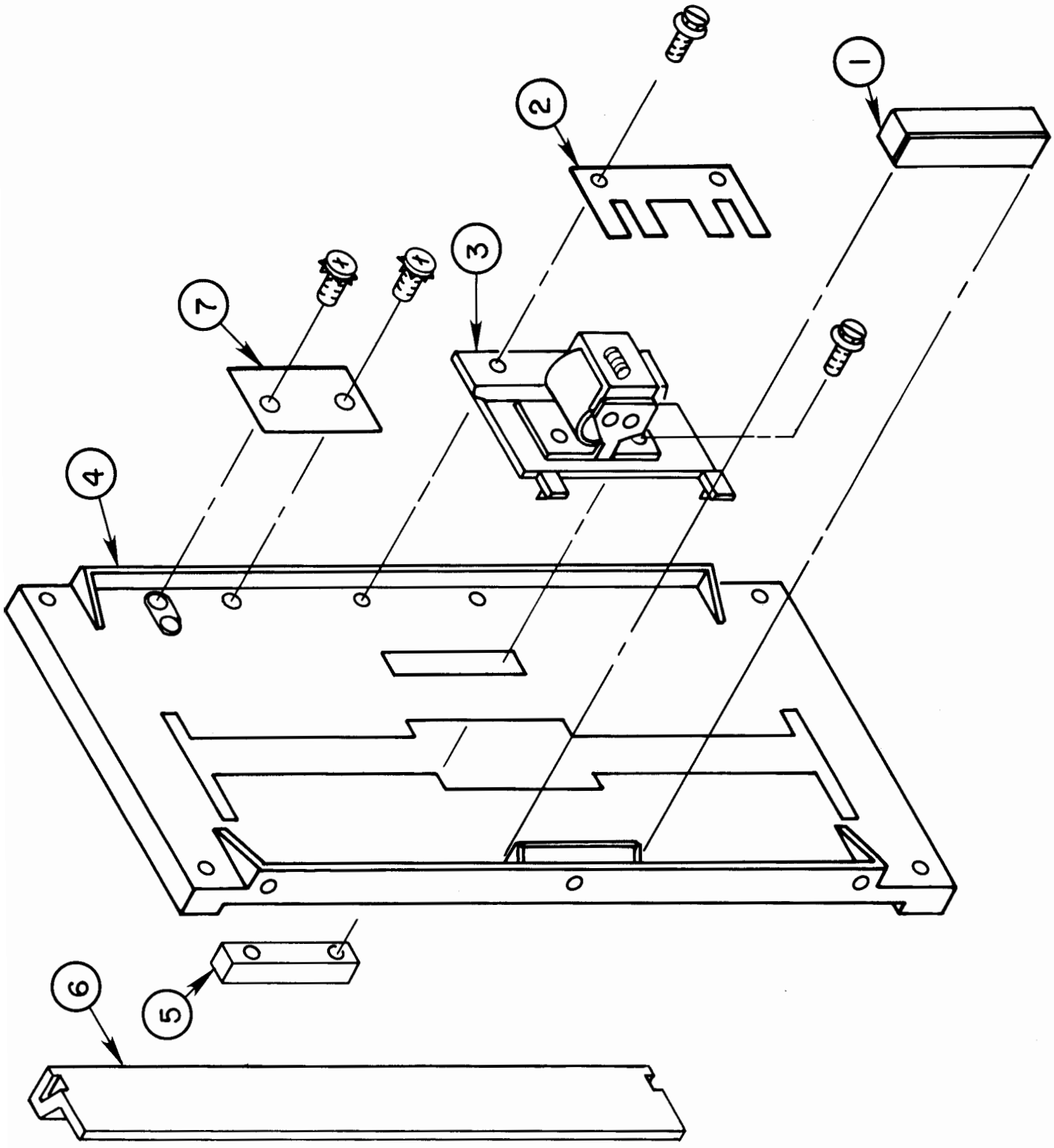


Figure 6-12: Disc Drive Assembly

Table of Contents

System Configuration Errors

-Message-	-Meaning-	-Action-
UNEXPECTED MEMORY PRESENT--BLOCK#(decimal), UPPER (or LOWER) HALF	system found more memory than expected	>Memory Board Switch settings may be incorrect. >Memory configuration table may be incorrect. >Additional block of memory may be present.
MEMORY FAILURE--BLOCK#(decimal), UPPER (or LOWER) HALF	system found less memory than expected	>Memory Board Switch settings may be incorrect. >Memory configuration table may be incorrect. >Memory failure during self-test.
CONSOLE ON PORT 0 GIVEN ALTERNATE SIZE MEMORY BLOCK	system found memory that had not been configured for use	>DROM or Remote Console table not/incorrectly configured. >Memory Board switch settings may be incorrect.
DROM LOADER FAILURES (will display DROM name and reason for failure)	insufficient space	>Memory Board switch settings may be incorrect. >DROM configuration table may be incorrect. >Memory failure during self-test.
	checksum error	>System failed to load correctly. >Operating System disc may be defective.
	DROM not present	>Certain DROMs require that other DROMs be loaded--DROM configuration table may be incorrect.

-Message-	-Meaning-	-Action-
LOADER ERROR A	a checksum error	>reload the system >try another Operating System disc
LOADER ERROR B	disc read error	>reload the system >try another Operating System disc
LOADER ERROR C	a check read error	>reload the system >try another Operating System disc
LOADER ERROR D	insufficient memory to load	>Memory Board switch settings may be incorrect. >Memory failure during self-test.
LOADER ERROR E	HP-IB power on or interrupt error	>reload the system >replace Peripheral Interface Board
LOADER ERROR F	the disc system did not identify or an internal system error	>reload the system >try another Operating System disc >See Chapter 5, Tests and Procedures
The SYSTEM FILE was not found	the Operating System was not found	>Operating System disc is not in any of the drives. >disc drive door open
SYSTEM LOAD FAILURE; ALL CONSOLES DOWN---CONSOLE ON PORT 0 DOWN; NO MEMORY AVAILABLE		>Memory Board switch settings may be incorrect. >Remote Console Configuration table may be incorrect, to modify the user's Remote Console Configuration table, load the system from the Support Disc. Record Support Disc table to user's disc and try reloading from

System Load Errors (continued)

-Message-	-Meaning-	-Action-
		user's Operating System disc.)If Support Disc connot be loaded, a memory failure most likely has occured.
KEYBOARD LOADER FAILURE		)reload the system)try another Operating System disc)Using the Support Disc, re-set the user's key-board configuration.(1)

(1)The Syntax Reference (p/n 45251-90050) contains pictorials for each language keyboard.

1 Software (DROM) configuration error.

2 Memory overflow.

3 Line not found or not in current program segment.

4 Improper RETURN

5 Abnormal program termination..

6 Improper FOR-NEXT matching.

7 Undefined function or subprogram.

8 Improper parameter matching.

9 Improper number of paramters.

10 String value required.

11 Numeric value required.

12 Attempt to re-declare a variable.

13 Array dimensions not specified.

14 Incorrect OPTION BASE statement usage.

15 Invalid bounds on array dimension, or string length in memory allocation statements.

16 Dimensions are improper or inconsistent.

17 Subscript out of range.

18 Substring out of range or substring too long.

19 Improper value.

20 Integer-precision overflow.

21 Short-precision overflow.

22 Real-precision overflow.

23 Intermediate-result overflow.

24 TAN(N*PI/2), when N is odd.

25 Argument of ASN or ACS is >1 in absolute value.

26 0 to a negative power.

27 Negative number to non-integral power.

28. Argument of LOG or LGT is negative.

29 Argument of LOG or LGT is 0.

30 Argument of SQR is negative.

31 Division by 0, or module 0.

32 String does not represent valid number, or string response when numeric data required.

33 Argument of NUM, CHR$, or PRT$ is improper.

34 Referenced line is not an IMAGE statement.

35 Improper image.

36 Out of data.

37 Edit string too long.

38 Syntax error in LENTER or ENTER.

39 Function subprogram not allowed.

40 Improper REPLACE or DELETE.

41 First line number>second line number.

42 Attempt to replace or delete a busy line or subprogram.

43 *Unused.*

44 Unused.

45 Nested keyboard-entry statements.

46 No binary in (RE)-STORE BIN or no progra(RE-)SAVE or (RE-) STORE or no key in (RE-)STORE KEY.

47 Subprogram COM declaration is not consistent with main program.

48 Recursion in single-lne function.

49 Line specified in ON declaration not found.

50 File number out of range from 1 thru 10.

51 File not currently assigned.

52 Improper volume label or mass storage unit specifier.

53 Improper file name.

54 Duplicate file name.

55 Directory overflow.

56 File name is undefined.

57 Attempt to use device of unknown type for mass storage.

58 Improper file type.

59 End of file found.

60 Physical or logical end of record found in direct access mode.

61 Defined record size too small for data item.

62 File is protected, or wrong protect code specified.

63 Number of records, bytes per record, or physical sectors exceeds 65534.

64 Medium overflow.

65 Incorrect data type.

66 Unused.

67 Parameter is < 0.

68 Invalid line number enountered during MERGE, GET, or LINK.

69 -

76 Unused.

77 Specified label not found.

78 Disc operation completed on device with possible volume label conflict.

79 Requested subprogram segment not present or binaries are not allowed in LOAD SUB.

80 Mass storage device door open or medium has been removed.

81 Mass storage device failure.

82 Mass storage device not present.

83 Mass storage device is write-protected.

84 Record not found.

85 Mass storage medium is not initialized.

86 Access not allowed to specified device.

87 Record address error.

88 Read data error.

89 Checkread error.

90 Mass storage system error.

91 Attempt to access a busy file.

92 Cannot get exclusive access to a specified file.

93 Attempt to access an exclusive file.

94 Specified file cannot currently be locked.

95 String not intact on file.

96 Program is run-only.

97 Door opened - data files closed.

98 Door opened - data lost.

99 Locked door opened.

100 Image specification expects a numeric item.

101 Image specification expects a string item.

102 Numeric field specification is larger than internal buffer size.

103 Item in PRINT USING list has no corresponding image specification.

104 -

119 Unused.

120 Output field overflow.

121 Improper value in CURSOR statement.

122 -

129 Unused.

130 Parameter for REQUEST or RELEASE out of range.

131 Specified device not available.

132 Referenced device missing or wrong type.

133 Printer is down.

134 Printer is offline.

135 -

139 Unused.

140 Spool file record length must be 256 bytes.

141 Incorrect data type found in spool file.

142 Door open - spool operation aborted.

143 Expansion of spool file would cause medium overflow.

144 Spool file size too small.

145 -

199 Unused.

PACK/250 Errors

200 Referenced line not a PACKFMT.

201 Target string for PACK may not be a string expression.

202 Insufficient dimension length in PACK statement, or insufficient curren length in an UNPACK.

203 List item > 32 K in PACK or UNPACK.

204 Conversion error.

205 UNPACK requires a source string of greater current length.

IMAGE/250 Errors

210 Bad status array.

211 No DBASE IS statemennt active; improper data bse specified or data base is not open.

212 Specified data set not found.

213 Too many variables in list.

214 IN DATA SET already active for data set.

215 Number of elements does not match.

216 Variable type does not match with associated field in set.

217 String length in list insufficient, or length of list array > 255 bytes.

218 Variable not in common.

219 Line referenced is not an IN DATA SET LIST statement.

220 Improper or illegal use of maintenance word.

221 Data set not created.

222 Needed volume lost during dismount.

223 Improper backup file.

224 Incomplete backup file.

225 Improper utility version number in root file.

226 Corrupt data base - must recreate it.

227 Corrupt data base - must erase it in its entirety.

228 Data sets cannot b e restored without a root file.

229 No volume name on data base or backup volume.

SORT/250 Errors

230 Improper nesting of SORT statements, including DATA BASE IS and IN DATA SET.

231 Cannot reactivate workfile.

232 Data base mode improper for sort.

233 Required data set or root file not mounted.

234 Missing or improper set linkage.

235 No WORKFILE IS # statement active.

236 Improper data item or data item not found.

237 Sum of sort field lengths plus overhead exceeds 256 bytes in SORT BY.

238 Improper synthetic linkage.

239 Insufficient space in workfile.

240 Program lost due to disc failure.

241 Improper operation attempted on workfile.

242 Improper READ # or PRINT # on workfile.

243 Workfile contains invalid information.

REPORT WRITER/250 Errors

250 BEGIN REPORT does not reference a REPORT HEADER statement.

251 Report Writer is already active.

252 An END REPORT DESCRIPTION statement is missing as terminator to the Report Description section statement.

253 Duplicate Report Writer Description section.

254 Blank lines in PAGE LENGTH statement is greater than page size, or is negative.

255 Expression in a Report Writer statement evaluates to an unacceptable value.

256 A TOTALS ON or GRAND TOTALS ON statement is improperly

positioned in the Report Description section.

257 A Report Writer operation was requested while outside the program scope of an active Report Writer, or an END REPORT was not executed for an active Report Writer before subprogram termination.

258 Effective page size is less than three lines.

259 Illegal execution of a Report Description section statement.

260 Insufficient space for printed output within the current page.

261 Left margin specified is less than 1, greater than current printer width -1, or greater than 132.

262 Control variable in BREAK WHEN statement has a length greater than was initially allocated.

263 A DETAIL LINE statement may not appear within the Report Description section.

264 Level parameter is out of range of from 0 thru 9.

265 (GRAND) TOTALS ON statement is not active for the level requested.

266 Sequence parameter is out of range for (GRAND) TOTALS ON statement at the level requested.

267 WITH number LINES parameter in a header, trailer, or detail line is greater than the effective page size or is negative.

268 OLDCV($) function references a level which does not have a break defined.

269 OLDCV($) function does not match the data type for the control variable in the BREAK WHEN statement at the level requested.

270 PRINTER IS statement may not be executed while Report Writer is active.

271 A Report Writer statement may not be used recursively.

FORMS/250 Errors

290 Not allowed when form is active.

291 Not allowed within form image.

292 Attempt to input after last field of form.

293 Attempt to output after last field of form.

294 Not allowed unless form is active.

TIO/250 Errors

310 Port ordinal out of range of from 11 thru 15.

311 Priority value out of range from 1 thru 15.

312 Invalid address in ON...interrupt statement.

314 Ownership error: must do REQUEST before ON INPUT.

315 No input available: cannot do AREAD$ from specified port.

316 Invalid SEND or SEND BREAK statement: specified device is not a computer.

Duplicate Errors

800 Source and destination volume specs are the same.

801 Device cannot be locked (files currently opened on that device).

802 Source and destination are not compatible.

803. Destination medium too small for source.

System Errors

1000 System files table full.

1001 Too many accesses to specified file.

1002 Request would result in deadlock.

1010 Memory parity error.

Some system malfunctions are denoted by an error-like message on the display. These messages will appear as the words "SYSTEM ERROR" followed by a letter. In addition, a table of numbers may be listed. If a condition of this type occurs, see Chapter 4, Software and Firmware.

Loader Errors

LOADER ERROR messages indicate that the operating system cannot be loaded successfully--

A	Checksum error.	D	Insufficient memory.
B	Disc read error.	E	Interface error.
C	Checkread error.	F	Disc or system error.

Loader errors A thru C may indicate that the operating system disc is worn or damaged. Try loading the system with the backup (spare) copy of the operating system disc. See System Load Errors in this chapter.

IMAGE Status Errors

The following list describes the condition word values for IMAGE programming statements.

Condition Word	Description Error
0	Successful execution - no error.
-1	No such data base. Data base is currently opened in an incompatible mode. Bad root file reference. Data base opened exclusively.
-7	Data base lock request was already made in current environment.
-10	User may not open additional data bases, five are already opened.

-11 Bad data base name or preceding blanks missing.

-12 DBPUT, DBDELETE, or DBUPDATE called with data base not locked.

-14 DBPUT, DBDELETE and DBUPDATE not allowed in access mode 8.

-21 Bad password - grants access to nothing.
Data item nonexistent or inaccessible.
Data set nonexistent or inaccessible.
Data set volume nonexistent.

-23 User lacks write access to data set.

-24 DBPUT, DBDELETE, DBUPDATE not allowed on automatic masters.

-31 Bad mode.
DBGET mode 7 - illegal for detail data set.
DBGET mode 5 - specified data set lacks chains.

-52 Item specified is not an accessible search item in the specified set.

Bad LIST variable - must be "@;" or "@".

-91 Root file not compatible with current IMAGE/250 statements.

-92 Data base requires creations.

-94 Data or structure information lost. Data base must be erased or re-created.

11 End-of-file.

12 Directed beginning of file.

13 Directed end of file.

15 End of chain.

16 The data set is full.

17 There is no chain for the search item value.
There is no entry with the specified key value.
No current record or the current record is empty.
The selected record is empty.

18 Broken chain.

20 Data base currently locked by another user.

41 DBUPDATE will not alter a search item.

43	Duplicate key value in Master.
44	Can't delete a Master entry with non-empty Detail chains.
50	User's buffer is too small for requested data.
53	ARGUMENT field type incompatible with search field type (DBGET, mode 7, or DBFIND). ARGUMENT's current string length is less than the string length of the search field.
80	Data set volume is not on-line.
90	Root file volume is not on-line.
1xx	There is no chain head for path xx.
3xx	The automatic master for path xx is full.
4xx	The master data set for path xx is not currently mounted (applies to DBPUT and DBDELETE for detail data sets).

DBLOAD/DBUNLD ERRORS

Error Number	Error Message
1	INCORRECT PASSWORD
2	IMPROPER SET COUNT
3	IMPROPER ITEM COUNT
4	SEARCH ITEM SUBCOUNT > 1
5	UNKNOWN SEARCH ENTRY TYPE
6	IMPROPER SEGMENT ENTRY COUNT
7	OPERATION TERMINATED
8	NO ROOM ON CURRENT BACKUP VOLUME
9	DATA SET NAME NOT FOUND
10	DATA BASE STATUS
11	DATA BASE NOT AVAILABLE
12	BACKUP FILE VOLUMES OUT OF ORDER

13 DUPLICATE BACKUP FILE NAME

14 PURGE NOT CONFIRMED; OLD FILE KEPT

15 FATAL ERROR

16 ROOT FILE NOT FOUND

17 ATTEMPT TO UNLOAD OR LOAD AUTOMATIC MASTER

18 ITEM POSITION VALUE EXCEEDS ITEM COUNT

19 IMPROPER VOLUME COUNT

20 ITEM TYPES DO NOT MATCH

21 ATTEMPT TO LOAD CORRUPT DATA BASE

22 REQUESTED DATA SET NUMBER NOT FOUND

23 ZERO LENGTH BACKUP FILE

24 IMPROPER DATA SET NUMBER

25 FORM IS NOT COMPLETE

26 FILE NAME NOT FOUND

27 IMPROPER PATH NUMBER

28 IMPROPER INPUT VALUE

29 INCORRECT FILE TYPE

30 BACKUP FILE NOT CREATED BY DBUNLD UTILITY

31 ERASE REQUIRES ALL VOLUMES BE MOUNTED

32 FEWER ENTRIES UNLOADED THAN EXPECTED

33 FEWER ENTRIES LOADED THAN EXPECTED

34 DATA BASE IS MARKED CORRUPT

35 PROGRAM FILE VERSION DESAGREEMENT

36 BACKUP SET NUMBER NOT IN DATA BASE

37 READ FAILURE IN DATA SET RECORD POSITION

38 SEARCH ITEM ERROR

39 MISSING MASTER ENTRY FOR SEARCH VALUE

40 VOLUME NAME TOO LONG: TRUNCATED VALUE

41 FILE PROTECT CODE DOES NOT MATCH

42 MISSING DATA SET

CHAPTER 8

Data Communications

Table of Contents

PART I: Asychronous Serial Interface

PART I: Asychronous Serial Interface

The Asynchronous Data Communication Board is a microprocessor-controlled interface between the HP 250 and up to five remote devices. Any combinition of terminals, printers, and computers is permited. Connections are made via RS-232C, 20mA current-loop , and/or modem.

Each port on the RS-232C Connector Board can be configured to run at any of nine speeds from 110 thru 9600 baud. The rate is selected with a 10-position baud-rate switch for each port. Each port must also be configured, via jumpers, for the type of connection desired.

Installation Procedures

See Figure 8-1: Interface Installation.

1. Turn the HP 250 OFF and disconnect the power plug.

2. Open the back-panel door.

3. Remove the Cover Plate from the rear side panel.

4. Remove all connectors from the connector-plate and then remove the connector-plate from the rear side panel.

5. Install the Cover Panel to where the Cover Plate and Connector-Plate were removed.
   Cover Plate was removed using the Cover Plate screws.

6. Set the RS-232C Connector Board jumpers as determined by port usage. See Table 8-2: Jumper Configurations.

7. Connect the Board Interconnection Cable to the RS-232C Connector Board. See Figure 8-3: RS-232C Connector Panel Assembly.

8. Mount the RS-232C Connector Board Assembly to the left side of the Cover Panel.

9. Mount the blank Panel to the right side of the Cover Panel.

10. Route the Board Interconnection Cable along the wire bundle to the card cage. Secure the cable to the wire bundle with wire ties and the aluminum cable tray. Longer screws may be required to secure the cable tray.

11. Check that all the Asynchronous Data Communication Board jumpers are in the 'A' position. Plug the board into a card-cage slot designated for Data Communications use. See Chapter 3, Figure 3-3: Card-Cage Configuration.

12. Connect the Board Interconnection Cable to the Asynchronous Data Communication Board.

13. Set the baud-rate switches as required for each port. See Figure 8-2: Baud-Rate and PA Switches.

14. Set the Peripheral Address Switch to PA5. This will ensure that the left-most port is Port 1 and the right-most port is Port 5. See Figure 8-2: Baud-Rate and PA Switches.

NOTE

When accessing a port with a program, add 10 to the port number(1-5) to get the port address.

15. Run the CONFIG program and edit the TIO DROM to auto-load, and the Remote I/O Configuration to reflect the port designation made during Step 6.

16. Verify the Asynchronous Serial Interface operation. See Operation Verification on page 8-10.

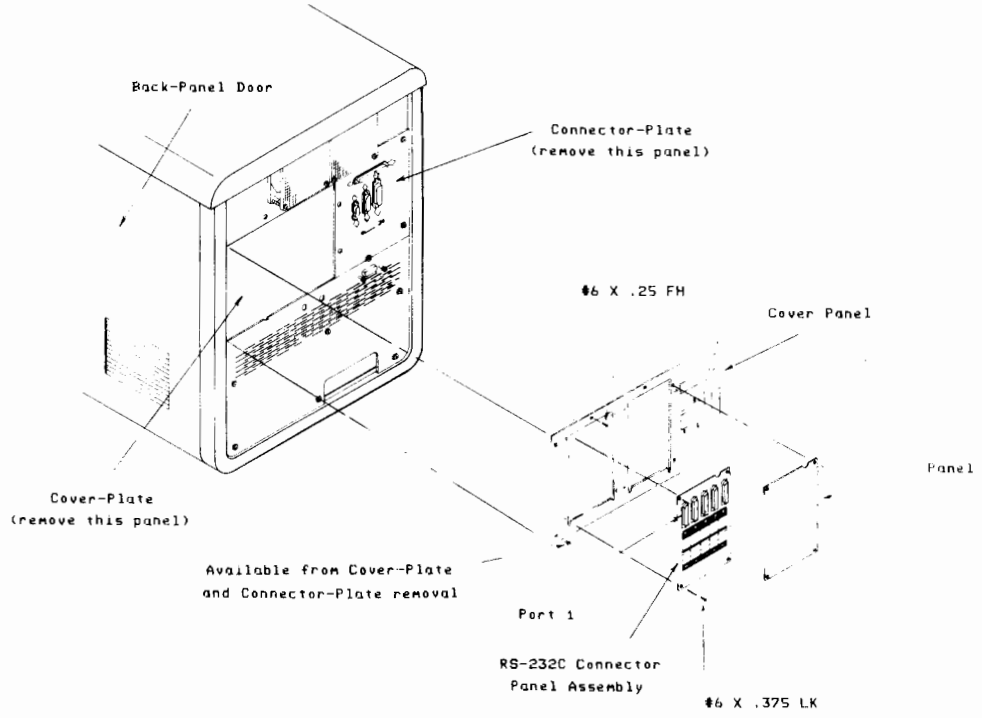


Figure 8-1: Interface Installation.

Peripheral devices are connected to the HP 250 by using a modem, direct connection, or 20 mA current loop. Table 8-1 shows the type connection and the cabling needed to connect the supported peripheral devices to the HP 250.

Table 8-1: Cabling Information

DEVICE	TYPE CONNECTION	CABLE/OPTION REQUIREMENTS	
		HP 250	DEVICE
TTY Compatible RS-232C I/O	MODEM	45111A	Customer Supplied
	DIRECT	45113A*	Customer Supplied
HP 264X Series Terminals	MODEM	45111A	13232A (both) 13232M (EUR) 13232N (US)
	CURRENT+	45112A	13232F
	DIRECT	45113A*	13232A (both) 13232M (EUR) 13232N (US)
HP 262X Series Terminals	MODEM	45111A	13222M (EUR) 13222N (US)
	DIRECT	45113A*	13222M (EUR) 13222N (US)
HP 2635 Keyboard/Printer and HP 2631 Printer	MODEM	45111A	Option 41
	DIRECT	45113A*	Option 41
HP 3000 COMPUTER	MODEM	45111A	30062B
	DIRECT	45111A	45113A*

*The 45113A cable is optional, and is used to expand the distance between the HP 250 and the terminal. (gives an additional 10.5 metres)

+The General Purpose Asynchronous Card (HP 13260B) is required for current loop connections to 264X series terminals.

Baud-Rate and PA Switches

The baud-rate and PA switches are located on the Asynchronous Data Communication Board, as shown in Figure 8-2. Each baud-rate switch must be set to match the baud-rate for the device connected to the corresponding port.

Always set the PA switch to position PA 5. This ensures that the RS-232C Connector Board ports are numbered 1 thru 5, left to right respectively. Position PA 4 is not available for use at this time.

SWITCH SETTING	BAUD RATE
0	110
1	200
2	300
3	600
4	1200
5	1800
6	2400
7	4800
8	9600
9	not used

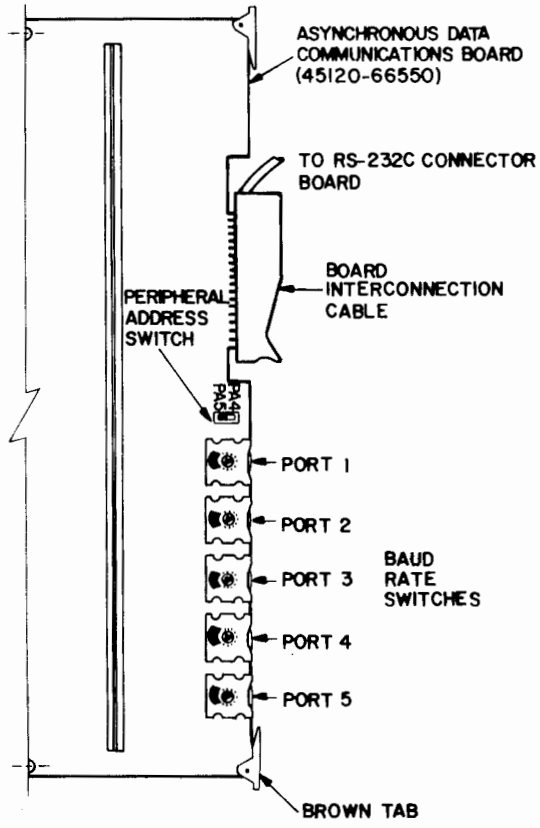


Figure 8-2: Baud-Rate and PA Switches

A full description of the RS-232C interfacing standard is beyond the scope of this manual. More detail concerning the mnemonics used in defining the jumpers can be found in: EIA STANDARD RS-232-C. A copy may be obtained from the Engineering Department of the Electronic Industries Association.

Table 8-2: Jumper Configurations

JUMPER	DIRECT CONNECTION = RS-232C	DIRECT CONNECTION = CURRENT LOOP	MODEM CONNECTION = LEASED LINES	MODEM CONNECTION = SWITCHED LINES
1	A	B	A	A
2	A	B	A	A
3	A	B	A	A
4	A	B	A	A
5	A	B	A	A
6	A	A	A/B/C (2)	A
7	A	A	B	B
8	A	A	A	B
9	A/B (1)	A	B	B
10	A	A	C	B/C (3)

NOTES:

1 A -if DTR is not provided by the remote device
B -if DTR is provided by the remote device

2 sets desired Data Rate Select (function of the modem used)

3 B -monitor CTS (US)
C -monitor DCD (EUR)

Jumper Definitions

Jumper	Definitions
1-5	A RS-232C B 20mA Current Loop
6	A DRS not used B DRS wired to +12v C DRS wired to -12v
7	A RTS not used B RTS wired to +12v thru 2.7K pull-up
8	A DSR(DTR for modem) wired to +12v thru 2.7K pull-up B DSR(DTR for modem) controlled by UART
9	A DTR(DSR for modem) wired to +12v thru 2.7K pull-up B DTR(DSR for modem) monitored
10	A CTS and DCD not monitored: input to UART wired to +12V thru 2.7K pull-up B CTS monitored C DCD monitored

HP Terminals and Printers

When connecting the HP 264X series terminals, HP 2635 Keyboard/Printer, or the HP 2631 Dot Matrix Printer directly to the HP 250, use direct connection RS-232C with all jumpers set to 'A' except jumper #9. Set jumper #9 to 'B'.

HP 3000

Direct connection of the HP 250 to an HP 3000 requires that all jumpers be set to 'A' except jumper #9. Set jumper #9 to 'B'.

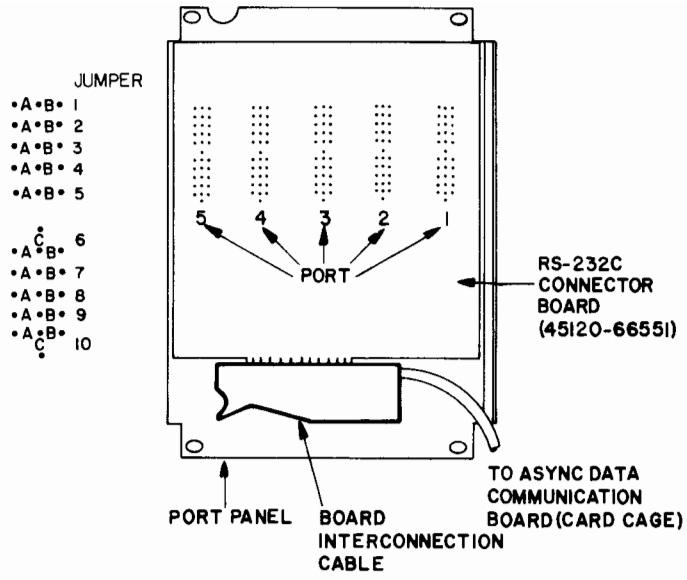


Figure 8-3: RS-232 Connector Panel Assembly

HP Terminals

Enter and run the following program for each terminal port.

```
10    INPUT "ENTER DEVICE ADDRESS OF PORT UNDER TEST";P
20    REQUEST P
30 Pr:  PRINTER IS P
40    PRINT "TYPE IN DATA AND PRESS RETURN KEY"
50    ON INPUT #P GOTO In
60    WAIT
70 In:  PRINTER IS 8
80    DISP AREAD$(P)
90    END
```

This program outputs the statement "TYPE IN DATA AND PRESS RETURN Key" to the terminal. Data entered at the terminal is then transferred to the HP 250 and displayed on the CRT.

HP 2631 Printer

Execute the PRINTER IS <port # +10> statement.
Execute PRINT "TEST"
The printer should print the word 'TEST'.
Repeat the test for each printer port.

HP 3000 Computer

Run the HP 3000 link program, "LK3000".
The HP 3000 system prompt (:) should appear.
LOG ON
LOG OFF
Depress the HALT Key to terminate the "LK3000" program.
Repeat the test for each HP 3000 port.

Description	Part Number	
Asynchronous Data Communication Board	45120-66550	
RS-232C Connector Board	45120-66551	
Board Interconnection Cable	45120-61600	
Panel	45120-00211	
Panel, Connector	45120-00212	
Panel, Cover	45000-00214	
RS-232C Modem Cable (4.5 meters)	45111-61601	
20mA Current-Loop Cable (1.5 meters)	45112-61602	
RS-232C Direct Connection Cable (10.5 meters)	45113-61603	(optional)
Screw, panhead w/lock	2360-0117	(available from cover plate removal)
Screw, #6x.25 FH	2360-0181	(not included with HP 45120A)
Screw, #6x.375 LK	2360-0117	
Label, I/O Port	7120-1144	

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