# HP 92900A SUBSYSTEM
# HP 3070A REAL-TIME APPLICATIONS TERMINAL
# HP 40280A SERIAL LINK CONTROLLER
# DIAGNOSTIC

for

hp-21MX or 2100 A/S COMPUTERS

# reference manual

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Manual Part N° 92900-90003
Microfiche Part N° 92900-90004

Printed in Germany 10/76

# LIST OF EFFECTIVE PAGES

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## TABLES



## ILLUSTRATIONS

# SECTION I

# INTRODUCTION

## 1-1. GENERAL

The HP 92900A Diagnostic verifies proper operation of the HP 92900A Real Time Applications Terminal Subsystem (40280A Controller Interface and 3070A associated Terminals) used with HP21MX or 2100A/S Computer Series. The Basic I/O portion of the card and most the functions of the subsystem are exercised. Some tests are provided to allow verification of installation itself.

Refer user to 3070 Terminal, 92900 Subsystem and 40280 Controller Manuals for further details of the products. Part n° 03070-90001, 92900-90001, 40280-90001, respectively.

The diagnostic is run in conjunction with the HP2000 Computer systems diagnostic configurator (Part n° 24296-60001).

## 1-2. REQUIRED HARDWARE

The minimum required hardware consists of the following :

- An HP 21MX or 2100 A/S Computer with a minimum of 8 K Memory
- An HP 40280A Serial Link Controller
- An HP 3070A Terminal
- A loading device for loading the diagnostic program
- A system console device is optional but recommended for report and error message output.
- An HP 92900-60000 Test cable or User Installation Cable set-up with 92901A connexion boxes.
- An HP 03070-60007 Terminal to Serial Link Cable
- An HP 40280-60002 Interface cable.

## 1-3. REQUIRED SOFTWARE

The required software consists of the following :

- HP 2100 Computer Systems Diagnostic Configurator Part No 24296-60001.
- HP 2100 Computer Systems Diagnostic Configurator Manual Part No 02100-90157.
- HP 92900A Subsystem Diagnostic Part No 92900-16001.
- HP 92900A Subsystem Reference Manual Part No 92900-90003.

The Diagnostic Serial Number (DSN) is contained in memory location 126 of the program. The DSN for this program is 104017.

## 1-4. TEXT CONVENTIONS

All halt codes, select codes and addresses mentioned in this manual are octal unless specifically shown otherwise.

# SECTION II

# PROGRAM ORGANIZATION

## 2-1. ORGANIZATION

This diagnostic program contains an initialization section, control section, 9 standard tests and 3 optional tests. The tests are called into execution as sequential or selectable subroutines.

The following functions are placed under test by this diagnostic :

| | |
|---|---|
| - Flag and Control (Basic I/O) | TST 00 |
| - Controller and RAM alone | TST 01 |
| - Communication Module (ISP) | TST 02 |
| - Terminal Functions | TST 03 |
| - Prompting Lights | TST 04 |
| - Display | TST 05 |
| - Keyboard keys | TST 06 |
| - Special Function Keys | TST 07 |
| - Address Test | TST 10 |
| - Cable Quality and Transmission test | TST 11 |
| - Extended Cable/Controller Test | TST 12 |
| - Total Installation test | TST 13 |



## 2-2. TEST CONTROL AND EXECUTION

The program executes the tests according to the options selected in the S-register by the operator. The control section mainly supervises S-register bits 15 (decimal) 13 (decimal) and 12 (decimal).

The program also keeps count of the number of passes that have been completed and will load the A-register with the pass count at the end of each pass.

The count is cleared whenever the program is restarted. Test sections are executed one after the other in each diagnostic pass (sequentially or selectively according to operator intervention).

## 2-3. SELECTION OF TESTS BY OPERATOR

User selection or default will determine which test sections will be executed. The operator may select his own test or tests to be executed via S register bit 9 (decimal). Paragraph 3-4 outlines the test selection.

## 2-4. MESSAGE REPORTING

There are two types of messages - error and information. Error messages are used to inform the operator of a failure within the hardware. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform some operation related to the unit's function.

An associated halt will occur to allow the operator time to perform the function ; the operator must then press run.

When a console device is used, the printed message will be preceeded by an E (error) or H (information) letter prefix and a number (octal). The number is the same as the last two octal digits of an associated halt code.

Example : Error with halt
Message : E 001
Halt code : 102001 (T register)

Example : Information with halt
Message : H 027
Halt code : 102027 (T register)

Example : Information without halt
Message : H 054
Halt code : none

Error messages can be suppressed by S-register bit 11 (decimal) and error halts can be suppressed by S-register bit 14 (decimal).

Information messages are suppressed by S-register bit 10 (decimal).

## 2-5. PROGRAM LIMITATIONS

Interface capability for receiving, passing and denying priority (priority string logic) is not completely checked by this diagnostic. If the interface does not receive priority (ie PRM from the next lower select code) an error E014 (NO INT) will occur. To check this, remove an interface of a lower select code and run the Basic I/O test. The above mentioned error should occur. Checking the interface's ability to pass or deny priority is beyond the scope of this diagnostic. Also the Direct Memory Access (DMA) or Dual Channel Port Controller (DCPC) portion of the interface is not tested by this diagnostic. Finally, it does not test HP-IB beyond the terminal itself.

# SECTION III

# OPERATING PROCEDURE

**WARNING**

TST 01 must be run with all terminals connected to the loop **switched off.**

TST 02 through TST 07 and TST 11 must be run with **one terminal** whose internal **address is set to 63** (77 octal).

The tests TST 10, TST 12 can be run with **one terminal** whose internal **address is operator choosen.**

TST 13 and **only TST 13** can be run with more than one terminal switched ON on the serial link at any given time.

(A flowchart of the operating procedure is provided in figures 3-1 and 3-2).

## 3-1. LOADING AND CONFIGURING

First the Diagnostic Configurator is loaded and configured, then the Diagnostic is loaded. The configuration section of this diagnostic must be completed according to instructions that follow, prior to execution.

## 3-2. LOADING THE PROGRAMS

Load the Diagnostic Configurator (24296-60001) and configure it if necessary according to the HP 2000 computer System Diagnostic Configurator Reference Manual Part no 02100-90157.

## 3-3. CONFIGURING THE DIAGNOSTIC

If a preconfigured diagnostic has been loaded, proceed with paragraph 3-4. Otherwise, load the P-register with starting address 100 (octal), load the Switch Register with the select code of the interface under test, (bits 0 through 5). Press PRESET (INT & EXT) and press RUN. The computer will run and then halt with 102 074 in the Memory Data Register (MDR). If halt 102 073 occurs the select code input was less than or equal to 7 (octal). Correct the select code and press RUN.

## 3-4. RUNNING THE DIAGNOSTIC

If a preconfigured tape was loaded or the dump routine was used, Set P-register equal to 2000 (octal) ; if not, do not modify the P-register. Select program options according to table 3-2 (Standard tests, 0 to 10, are executed if S-register is left to 0).

Refer to section IV for test execution and description.

At completion of each pass of the diagnostic, the pass count is output to the A-register for operator information. If S-register bit 12 is clear, the computer halts with 102 077 in the T-register. To start another pass, the operator should press RUN.

If the optional tests (TST 11, TST 12, TST 13) are selected, the program remains in one of these tests until S-register bit 7 is set.

If a trap cell occurs (T register = 106077), the user must determine the cause of the interrupt or transfer of control to the location in the M-register. The program may need to be reloaded to continue.

Refer to table 4-2 for halts and messages and table 4-3 for test execution times.

## 3-5. RESTARTING

The program may be restarted by setting the P-register to 2000, select the desired program options per table 3-2 in the S-register and press PRESET, RUN. The program may be reconfigured and restarted by setting the P-register to 100 select the program configuration table 3-1 in the S-register and press PRESET, RUN (Refer to figure 3-1).

## 3-6. TEST SELECTION BY OPERATOR

The control portion of the program allows the operator the option to select a test or sequence of tests to be run. The operator sets the S-register bit 9 and press RUN. If the computer is running, the test in progress will be completed and then the computer will halt with 102 075. The operator loads the A & B registers with the tests desired per table 3-3.

The operator must clear the S-register bit 9 and press RUN. If bit 9 not cleared, computer will halt 102 075 again. The operator selected tests will then be executed.

If the operator clears all the bits in the A & B registers, the default set of tests (TST00 through TST10) will be run.

Table 3-1. Program Configuration S-Register Settings

| Bits | Function |
|---|---|
| 0-5 | Enter the select code of HP 40280A Serial Link Controller. This must be an octal number greater than 7 and less than or equal to 77. |
| 6-15 | Reserved |

Table 3-2. Program Options S-Register Settings.

| Bits | Meaning if set |
|---|---|
| 0-6 | Highest address to be polled during TST 13. (If left 0 then $77_8$). |
| 7 | Abort current test and continue the diagnostic sequences. |
| 8 | Suppress tests requiring operator intervention. (Tests are entered and immediately exited). |
| 9 | Select a particular set of tests. When a test is currently executing (*), bit 9 set aborts diagnostic execution at end of current test section and halts 102075. User may specify a new group of tests in the A Register (see table 3-3). Clear S register bit 9 and press RUN. |
| 10 | Suppress non-error messages. |
| 11 | Supress error messages. |
| 12 | Loop on diagnostic and suppress tests requiring operator intervention. Message "Pass XXXX" is printed if a console is present. |
| 13 | Repeat last test section. |
| 14 | Suppress error halts. |
| 15 | Halt 102076 at the end of each test. The A Register contains the test number in octal. |
| (*) If computer is not running press RUN to get halt 102075. | |

Table 3-3. Test Selection Summary S-Register Settings.

| A-reg bit | If set will execute | |
|---|---|---|
| 0 | TST 00 | Basic I/O |
| 1 | TST 01 | Communication Module Test |
| 2 | TST 02 | Controller Test |
| 3 | TST 03 | Terminal Functions Test |
| 4 | TST 04 | Annunciator Lights Test |
| 5 | TST 05 | Display Test |
| 6 | TST 06 | Keyboard Test |
| 7 | TST 07 | Special Function Key Test |
| 8 | TST 10 | Address Test |
| 9 | TST 11 | Cable Test |
| 10 | TST 12 | Extended Cable/Controller Test |
| 11 | TST 13 | Total Installation Test |
| 12-15 | Reserved | |
| B-reg bit | | |
| 0-15 | Reserved | |

**Note :**
If the A - and B - registers are clear, the default set of tests (TST 00 - TST 10) are run - TST 11, TST 12, TST 13 are optional tests.

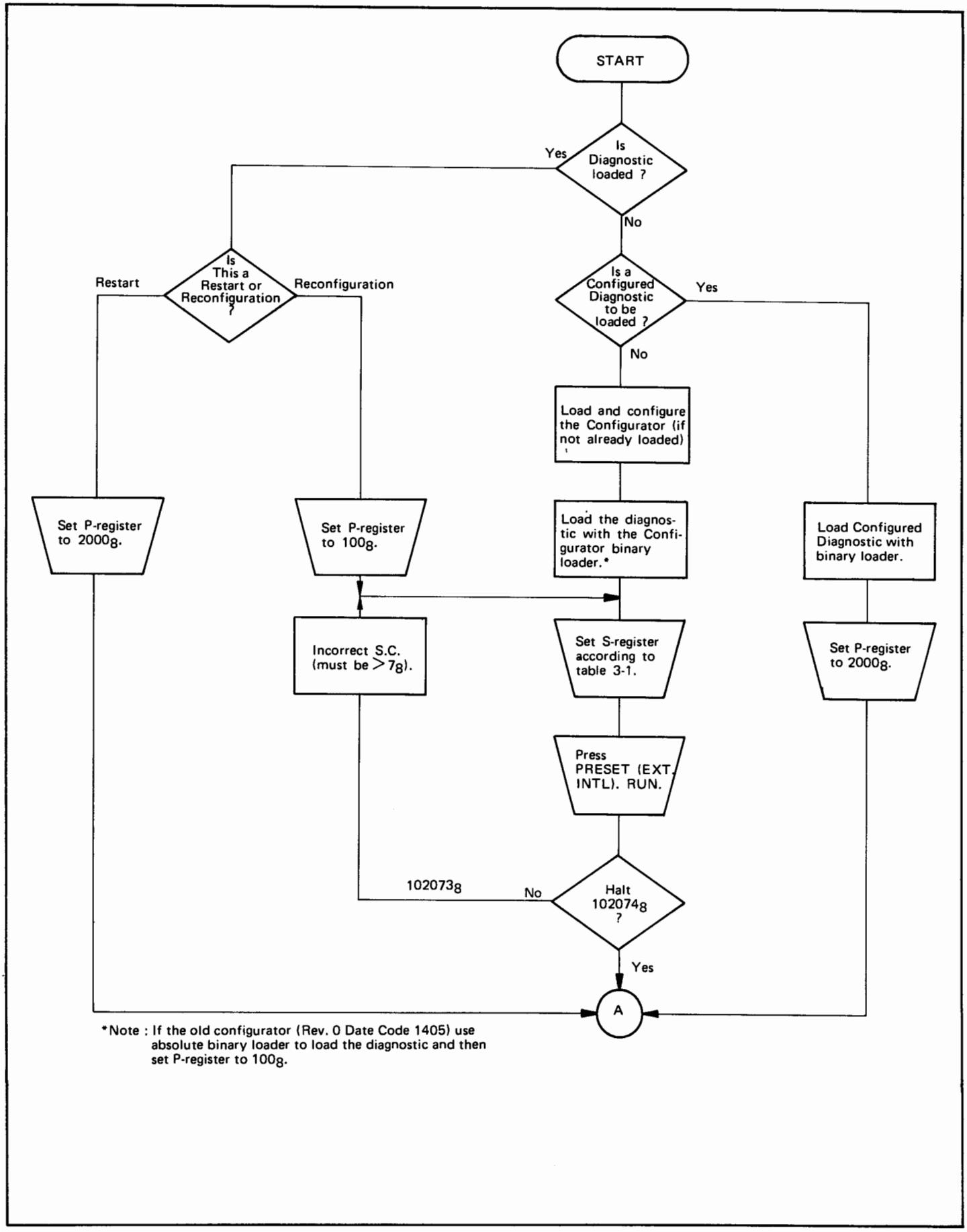



Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 2)

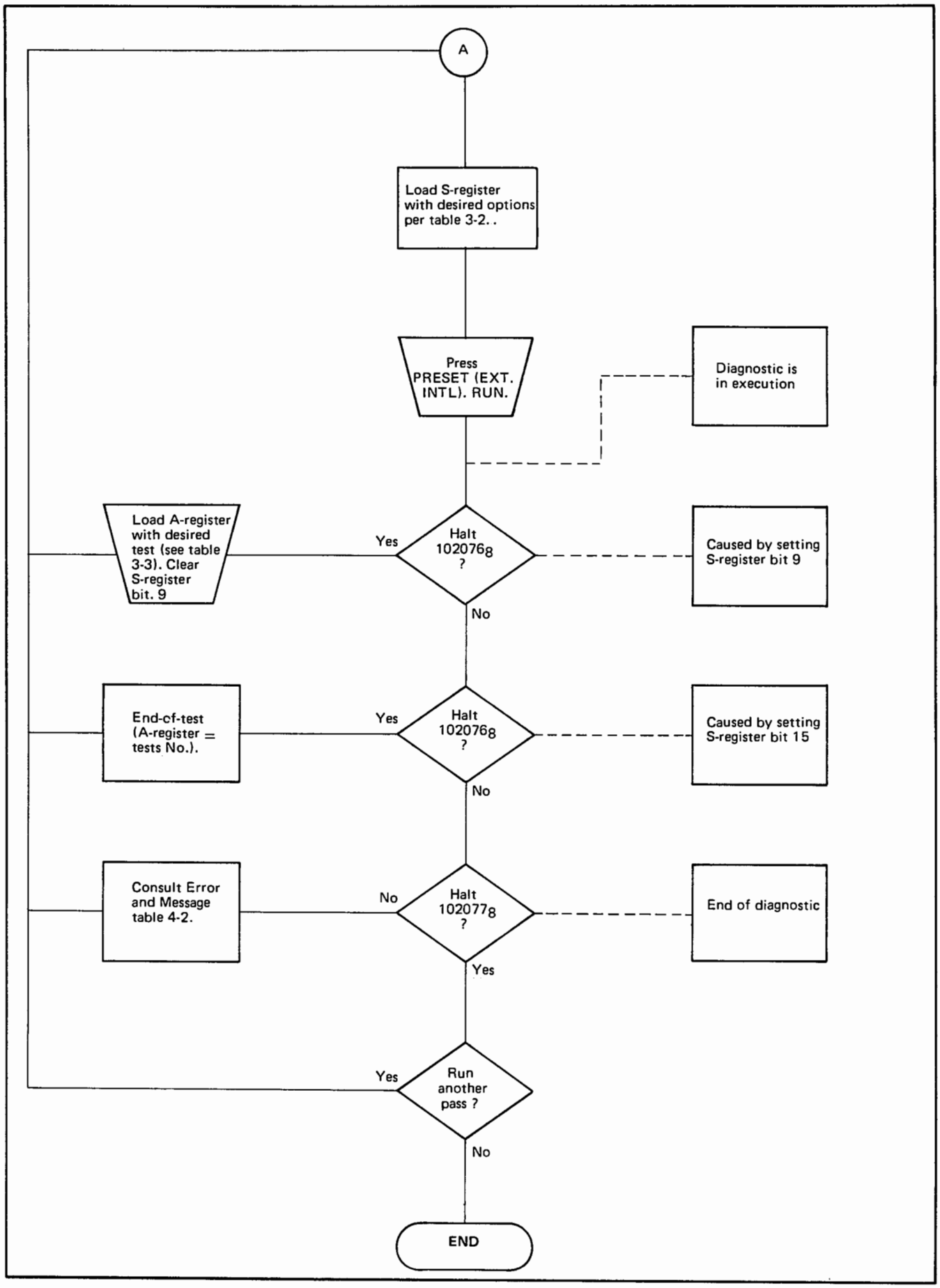



Figure 3-1. Operating Procedure Flowchart (Sheet 2 of 2)

# SECTION IV

# DIAGNOSTIC PERFORMANCE



## 4-1. TEST DESCRIPTION

The tests in this diagnostic are described in the following paragraphs.

Fig. 4-1 illustrates the command formats and interface link status for each terminal data transfer table word.
Table 4-1 Summarizes halt codes.
Table 4-2 Provides additional details on the content of each test and messages/halts signification.
Table 4-3 Contains the various test execution times.

## 4-2. BASIC I/O TST 00

**Subtest 1**

Checks the ability to clear, set and test the interrupt system. The following instruction combinations are tested :

CLF 0 - SFC 0
CLF 0 - SFS 0
STF 0 - SFC 0
STF 0 - SFS 0

Errors in the above sequences produce error messages E000 - E003 as shown in table 4-2.

**Subtest 2**

Checks the ability to clear, set and test the interface Flag. The following instruction combinations are tested :

CLF SC - SFC SC
CLF SC - SFS SC
STF SC - SFC SC
STF SC - SFS SC

Errors in the above sequence produces error messages E005 - E010 as shown in table 4-2.

**Subtest 3**

Checks that the test select code does not cause an interrupt with the flag and control set on the interface and the interrupt system off. The sequence of instructions is shown below :

```
STF 0
STF  SC
STC  SC
CLF  0
```

The CLF 0 instruction should inhibit an interrupt from occuring. Error message E004 occurs if CLF 0 fails.

**Subtest 4**

Checks that the flag of the interface under test is not set when all other select code flags are set. Error message E011 occurs if a flag is set incorrectly.

**Subset 5**

Checks the ability of the interface to interrupt. With the Flag and Control set and the interrupt system on, there should be an interrupt from the Select Code. If not, error message E014 occurs. Check that the interrupt occured where expected. The interrupt should not occur before a string of priority affecting instructions are executed. The following instructions are used to check the hold-off operation :

```
STC  1
STF  1
CLC  1
CLF  1
JMP  *+1,I
DEF  *+1
JSB  *+1,I
DEF  *+1
NOP
```

Error messages E012 and/or E015 will occur if the hold off fails. This test also checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message E013 will occur if an interrupt does occur. Check that no instruction was missed during the interrupt (E026 INT EXECUTION ERROR).

**Subset 6**
Check that with the interrupt system on and the SC control and Flag set, there is no interrupt following a CLC SC instruction. The following sequence of instructions are used :

```
STC  SC
STF  SC
STF  0
CLC  SC
```

If the CLC SC fails to inhibit an interrupt, error message E-16 will occur.

**Subtest 7**
Checks that the CLC 0 instruction inhibits interrupts when the SC Control and Flag are set. The following sequence of instructions are used :

```
CLF  SC
STC  SC
STF  SC
STF  0
CLC  0
```

If the CLC 0 fails to inhibit an interrupt, error message E017 will occur.

**Subtest 8**
Checks that the PRESET (EXTERNAL and INTERNAL if applicable) switches on the operator panel perform the following actions :

1. Sets the interface Flag (EXTERNAL)
2. Clears the interface Control (EXTERNAL)
3. Turns off the interrupt system (INTERNAL)
4. Clears the I/O data lines (EXTERNAL).

## 4-3. CONTROLLER TEST = TST 01

This test is run with no terminal on or connected.

This test sends data patterns to the controller, simulating a transfer.
Data patterns are stored in the RAM, serialized and stored back again. Content is checked against initial patterns. Some hardware flowcharts are exercised on the controller at the same time.

Upon error detection a message is printed with failing RAM location address in the B-register ; after pressing RUN a second halt occurs with the actual pattern in A-register and the expected pattern in B-register.

According to the nature of the problem (lost bits and number of addresses in error) it is possible to localise the defect on the controller.

**CAUTION**

The test must be run with all terminals OFF (or with controller alone) because the bit of acknowledgement (OK bit) must return with a logical zero level.

**NOTE** : This test exercises the RAM, shifters, serializer, flowcharts (main, input, link) and input circuits. Not checked at this point are the synchronization, cyclic redundancy checking, line drivers and input synchronization circuits.

## 4-4. COMMUNICATION MODULE TEST = TST 02

This test is run with one terminal whose address must be 77 (octal) connected to the computer via the test cable (HP part no. 92900-60000).

The test allows verification, at the communication module level, of correct transmission of commands and control bits in output and input phases.

The data output is a pattern of possible combinations (110000 to 114000) and alternates with input commands.

If any error occurs, error message will be printed with terminal address found in error in B-register. After pressing RUN a second halt occurs with A-register = actual data ; B-register = expected data.

To shorten this test section set S-register bit 7.

### 4-5. TERMINAL FUNCTIONS TEST = TST 03

This test is run with the same set-up as TST 02.

This test exercises the main functions of the terminal which are configuration and deconfiguration for listeners and talker, ability to send a SRQ, ability to stay in Idle State and reset on IFC command.

A first halt (102042) indicates the user to check that display is clear and the keyboard configured. If yes press RUN. A second halt (102043) indicates to check if keyboard is deconfigured. If yes, press RUN.

After halt 102044 press RUN and type up to 15 characters on keyboard terminated by ENTER.

After ENTER is pressed, a halt 102045 occurs = Check if the display is clear. If yes, press RUN = Display will output the characters just typed in.

After halt 102046 press RUN and type up to 15 characters within 15 seconds. After this delay, if no errors are detected, a halt 102047 occurs. Press Service Request key within 15 seconds. If no errors are detected test TST 03 completes.

### 4-6 PROMPTING LIGHTS TEST = TST 04

This test is run with the same set-up as TST 02.

This test is a display test but oriented toward prompting lights. It exercises the unique relation between a specific "ON" order and the associated light with all lights off, and a specific "OFF" order and the associated light with all lights "ON".

User must check that an "ON" order of the sequence doesn't light other lights, and the same default doesn't occur with "OFF" order sequence.

### 4-7. DISPLAY TEST = TST 05

This test is run with the same set-up as TST 02.

The test allows a visual check of each possibility of each digit and at the same time verifies ability to display variable line length and listener configuration deconfiguration.

The user checks proper execution of the following sequence :
- Display of a full line of "8",
- Display of variable length lines (character "8" goes from right to left, preceded by "-" character).
- Output of a full "." line.
- Output of a line with all the displayable characters.

Then a halt 102057 prompts the user to check display is clear and remains clear while test writes on deconfigured display.
Test completes on halt 102060.

### 4-8. KEYBOARD TEST = TST 06

This test is run with the same set-up as TST 02.

The test exercises the keyboard keys and the keyboard talker function by control of :
- Absence of deconfiguration between two characters input,
- Deconfiguration after ENTER code keying,
- Proper character code generation.

The terminal display prompts the operator with the key to be pressed and returns the received code. If an error is detected "EE" is displayed.

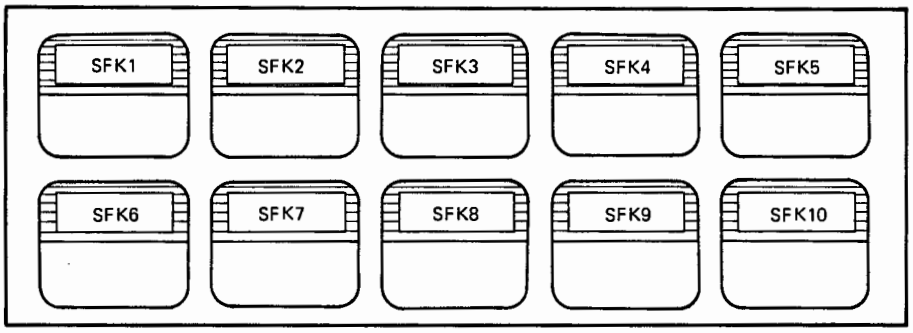
The indicated key is to be pressed only after the "keyboard configured" indicator is "ON".
The order is : 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, ., –; delete, enter.

## 4-9. SPECIAL FUNCTION KEYS TEST = TST 07

This test is run with the same set-up as TST 02.

This test is based on the same scheme as the keyboard test and the operator has to depress keys in a given order. An annunciator light is lit and user has to press the corresponding special function key. If code received is not correct, "EE" is displayed.

Otherwise, the next annunciator light corresponding to the Special Function key to press is lit.
The order in which the Special Function keys must be pressed is :
SFK 1, SFK 2, SFK 3, . . . . . , SFK 9.




## 4-10. ADDRESS TEST = TST 10

This test is run with one terminal whose internal address is set to any desired value (between 1 and 77 octal), connected to the computer via the test cable (HP part no. 92900-60000).

The test checks proper operation of the terminal addressing mechanism.

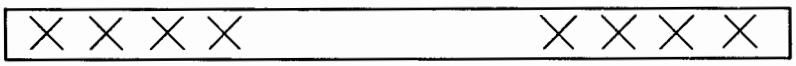
The operator sets an address during a halt, presses RUN. The terminal display indicates the address of the responding terminal while information is sent to the terminal annunciator lights section a hundred times.

A halt then occurs to allow change of address on the terminal and shows last address tested in A-register.
It is recommended to first test addresses 21 and 42 (decimal), 25 and 52 (octal), 0 1 0 1 0 1 and 1 0 1 0 1 0 (binary).
To abort this test section set bit 7 on S-register.

## 4-11. CABLE TEST = TST 11 (OPTIONAL)

This test is run with only one terminal switched ON (at a time) on the serial link under test. The terminal address must be set to 77 (octal).

The test is executed to measure the quality of transmission on a given cable. While the test runs, the terminal displays the number of retransmission requests for the last thousand outputs as well as the total retransmission requests (both quantities in octal). Quantities are updated every 1000 transmissions.



Retransmission requests (octal) for the last thousand outputs

Total retransmission requests since test section beginning (octal)

For example, the retransmission rate should not exceed 0.5 % in a low electrical noise environment and a short link cable (≅ 50 feet).

To abort test set S-register bit 7.

## 4-12. EXTENTED CABLE / CONTROLLER TEST = TST 12 (OPTIONAL)

This test is run with only one terminal switched ON (at a time) on the serial link under test. The terminal address is set to any desired value between 1 and 77 (octal).

The test allows verification of resynchronization function and resolution of muting zones problems that could exist on an installation because of controller "perfect bit" ROM failure.

The terminal address is displayed and the keyboard is configured.

The operator has to type up to 15 characters + Enter within 15 seconds. Operator input from keyboard is channelled through the cable, the controller, to the CPU and sent back to the terminal where it is redisplaved along with the terminal address.

- The operator may now select a new address or a new position on the link and perform the same operations again.

Error messages for Terminal address variation will occur but operator has to press RUN to continue because the origin of this halt is obvious after a change.
To abort this test section set S-register bit 7 and press ENTER.

## 4-13. TOTAL INSTALLATION TEST = TST 13 (OPTIONAL)

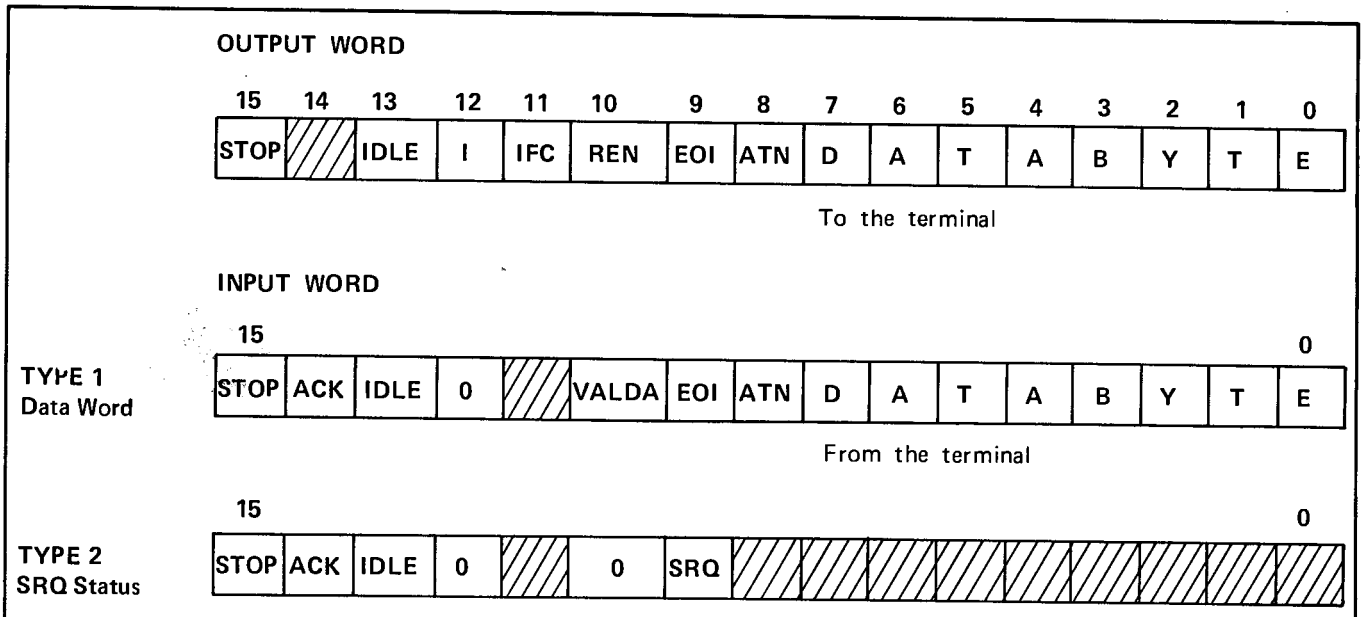
This test is in fact a small program which is able to test simultaneously each one of 63 terminals (1 by address number) in the following manner.

- Detects service requests (coming from any terminal keyboard).
- Clears the request via a Serial Poll sequence.
- Switch ON, then OFF all prompting lights.
- Configures the terminal for input.
- Accepts input sequence :
  if special function key, switches ON corresponding prompting lights.
  if numbers waits until ENTER is depressed or 16 characters are entered, then re-displays the input string.
- Deconfigure the terminal and wait for another service request (this test allows a complete installation check without the need for a configured RTE System.

Running this test :

- Once the test has been selected (see 3-6 and table 3-3) the computer halts with T-Reg = 106007. Operator has to set S-Reg = polling cycle length (maximum number of terminals on the link or highest terminal address on the link) in bits 5-0, then press RUN.
- Test each terminal on the link by pushing the Service Request Key and following the sequence above described.
- To abort this test set S-Reg bit 7 to one.

Fig. 4-1. Data Transfer Table Word Format




STOP = 0 last
1 not last
} Data Transfer Table Word

ACK = 0 Transmission error
1 Transmission all right

IDLE = 1 Output : Set terminal idle
input : terminal is idle
0 Output : Set terminal working
input : terminal is working

VALDA = 0 no data byte transfered for this input
1 bit 0-9 valid and reflecting data lines +control lines of HP-IB

SRQ = 0 no SRQ pending on HP-IB
1 SRQ pending on HP-IB in conjonction with VALDA = 0

IFC = 1 causes the IFC one-shot to be triggered. This sets the BUS signal line IFC (Interface Clear) low which unadresses all Talkers and Listeners, clears the Serial Poll Mode and deactivates all other controllers.
0 inactive.

REN = 1 causes the Bus signal line Remote Enable to be Low. This enables all devices on the Bus to switch to remote control when addressed to listen to their remote programming codes.
0 inactive.

EOI = 1 causes the Bus Signal line End Or Identify to be low. This indicates that the next byte sent as a Talker is the last in the string or, when ATN = "1", initiates a Parallel Poll. Devices so equipped, respond on a preassigned data line.
0 inactive.

ATN = 1 causes the Bus signal line Attention to be Low. This puts the Bus into the Command Mode which enables the computer to send Commands and Addresses.
0 Allows the Bus signal line Attention to be high. This puts the Bus into the Data Mode so that the Talker and Listener(s) may transmit data.

Table 4-1. Summary of Halt Codes

| Halt | Meaning |
|---|---|
| Tests 0 to 13 | |
| 102000-102067 | Error (E) & Information (H) messages 00 - 67 |
| 106000-106027 | Error (E) & Information (H) messages 100 - 127 |
| Control | |
| 102073 | Select Code Input error |
| 102074 | Select Code Input complete |
| 102075 | User Selection Request |
| 102076 | End of Test (A register = Test number) |
| 102077 | End of Diagnostic Run |
| 106077 | Trap cell halts in location 2 - 77 |



**Note :**
See table 4-2 for a complete explanation of individual halts.

Table 4-2. Halts and Messages

| Halt code | Test | Message | Comments |
|---|---|---|---|
| None | Test Control | START 92600A subsystem Diagnostic | Header message. Output at initial start of diagnostic. |
| None | Test Control | Test XX | Information message before error message (XX = test number). Message occurs only once within a test and is suppressed for any subsequent messages within the same test. |
| 102000 | Test 0 | E000 CLF0 - SFC0 | CLF/SFC0 combination failed. CLF did not clear flag or SFC caused no skip with flag clear. |
| 102001 | Test 0 | E001 CLF0 - SFS0 | CLF/SFS0 combination failed. CLF did not clear flag or SFS caused no skip with flag clear. |
| 102002 | Test 0 | E002 STF0 - SFC0 | STF/SFC0 combination failed. STF did not set flag or SFC caused skip with flag set. |
| 102003 | Test 0 | E003 STF0 - SFS0 | STF/SFS0 combination failed. STF did not set flag or SFS caused skip with flag set. |
| 102004 | Test 0 | E004 CLF0 did not inhibit int | With interface Flag and Control set, CLF0 did not turn off interrupt system. |
| 102005 | Test 0 | E005 CLFSC - SFCSC | CLF/SFS SC combination failed. CLF did not clear flag or SFC caused no skip with flag clear. |
| 102006 | Test 0 | E006 CLF SC - SFS SC | CLF/SFS SC combination failed. CLF did not clear flag or SFS caused skip with flag clear. |

Table 4-2. Halts and Messages (cont'd)

| Halt Code | Test | Message | Comments |
|---|---|---|---|
| 102007 | Test 0 | E007 STF SC - SFC SC | STF/SFC SC combination failed.<br>STF did not set flag or SFC caused with flag set. |
| 102010 | Test 0 | E010 STF SC - SFS SC | STF/SFS SC Combination failed.<br>STF did not set flag or SFS caused no skip with flag set. |
| 102011 | Test 0 | E011 STF XX<br>Set cart flag | Select Code screen test failed.<br>A Register contains XX, where XX = select code that caused that interface flag to set. |
| 102012 | Test 0 | E012 int during<br>hold off instr. | Interrupt occured during an I/O intruction or a JMP/JSB indirect instruction. |
| 102013 | Test 0 | E013 second int occured | Card interrupted a second time after initial interrupt was processed and interrupt system was turned back on. |
| 102014 | Test 0 | E014 no int | No interrupt occured with interface flag and control set and the interrupt system ON. |
| 102015 | Test 0 | E015 int RTN addr | Interrupt did not store the correct return address in memory. |
| 102016 | Test 0 | E016 CLC SC | CLC SC did not clear interface control with the interrupt system ON. |
| 102017 | Test 0 | E017 CLC0 | CLC0 did not clear interface control. |
| 102020 | Test 0 | E020 preset (EXT)<br>did not set flag | Preset (EXT) did not set the interface flag. |
| 102021 | Test 0 | E021 preset (INT)<br>did not disable ints | Preset (INT) did not disable the interrupt system. |
| 102022 | Test 0 | E022 preset (EXT)<br>did not clear control | Preset (EXT) did not clear control. |
| 102023 | Test 0 | E023 preset (EXT)<br>did not clear I/O lines | Preset (EXT) did not clear I/O data lines.<br>Data lines should be zero. |
| 102024 | Test 0 | H024 press preset,<br>(EXT & INT) run | Press Preset (External, Internal) then RUN. |
| None | Test 0 | H025 BI-O comp | Basic I/O tests completed. |
| 102026 | Test 0 | E026 int execution | Interrupt was not processed correctly and one or several instructions have been processed incorrectly during the interrupt. |
| None | Test 1 | Test 01 controller test | Begin Test 1 execution. |
| 102030 | Test 1 | H030 all terminals on loop<br>must be off, press run | All terminals connected to the loop must be switched OFF (to test bit 14 returns with logic level 0 for each terminal address). Press RUN then. |
| 102031 | Test 1 | H031 end test 01 :<br>set one terminal on with<br>Address 77 octal, press run | End of test 1, switch one terminal ON for the following tests.<br>Address must be 63 (77 octal). |
| 102032 | Test 1 | E032 flag not set within the<br>required time | Controller flag did not set within the appropriate time delay after forced completion of a polling cycle. Controller is faulty. |

Table 4-2. Halts and Messages (cont'd)

| Halt Code | Test | Message | Comments |
|---|---|---|---|
| 102033 | Test 1 | E033 flag not set should be set (input) | Controller flag did not set during OTA SC, C sequence (when transfering data from memory to controller RAM). |
| 102034 | Test 1 | E034 flag not set, should be set, (output). | Controller flag should be set during LIA SC, C sequence (when transfering data from controller RAM to memory). |
| 102035 | Test 1 | E035 Bit 15 set in last transfer table word | Bit 15 was set to "0" in last Transfer Table word and must remain "0".<br>Found with logic level "1" here, controller is faulty. |
| 102036 | Test 1 | E036 data received different from data sent (B = RAM addr) press run | Controller returns bad data from a RAM addr (B-reg = addr), (A-reg = bits in error), after OTA SC, LIA SC sequence.<br>Press RUN to have more information. |
| 102037 | Test 1 | E037 data received different from data sent A = received, B = sent, press run | This halt follows halt E036. A reg = Data Received. B-reg = Data sent. |
| None | Test 2 | Test 02 communication module test | Begin communication Module Test. |
| None | Test 3 | Test 03 terminal functions test | Begin General Functions Test for Terminal. |
| 102042 | Test 3 | H042 check keyboard is configured & display clear, press run | If display not cleared, logic responding to IFC faulty. If keyboard not configured, logic responding to "configure talker" or keyboard addressing faulty. |
| 102043 | Test 3 | H043 check keyboard is deconfigured, press run | If keyboard not deconfigured, logic responding to IFC faulty. (deconfigure talker). |
| 102044 | Test 3 | H044 press run, check display remains clear while typing charact. +ENTER | If display not clear when typing in any characters+ ENTER, logic responding to IFC faulty. (deconfigure listener). |
| 102045 | Test 3 | H045 check display is clear & press run to display charact. typed in | Display must be clear before pressing run because not yet configured as listener. If not display circuits or addressing faulty. |
| 102046 | Test 3 | H046 press run, type any character within 15 sec. | Press RUN and type in any characters within 15 sec to test that nothing is transmitted from the HP-IB to the Serial Link because the communication module is not configured as a listener. If not, listener of communication module faulty. |
| 102047 | Test 3 | H047 press run, press service, request key within 15 sec. | Press RUN and press SRQ key to verify request is received with every thing deconfigured. If not, SRQ circuits faulty. |
| 102051 | Test 3 | E051 character received with comm.module deconfigured | Communication Module not deconfigured as listener Logic responding to IFC faulty. |
| 102052 | Test 3 | E052 no service request during delay | Error if service request key actually pressed (SRQ circuit faulty). Otherwise press RUN then press service request key as required. |

Table 4-2. Halts and Messages (cont'd)

| Halt Code | Test | Message | Comments |
|---|---|---|---|
| 102053 | Test 3 | E053 ack received when not allowed | Controller received response (bit 14) from terminal placed in IDLE STATE (bit 13). Controller or communication module faulty. |
| None | Test 3 | H054 terminal functions test completed | End of terminal functions Test (IDLE & SRQ are ON) |
| 102055 | Test 4 | Test 04 annunciator lights test H055 press run, check according to manual | Begin Prompting Light Test. |
| 102056 | Test 5 | Test 05 display test H056 press run, check according to manual | Begin Display Test. |
| 102057 | Test 5 | H057 display must be clear & remain clear, press run | If display not clear, logic responding to "clear display" faulty. Display must remain clear because deconfigured as listener. |
| 102060 | Test 5 | H060 if display not clear = error, press run | If display not clear, logic responding to "deconfigure listener" or display addressing faulty. |
| 102061 | Test 6 | Test 06 keyboard test H061 press run, check according to manual. | Begin keyboard test. |
| 102062 | Test 7 | Test 07 special function keys test. H062 press run check according to manual. | Begin Special Function Keys test. |
| None | Test 10 | Test 10 address test | Begin Address Test. |
| 102064 | Test 10 | H064 set terminal address you want to test, press run | It is recommended to always test terminal addresses $21_{10}$ and $42_{10}$ ($25_8$ and $52_8$) which are basic patterns for address switch. |
| 102065 | Test 10 | H065 test ok (A reg = addr) change terminal address, press run | ACK received from only one origin. Origin address displayed on terminal and stored in A Register. New Address test possible : Change terminal address and Press RUN. |
| 102066 | Test 10 | E066 terminal addr variation : A actual, B excepted, press run | Unexpected ACK found during last polling cycle.<br>A-reg = Time window address.<br>B-reg = normal time window address.<br>(Replace terminal unit to isolate failures in Controller or Terminal). |
| 102073 | Configuration | None | I/O Select Code entered at configuration is invalid. Must be greater than 7. Re-enter a valid select code and press RUN. |
| 102074 | Configuration | None | Select code entered during configuration valid. Enter program options in S-reg and press PRESET, RUN. |
| 102075 | Control | None | Test selection request resulting from S-register bit 9 being set. Enter into A - and B - registers the desired test (S) to be run (see table 3.3) Clear S-register bit 9 and press RUN. |

Table 4-2. Halts and Messages (cont'd)

| Halt Code | Test | Message | Comments |
|---|---|---|---|
| 102076 | Control | None | End of test halt resulting from S-register bit 15 being set. The A-Register contains the test number of the test just executed. |
| 102077 | Control | Pass XXXXX | Pass number XXXXX of the diagnostic is complete. A-Register contains the pass count equal to XXXXX, Press RUN to execute another pass. |
| None | Test 11 | Test 11 cable quality test | Begin Cable Quality and Transmission test. |
| 106001 | Test 11 | H101 set terminal address (77 octal), press run | Technical halt for terminal address setting at 63 (77 octal) press run. |
| 106002 | Test 11 | E102 terminal addr variation, A actual, B expected, press run | Ensure terminal address is 77, if so unexpected ACK found during last polling cycle. Replace terminal unit to isolate faulty terminal or (controller) device. A-reg = erroneous response address. B-reg = 63 (77 octal) normal address. |
| None | Test 12 | Test 12 extented cable/ controller test | Begin Extended Cable / Controller Test. |
| 106004 | Test 12 | H104 set terminal address (see manual), press run | Technical halt to allow terminal address setting between 1 and 63. Refer to paragraph 4-12. |
| None | Test 13 | Test 13 total installation test | Begin total Installation Test. |
| None | Test 13 | Total installation test complete | End of test 13 occurs because S reg bit 7 set. |
| 106007 | Test 13 | H107 enter max terminal address (S reg bit 5-0) press run | Halt to allow specification of polling cycle length. (1 to N, N= octal number $\leq$ 77 in S register bit 5 - 0). If left to 0 : equivalent to 77 (max polling cycle length). |
| 106010 | Test 2 to Test 12 | E110 flag not set | Controller did not set during OTA SC, C sequence (when transfering data from memory to controller RAM). |
| 106011 | Test 2 to Test 13 | E111 flag not set within the required time | Controller flag did not set within the appropriate time delay after forced completion of last polling cycle or LIA SC, C instruction. May be no terminal address in polling cycle, (check if terminal is ON). |
| 106012 | Test 2 | E112 data received different from data sent (B = ram data)<br>Press run | Controller returns bad data from a RAM addr (B-Reg = addr) (A-Reg = bad data). Press RUN to get bad data and expected data. |
| 106013 | Test 2 | E113 data received different from data sent<br>A = RCVD,<br>B = SENT, press run | Controller returns bad data from a RAM addr = (A-Reg = bad data), (B-reg = data expected).<br>See data Transfer Table Word format to analyze signification of bits. |
| 106014 | Test 13 | E114 invalid response during serial poll, press run | The keyboard raised SRQ, on a Serial Poll it should reply with OK (Bit 14), Valda (Bit 12) and Bit 6 in Data Transfer Table Word. Condition not met here. Press run and try again. |

Table 4-2. Halts and Messages (cont'd)

| Halt Code | Test | Message | Comments |
|---|---|---|---|
| 106015 | Test 2 to<br>Test 7<br>Test 11<br>Test 12 | E115 Hardware failure or no key pressed within delay, Press run | Controller flag did not set within 15 sec delay. Error if character actually typed in (logic flag set responding faulty. If no character typed in, press RUN and continue. |
| 106016 | Test 11 | E116 more than one ack received, Press run | Controller has detected two or more acknowledgments when only one is expected during this polling cycle. |
| 106017 | Test 10<br>Test 12 | E117 no ack received, Press run | Controller did not find any acknowledgment when one was expected during last polling cycle. (Check if terminal is ON). |
| 106020 | Test 2 to<br>Test 12 | E120 bit 15 set on last transfer table word | Bit 15 was set to "0" in last Transfer Table Word and must remain "0". Found with logic level "I" here Controller is faulty. |
| 106021 | Test 2 to<br>Test 12 | E121 bit 15 clear & not last transfer table word | Bit 15 was set to "I" in Transfer Table Word and must remain "I". Found with logic level "0" here Controller is faulty. |
| 106022 | Test 2 to<br>Test 7<br>Test 11<br>Test 12 | E122 terminal address variation, press run | Acknowledgment received at the wrong window time during the last polling cycle. |
| 106023 | Test 2 to<br>Test 7<br>Test 11<br>Test 12 | E123 SRQ detected when not expected. | Operator has to press SRQ key only during test 3 or 13. If SRQ has not been depressed inadvertently then a faulty SRQ has happened. |
| 106024 | Test 2 to<br>Test 7<br>Test 11<br>Test 12 | E124 invalid interrupt | Controller sets flag when the following logic condition is verified : OK. IDLE. (INT + VALDA +COI) Flag is set here with logic condition not verified |
| 106025 | Test 2 to<br>Test 7<br>Test 11<br>Test 12 | E125 valda & service request simultaneously | Valda bit and SRQ bit both set to 1 Illegal possibility with terminal alone (Valda = I and COI = I $\Rightarrow$ EOI) |
| 106026 | Test 2 to<br>Test 7<br>Test 11<br>Test 12 | E126 ack received but not from proper address | Controller finds the ACK condition in a different polling cycle time window. (Not an error if happening after a terminal address change in Test 12). |
| 106027 | Test 6<br>Test 7 | E127 data received from unexpected address | Data byte and acknowledgment condition received at the wrong window time during the last polling cycle. |

Table 4.3. Test Execution Time.

| TEST SECTION | | EXECUTION TIME |
|---|---|---|
| TST 00 | Basic I/O | 1 SEC |
| TST 01 | Controller test | 3 SEC |
| TST 02 | Communication Module Test | 5 MN |
| TST 03 | Terminal Functions | *** |
| TST 04 | Prompting Lights | 30 SEC |
| TST 05 | Display | 3 MN |
| TST 06 | Keyboard | *** |
| TST 07 | Special Function Keys | *** |
| TST 10 | Address Test | ***** |
| TST 11 | Cable Test | ***** |
| TST 12 | Extended Cable/Controller Test | ***** |
| TST 13 | Total Installation Test | ***** |
| *** | Depends on operator response | |
| ***** | Depends on operator decision to end this test section. | |