FC370-673x

Server Boards

for

Density Series™ Systems

User's Guide

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User's Guide
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Chapter 1 – Introduction

The Cubix Density Series™ System houses multiple server-class Intelâ compatible computers neatly and efficiently in a single rack-mountable drawer (see Figure 1). The Density Series™ System is designed for the purpose of computer consolidation. Cubix equipment solves the problems associated with space-constrained backroom computing centers.

Cubix's versatile new FC370 series boards are Density processor boards which support both Pentiumâ III and Celeron processors. The FC370-673x board can plug into any one of the independent groups on a Density backplane. ("group" refers to a segment of slots within the backplane that will accommodate a Density processor board and peripheral third party card(s), which comprise the server-class system.) As many as eight of the new FC370-673x boards, with Pentiumâ III processors, can be installed in a Density, giving you the maximum power and performance you may require for your application needs.

This ***User's Guide*** provides switch and jumper settings, the steps necessary for proper installation of the board and information regarding the technical specifications of the FC370-673x board.

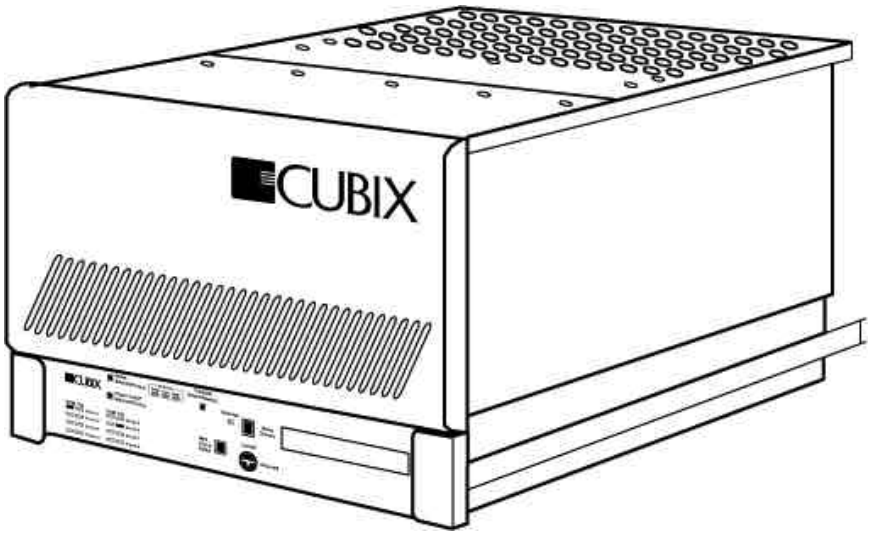


Figure 1 Density Series™ System

OVERVIEW

The FC370-673x board presented in this manual is the third board built in the FC370 Series of server boards for the Cubix Density Series™ Systems. This board uses the VIA chipset and supports the Pentiumâ III processors. The Pentiumâ III processor has a processor speed of up to 866Mhz. The FC370-673x board uses a 100/133Mhz front side bus for the Pentiumâ III.

Once installed in a Cubix Density System, each FC370 series board becomes an independent computer. The system multiplexor allows all Density computers in a chassis to share a single floppy disk drive and CD-ROM drive. The monitor, mouse and keyboard may be shared among computers and multiple chassis (up to 8 chassis).

The FC370-673x computer board includes on-board video, on-board audio, two serial ports, one parallel port, USB, keyboard and mouse support, memory and floppy drive support. Also included are two integrated Ethernet controllers each with 10/100 Base-TX connectors. The FC370-673x board supports one PCI expansion slot.

The FC370-673x board has an integrated Wide Ultra2 SCSI controller with Single-Ended or Low Voltage Differential (LVD) support to an internal SCSI connector. The board layout is pictured in Figure 2.

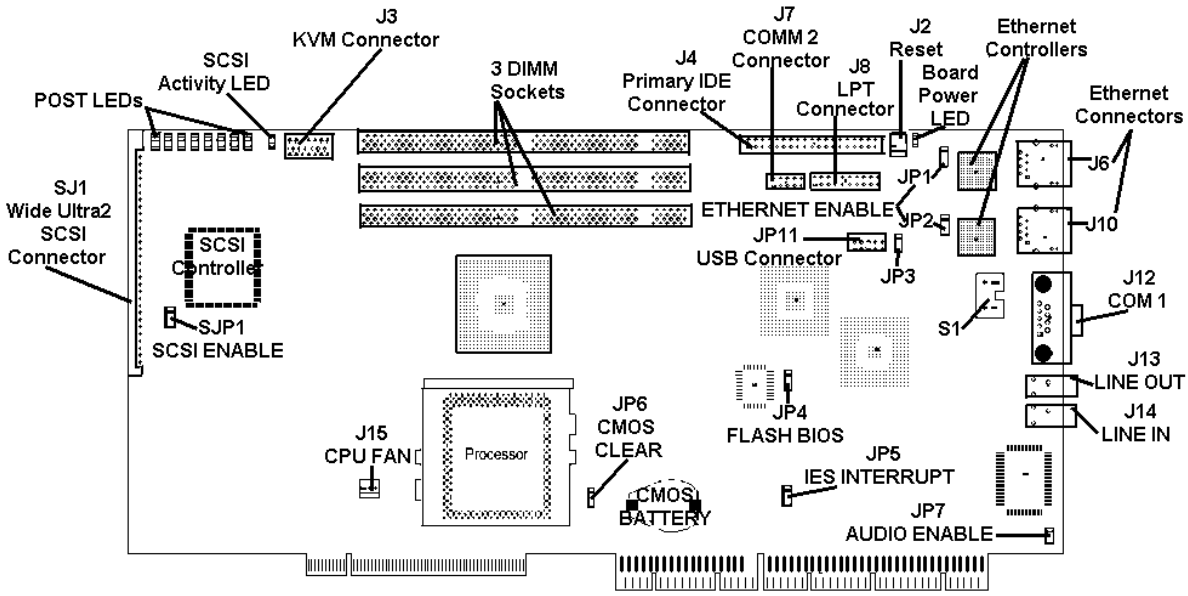


Figure 2 FC370-673x Board Layout

Chapter 2 – The FC370-673x Board

Switch 1 (S1) Settings

S1 – Position 1

The FC370-673x board comes equipped with a 2 position DIP switch for reset control. Position 1 is for data set ready (DSR). If position 1 is set in the "on" position (the "on" and "off" positions are designated by an arrow clearly marked on the switch), the FC370-673x board will reset the CPU on loss of data set ready. The factory default setting for S1, position 1, is in the "off" position.

S1 – Position 2

S1, position 2, is for data carrier detect (DCD). If position 2 is set in the "on" position, the FC370-673x board will reset the CPU when there is a loss of carrier. The factory default setting for S1, position 2, is in the "off" position. See Figure 2 for Switch 1 (S1) location.

Table 1 defines the switch positions for S1.

Table 1 S1 Switch Settings

Function of Reset Control Switch (S1)	1	2
Reset on Loss of DSR	On	
Do Not Reset on Loss of DSR	Off	
Reset on Loss of DCD		On
Do Not Reset on Loss of DCD		Off
Factory Settings	Off	Off

Jumper Settings

JP1 and JP2 – On-Board Ethernet Controller/Jumper Settings

The board is equipped with two integrated Intelâ 82559 PCI fast Ethernet controllers, each with RJ-45 10/100 BASE TX connectors on the mounting bracket at the rear of the board. The I/O addresses and interrupts are set by the PCI plug and play BIOS at boot time. The controllers are enabled or disabled via jumpers JP1 and JP2 (see Figure 2 for jumper locations).

JP1 corresponds to the top Ethernet controller and the top Ethernet port. JP2 corresponds to the bottom Ethernet controller and bottom Ethernet port. For unique situations requiring the disabling of the Ethernet controllers, JP1 and JP2 are incorporated onto the FC370-673x board.

Table 2 defines the jumper settings for JP1 and JP2

Table 2 Ethernet Jumper Settings for JP1 and JP2

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP1	Ethernet	Enabled	Disabled
JP2	Ethernet	Enabled	Disabled

JP4 – Flash Bios Enable

If the Flash Bios is to be upgraded, a shunt must be installed on the 2-pin jumper JP4 (see figure 2 for JP4 location). Upgrades typically come on a floppy disc and are accompanied by upgrade instructions.* When the upgrade is complete, the shunt should be removed to protect the system from accidental erasure.

Table 3 defines the jumper settings for JP4.

Table 3 Write Enable/Flash BIOS Jumper Settings for JP4

Jumper	Function	Jumper On	Jumper Off
JP4	Flash Write Enable	Enabled	Disabled

*Cubix provides Flash Bios upgrades via the Cubix web site. The web site address is provided in Appendix A of this manual.

JP5 – IES Interrupt on IRQ10

The IES module communicates with the FC370-673x processor in the subsystem via a hardware interrupt which is IRQ10. The supervisory interrupt is enabled with JP5 by placing the jumper on pins 1 and 2. If the FC370-673x board is part of the GlobalVision network, supervisory interrupt is necessary and IES Interrupt must be enabled. If this board is not part of the GlobalVision network, IES Interrupt can be disabled with JP5 by removing the jumper from pins 1 and 2, and placing the jumper on pins 2 and 3. The factory default setting for JP5 is in "enabled" status, unless otherwise specified at the time of purchase.

Table 4 defines the jumper settings for JP5.

Table 4 Enable/Disable IES Interrupt Jumper Settings for JP5

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP5	IES Interrupt on IRQ10	Enabled	Disabled

JP6 – CMOS Memory Clear

The CMOS memory can be cleared by using JP6 (see Figure 2 for JP6 location). This memory controls the maintenance and storage of three sets of information: (1) the date and time generated and displayed on the computer screen; (2) the peripheral setup, i.e. programming base register for the chip sets; and (3) the password necessary for entry.

The first two sets of information can be changed during boot-up by following specific directions displayed on the computer screen at the time the computer boots up. The CMOS memory will automatically update and store the new information input. However, if setup cannot be entered the normal way, CMOS memory clear (JP6) is the recovery mechanism which can be used. Or, if password information has been lost, the CMOS memory will need to be cleared so the information can be updated before program entry is possible.

To clear CMOS memory, the jumper on JP6 must be removed from pins 1 and 2, and placed on pins 2 and 3. After clearing, the jumper must be reinstalled on jumper pins 1 and 2 before updates can be made.

Table 5 defines the jumper settings for JP6.

Table 5 CMOS Clear Jumper Settings for JP6

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP6	CMOS Clear	Normal Operation	CMOS Clear

JP7 – Audio Enable/Disable

The FC370-673x board comes equipped with audio capacity. The factory default setting for JP7 is in "enabled" status unless otherwise specified (the shunt installed on pins 1 and 2). To disable the audio, remove the shunt from pins 1 and 2 and replace the shunt on pins 2 and 3. External amplified speakers may be plugged into the Line Out port (J13) to listen to computer generated sound. The Line In port (J14) can be used to bring audio into the computer for recording purposes. A 1/8" stereo phono jack can be used to make the connection.

Table 6 defines the jumper settings for JP7.

Table 6 Audio Enable/Disable Jumper Settings for JP7

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
JP7	Audio	Enable	Disable

Other Jumper Settings and Connectors

JP3 is currently not available and reserved for future use. J4, a Primary IDE connector, is also unavailable and reserved for future use.

Symbios SCSI Controller/Jumper Settings

The FC370-673x board has an integrated Wide Ultra2 SCSI controller with Single-Ended or Low Voltage Differential (LVD) support to an internal SCSI connector. The controller is enabled or disabled via a hardware jumper SJP1. (The "S" preceding the "JP" designates the jumper is specific to SCSI functions.)

The SCSI controller is a bus master device which gains control of the PCI bus to transfer data between the CPU memory and the SCSI devices. The I/O base address and interrupts are set by the PCI plug and play BIOS at boot time.

SJP1 – Enable/Disable SCSI Controller

As stated above, the on-board Symbios Wide Ultra2 SCSI controller can be enabled or disabled with SJP1 (see Figure 2 for SJP1 location).

Table 7 defines the jumper settings for SJP1.

Table 7 SCSI Jumper Settings for SJP1

Jumper	Function	Jumper On Pins 1-2	Jumper On Pins 2-3
SJP1	SCSI	Enabled	Disabled

DIMM MEMORY INSTALLATION

Additional memory can be installed on the FC370-674x board. There are three DIMM slots available on this board (see Figure 2 for DIMM slot locations). If only one DIMM is installed, this DIMM should be installed in the DIMM located closest to the top edge of the board. The sequence of DIMM installation relative to DIMM size is not important. DIMMs must be PC-100 compliant to run at 100MHz or PC-133 to run at 133MHz.

For installation, the card interface tabs must be aligned. Firmly seat the DIMM(s) into place.

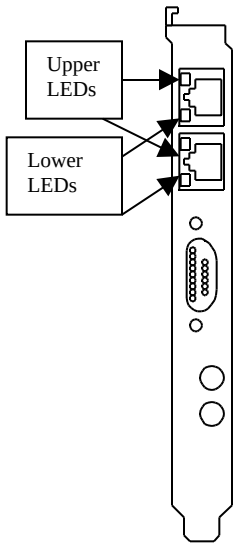
Please note the following information regarding DIMMs.

- DIMMs are 168 pin, 100MHz or 133MHz ECC SDRAM (72 bits).
- DIMMs do not need to be installed in pairs and different sizes may be mixed.
- DIMMs may be either registered or unbuffered. Registered and unbuffered DIMMs may not be mixed.
- DIMMs must have gold contacts (edge connectors).

*Pentium III processors can use either PC-100MHz or PC-133MHz memory sticks.

FC370-673X Board Information and Technical Specifications

Figure 3 - End Bracket for FC370-673x



ETHERNET ADAPTER LEDs

On each RJ-45 connector and visible in the mounting bracket is a set of light emitting diodes (LEDs). Figure 3 displays the FC370-673x end bracket.

On the upper LED:

- When the upper LED is green and blinking, this indicates a link to an Ethernet hub and that when blinking, there is activity.

On the lower LED:

- When the lower LED is green, this indicates the interface is set to 100 Mbit/s.

OTHER LEDs

POST Display

The FC370-673x board has a group of eight LEDs arranged to the right of the SCSI connector (SJ1) (see Figure 2 for POST LED location). As the system proceeds through its Power On System Test (POST) these LEDs display binary codes which can be used to diagnose board failures. Refer to the AMIBIOS POST Checkpoint Codes (Doc. #0882) for detailed POST code information, or check the Cubix website:

http://www.cubix .com

FC370-673x Board Power LED

There is a Board Power LED on the FC370-673x board which is located to the right of the Reset Jumper (J2) (see Figure 2 for Board Power LED location). This LED light will be green when there is power to the board. This LED is only visible when the cover is off the Density System.

SCSI Activity LED

There is a SCSI Activity LED located to the right of SJ1 and below the POST LEDs. This light will be amber when the SCSI is busy and is only visible when the cover is off the Density System.

MEMORY CONFIGURATION & INTERRUPTS

Table 8 shows the Memory map for the processor.

Table 8 Memory Map

Memory Range	Size	Use
00000-9FFFF	640KB	Conventional Memory
A0000-AFFFF	64KB	VGA Graphics Buffer
B0000-B7FFF	32KB	MDA Text Buffer
B8000-BFFFF	32KB	VGA/CGA Text Buffer
C0000-C7FFF	32KB	VGA Bios
C8000-DFFFF	96KB	Available
E0000-FFFFF	128KB	System & PCI BIOS

Table 9 defines the FC370-673x board's I/O configuration.

Table 9 I/O Map

ISA Ports	Description
0000-00FF	Various "AT" functions in ISP chip and keyboard controller
01F0-01F7	IDE hard drive interface
02F8-02FF	COM2
03A0	Cubix supervisory interface
03A8-03AF	IES serial port
03B4-03B5	VGA
0378-037F	LPT1
03C0-03CF	VGA
03D4-03D5	VGA
03F0-03F7	Floppy / IDE
03F8-03FF	COM1

System Interrupts

The 16 system hardware interrupts on the FC370-673x are represented in Table 10.

Interrupts are managed by two standard 8259A Programmable Interrupt Controllers (PICs) integrated into the chipset. Interrupts at IRQ 0 through 7 are located on the main PIC; IRQ 8 through 15 are on the SLAVE PIC.

Table 10 System Interrupts

IRQ	Description	IRQ	Description
0	Timer clock	**8**	Real Time Clock
1	Keyboard	**9**	Redirected IRQ 2, Set By PCI Plug & Play at Boot Time
2	Second PIC controller	**10**	Reserved for IES (Factory Default, see JP4)
3	COM2	**11**	Set By PCI Plug & Play at Boot Time
4	COM1	**12**	Available (or PS/2 Mouse)
5	Set By PCI Plug & Play at boot time	**13**	Math Coprocessor
6	Floppy Disk Controller	**14**	Available
7	LPT1	**15**	Secondary IDE Controller (CD-ROM)

TECHNICAL SPECIFICATIONS

Table 11 Technical Specifications for Density FC370-673X Series Board

CPU – Central Processing Unit	Intelâ Pentiumâ III
L2 Cache	256KB Full Speed on the Pentiumâ III
System Chip Set	VIA Apollo Pro133A
System Memory	
Speed	PC-100MHz or PC-133MHz SDRAM
Width	72 Bits ECC
Max Size	3 – 512KB DIMMS or 1.5GB
Type	Unbuffered or Registered, DO NOT MIX
Peripheral Bus Support	PCI
System BIOS	AMI BIOS
Super I/O	SMsC 37M812
Serial/Assignment	COM1 (J12), COM2 (J7)
UART Type	16C550 Compatible 230 Kbps Maximum
Parallel/Assignment	LPT 1 (J8), all Standard Modes
Dual On-Board LAN Interface	RJ-45 10/100 Base TX, Intelâ 82559 (Ethernet ports – J6 & J10)
VGA Chip Set (AGP Bus)	S3 Savage 4 (82C397) 8MB Video RAM
SCSI Chip Set	Wide Ultra2 SCSI Symbios 53C895 with Low Voltage Differential or Single-Ended SCSI support (internal connector only)
Max Transfer Rate	Single-Ended 40MB, LVD 80MB
Audio Chip Set	Cirrus Logic, CS4281/CS4297A
Other Input/Output	Video/Keyboard/Mouse – (J3) Internal Header
Power Requirements* *Does not include power for IDE Hard Drive	Volts / Amps Max / Power Max +5VDC 7.6A +12VDC 0.25A 41.6W -12VDC 0.05A
Operating Environment	FC370-673X with PIII up to 667MHz: 40C (104F) maximum ambient. FC370-673X with 700MHZ and greater PIII : 32C (90F) maximum ambient.
Warranty	Parts and Labor Return to Manufacturer 3 yrs.

Chapter 3 - Warnings and Board Installation Procedures

WARNINGS

The installation of all processor boards requires entry into the CPU bay of the Density Series system which is restricted to qualified service personnel only. Accordingly, the following warnings apply.

CAUTION!
CONTAINS HAZARDOUS VOLTAGES
NO USER SERVICEABLE PARTS

ATTENTION!
TENSION DANGEREUSE, L'APPAREIL NE COMPORTE AUUN ELEMENT QUE L'UTILISATEUR PULSSE REPARER

ACHTUNG!
GEFAHRLICHE STROMSPANNUNGEN!
KEIN BENUTZER QUGANGLICHE TEILE!

CAUTION!
Group power must be off before installing any Cubix processors, peripheral boards, or third-party peripheral cards. Failure to follow this warning may result in damage to the Density Series system and boards being installed.

BOARD INSTALLATION

The following steps guide through the installation process.

1. At the front console, select and turn power off to the group location where you intend to install the server board.
2. If a hard-drive is installed in the group hard drive slot, remove the hard drive.
3. Confirm the switch and jumper settings are correct on the board being installed.
4. Insert the board into the group slot, ensuring the board interface tabs are aligned with the center of the slot (see Figure 4).
5. Firmly seat the processor board into the slots by firmly pressing on the top of the board with the palm of your hand.
6. Install the hard drive assembly into the appropriate hard drive bay located in the front of the Density enclosure. The hard drive assembly will fit into the hard drive interface. Press firmly to seat.
7. Secure the board in the chassis by tightening the captured screw on the top of the L-bracket.
8. Connect all appropriate ribbon connectors and L-bracket connectors.
9. At the front of the console, apply power to the processor group.

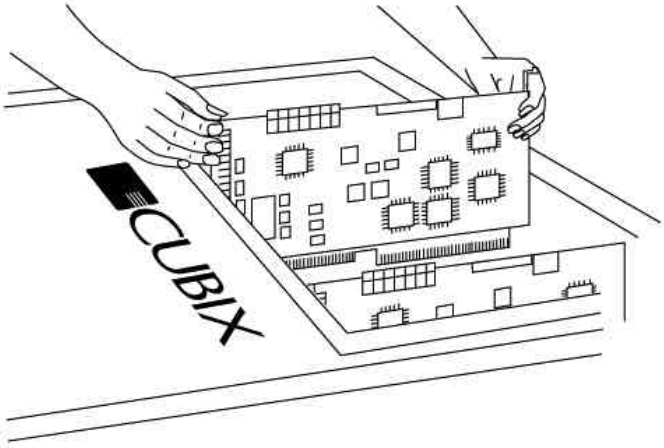


Figure 4 Inserting Server Board into Chasis Group

APPENDIX A

CUSTOMER SERVICE INFORMATION

For Customer Service Information: 1-800-829-0551

Customer Service available from:

5:00 a.m. to 5:00 p.m. PST Monday through Friday
Also, from 8:00 a.m. to 4 p.m. PST on Saturday
Closed holidays and holiday weekends

Use the Cubix Web site for trouble-shooting aids and for access to the latest information on Cubix products.

Customer Service Web site: http://www.cubix.com/support

Customer Service Email address: customerservice@cubix.com