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LINE DEFINITIONS

AD to A15	Address Bit 0 to 15
ADC	Address Enable Control
ADR	Attention
BA	Bus Available
BRACKET	Buffered System Reset
CI HIGH, CI LOW	Internal Cartridge Chip Select
CI HIGH, CI LOW	
CLK	Dynamic RAM Column Address (C1504)
CLK IN	Master Clock (Timing Phase, 14.31818 MHz)
CLAMP	Chroma Output
COMP	Composite Sync and Luma
CS	Chip Enable
CS	Chip Select
CSD	Low ROM Chip Select
CSI	High ROM Chip Select
CYT RTN	Cassette Motor Control
CYT RD	Cassette Read
CYT SENSE	Cassette Sense
CYT WR	Cassette Write
CR	Clear to Read
CR0 to CR7	Data Bit 0 to 7
CC	Data Carrier Detect
DSAR	Dynamic RAM
DSAR ADD	Dynamic RAM Address
DSR	Data Set Ready
DSR	Data Terminal Ready
EXT AUDIO	External Audio Input
DATA IN	DATA
IRQ	Interrupt Request
K0 to K7	Keyboard Latch 0 to 7
KRM	Kernel ROM Control Line
LUM	Composite Sync and Luminance
MMA	Address Multiplexer Control
M0 to M7	DATA Bit 0 to 7
RAD	Dynamic RAM Row Address Strobe
RESET	System Reset
SC0	Service Clock
SC0	Service Data
R/W	Read/Write Line
RTE	Request To Send
RSD	Reset Line
YED	Telet Display
YED	Teletext Data
SC0	System Clock (Stables between 1 and 3 MHz)
SC0	Address Valid Rising Edge, Anticlockwise
SC0	Data Valid Falling Edge